100307 Low Power Quint Exclusive OR/NOR Gate

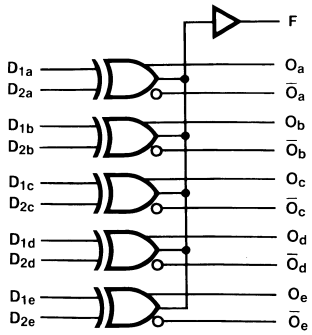
Check for Samples: 100307

FEATURES

- **Low Power Operation**
- **2000V ESD protection**
- **Pin/function compatible with 100107**
- **Voltage compensated operating range = −4.2V to −5.7V**
- **Available to industrial grade temperature range**
- **Available to Standard Microcircuit Drawing**
  - **(SMD) 5962-9459001**

DESCRIPTION

The 100307 is monolithic quint exclusive-OR/NOR gate. The Function output is the wire-OR of all five exclusive-OR outputs. All inputs have 50 kΩ pull-down resistors.



Logic Equation

$F = (D_{1a} + D_{2a}) + (D_{1b} + D_{2b}) + (D_{1c} + D_{2c}) + (D_{1d} + D_{2d}) + (D_{1e} + D_{2e})$.

Pin Names	Description
D_{na}–D_{ne}	Data Inputs
F	Function Output
O_a–O_e	Data Outputs
$\overline{O}_a$–$\overline{O}_e$	Complementary
	Data Outputs

Connection Diagram

Figure 1. 24-Pin DIP

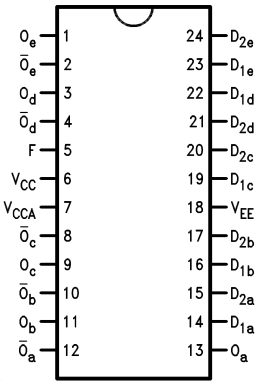
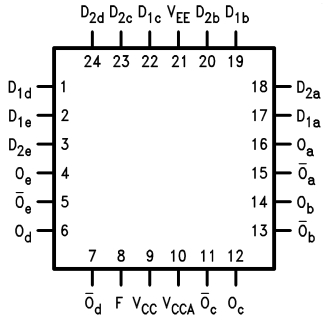


Figure 2. 24-Pin Quad Cerpak



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings (1)

Above which the useful life may be impaired. (1)	
Storage Temperature (T_{STG})	−65°C to +150°C
Maximum Junction Temperature (T_J)	
Ceramic	+175°C
Plastic	+150°C
V_{EE} Pin Potential to Ground Pin	−7.0V to +0.5V
Input Voltage (DC)	V_{EE} to +0.5V
Output Current (DC Output HIGH)	−50 mA
ESD (2)	≥2000V

(1) Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.
(2) ESD testing conforms to MIL-STD-883, Method 3015.

Recommended OperatingConditions

Case Temperature (T_C)	
Military	−55°C to +125°C
Supply Voltage (V_{EE})	−5.7V to −4.2V

Military Version
DC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND, T_C = −55°C to +125°C

Symbol	Parameter	Min	Max	Units	T_C	Conditions		Notes
V_{OH}	Output HIGH Voltage	−1025	−870	mV	0°C to +125°C	V_{IN} = V_{IH} (Max) or V_{IL} (Min)	Loading with 50Ω to −2.0V	*(1)(2)(3)
		−1085	−870	mV	−55°C			
V_{OL}	Output LOW Voltage	−1830	−1620	mV	0°C to +125°C			
		−1830	−1555	mV	−55°C			
V_{OHC}	Output HIGH Voltage	−1035		mV	0°C to +125°C	V_{IN} = V_{IH} (Min) or V_{IL} (Max)	Loading with 50Ω0 to −2.0V	(1)(2)(3)
		−1085		mV	−55°C			
V_{OLC}	Output LOW Voltage		−1610	mV	0°C to +125°C			
			−1555	mV	−55°C			
V_{IH}	Input HIGH Voltage	−1165	−870	mV	−55°C to +125°C	Guaranteed HIGH Signal for All Inputs		(1)(2)(3)(4)
V_{IL}	Input LOW Voltage	−1830	−1475	mV	−55°C to +125°C	Guaranteed LOW Signal for All Inputs		(1)(2)(3)(4)
I_{IL}	Input LOW Current	0.50		µA	−55°C to +125°C	V_{EE} = −4.2V V_{IN} = V_{IL} (Min)		(1)(2)(3)
I_{IH}	Input High Current					V_{EE} = −5.7V V_{IN} = V_{IH} (Max)		(1)(2)(3)
	D_{2a}–D_{2e}		250	µA	0°C to +125°C			
	D_{1a}–D_{1e}		350					
	D_{2a}–D_{2e}		350	µA	−55°C			
	D_{1a}–D_{1e}		500					
I_{EE}	Power Supply Current	−75	−25	mA	−55°C to +125°C	Inputs Open		(1)(2)(3)

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(2) ESD testing conforms to MIL-STD-883, Method 3015.
(3) F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals −55°C), then testing immediately without allowing for the junction temperature to stabilize due to heat dissipation after power-up. This provides “cold start” specs which can be considered a worst case condition at cold temperatures.
(4) Screen tested 100% on each device at −55°C, +25°C, and +125°C, Subgroups 1, 2 3, 7, and 8.

AC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = −55°C		T_C = +25°C		T_C = +125°C		Units	Conditions	Notes
		Min	Max	Min	Max	Min	Max			
t_{PLH}, t_{PHL}	Propagation Delay D_{2a}–D_{2e} to O, $\overline{O}$	0.30	2.10	0.40	1.90	0.40	2.40	ns	Figure 3 Figure 4	*(1)(2)(3)
t_{PLH}, t_{PHL}	Propagation Delay D_{1a}–D_{1e} to O, $\overline{O}$	0.30	1.90	0.40	1.80	0.40	2.20	ns		
t_{PLH}, t_{PHL}	Propagation Delay Data to F	0.80	2.90	0.90	2.80	0.90	3.40	ns		
t_{TLH}, t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.20	1.70	0.30	1.60	0.20	1.70	ns		*(4)

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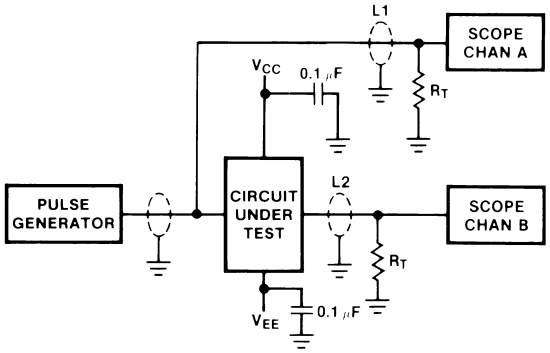
Test Circuitry



Notes:

V_{CC}, V_{CCA} = +2V, V_{EE} = −2.5V

L1 and L2 = equal length 50Ω impedance lines

R_T = 50Ω terminator internal to scope

Decoupling 0.1 µF from GND to V_{CC} and V_{EE}

All unused outputs are loaded with 50Ω to GND

C_L = Fixture and stray capacitance ≤ 3 pF

Figure 3. AC Test Circuit

Switching Waveforms

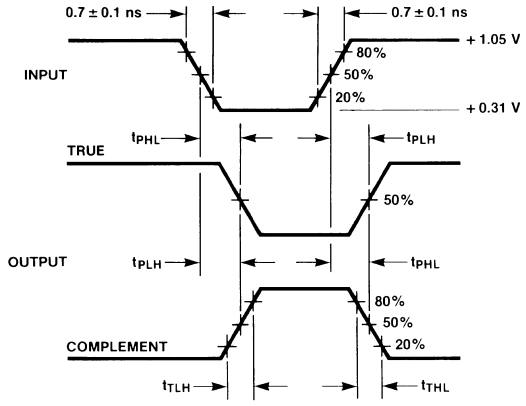


Figure 4. Propagation Delay and Transition Times

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