National Semiconductor

100311
Low Skew 1:9 Differential Clock Driver

General Description

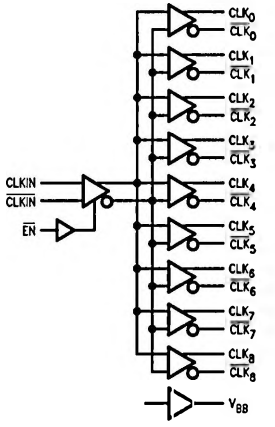
The 100311 contains nine low skew differential drivers, designed for generation of multiple, minimum skew differential clocks from a single differential input (CLKIN, $\overline{CLKIN}$). If a single-ended input is desired, the V_{BB} output pin may be used to drive the remaining input line. A HIGH on the enable pin ($\overline{EN}$) will force a LOW on all of the CLK_n outputs and a HIGH on all of the $\overline{CLK}_n$ output pins. The 100311 is ideal for distributing a signal throughout a system without worrying about the original signal becoming too corrupted by undesirable delays and skew. The 100311 is pin-for-pin compatible with the Motorola 100E111.

Features

- Low output to output skew
- 2000V ESD protection
- 1:9 low skew clock driver
- Differential inputs and outputs

Ordering Code: See Section 5

Logic Symbol



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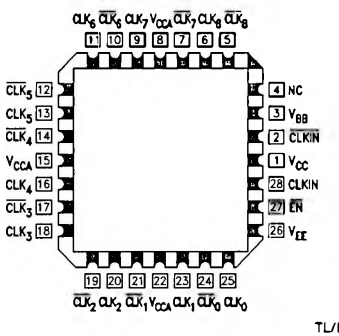
Pin Names	Description
CLKIN, $\overline{CLKIN}$	Differential Clock Inputs
$\overline{EN}$	Enable
CLK_{0-8}, $\overline{CLK}_{0-8}$	Differential Clock Outputs
V_{BB}	V_{BB} Output
NC	No Connect

Truth Table

CLKIN	$\overline{CLKIN}$	$\overline{EN}$	CLK_n	$\overline{CLK}_n$
L	H	L	L	H
H	L	L	H	L
X	X	H	L	H

Connection Diagram

28-Pin PCC



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Absolute Maximum Ratings

Above which the useful life may be impaired (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature (T_{STG})	−65°C to +150°C
Maximum Junction Temperture (T_J)	
Ceramic	+175°C
Plastic	+150°C
Pin Potential to Ground Pin (V_{EE})	−7.0V to +0.5V
Input Voltage (DC)	V_{EE} to +0.5V
Output Current (DC Output HIGH)	−50 mA
ESD (Note 2)	≥2000V

Note 1: Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: ESD testing conforms to MIL-STD-883, Method 3015.

Recommended Operating Conditions

Case Temperature (T_C)	
Commercial	0°C to +85°C
Industrial	−40°C to +85°C
Supply Voltage (V_{EE})	−5.7V to −4.2V

Commercial Version

DC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions	
V_{OH}	Output HIGH Voltage	−1025	−955	−870	mV	V_{IN} = V_{IH} (Max) or V_{IL} (Min)	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1830	−1705	−1620	mV		
V_{OHC}	Output HIGH Voltage	−1035			mV	V_{IN} = V_{IH} or V_{IL} (Max)	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage			−1610	mV		
V_{BB}	Output Reference Voltage	−1380	−1320	−1260	mV	I_{VBB} = −300 μA	
V_{DIFF}	Input Voltage Differential	150			mV	Required for Full Output Swing	
V_{CM}	Common Mode Voltage	V_{CC} − 2.0		V_{CC} − 0.5	V		
V_{IH}	Input High Voltage	−1165		−870	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input Low Voltage	−1830		−1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = V_{IL} (Min)	
I_{IH}	Input HIGH Current CLKIN, $\overline{\text{CLKIN}}$ $\overline{\text{EN}}$			 100 250	μA	V_{IN} = V_{IH} (Max)	
I_{CBO}	Input Leakage Current	−10			μA	V_{IN} = V_{EE}	
I_{EE}	Power Supply Current	−115		−57	mA	Inputs Open	

Note 3: The specified limits represent the "worst case" value for the parameter. Since these values normally occur at the temperature extremes, additional noise immunity and guardbanding can be achieved by decreasing the allowable system operating ranges. Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

Commercial Version (Continued)

AC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = 0°C			T_C = +25°C			T_C = +85°C			Units	Conditions
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
f_{max}	Max Toggle Frequency CLKIN to Q_n	750			750			750			MHz	
t_{PLH} t_{PHL}	Propagation Delay, $CLKIN_n$ to CLK_n											
	Differential	0.75	0.84	0.95	0.75	0.86	0.95	0.84	0.93	1.04	ns	*Figure 3*
	Single-Ended	0.65	0.90	1.05	0.67	0.93	1.17	0.74	1.06	1.24		
t_{PLH} t_{PHL}	Propagation Delay SEL to Output	0.75	1.03	1.20	0.80	1.05	1.25	0.85	1.12	1.35	ns	*Figure 2*
t_{PS}	LH–HL Skew		10	30		10	30		10	30	ps	Notes 1, 4
t_{OSLH}	Gate–Gate Skew LH		20	50		20	50		20	50		Notes 2, 4
t_{OSHL}	Gate–Gate Skew HL		20	50		20	50		20	50		Notes 2, 4
t_{OST}	Gate–Gate LH–HL Skew		30	60		30	60		30	60		Notes 3, 4
t_S	Setup Time EN_n to $CLKIN_n$	250			250			300			ps	
t_H	Hold Time EN_n to $CLKIN_n$	0			0			0			ps	
t_R	Release Time EN_n to $CLKIN_n$	300			300			300			ps	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	275	500	750	275	480	750	275	460	750	ps	*Figure 4*

Note 1: t_{PS} describes opposite edge skews, i.e. the difference between the delay of a differential output signal pair's low to high and high to low propagation delays. With differential signal pairs, a low to high or high to low transition is defined as the transition of the true output or input pin.

Note 2: t_{OSLH} describes in-phase gate-to-gate differential propagation skews with all differential outputs going low to high; t_{OSHL} describes the same conditions except with the outputs going high to low.

Note 3: t_{OST} describes the maximum worst case difference in any of the t_{PS}, t_{OSLH} or t_{OST} delay paths combined.

Note 4: The skew specifications pertain to differential I/O paths.

Note 5: f_{max} = the highest frequency at which output V_{OL}/V_{OH} levels still meet V_{IN} specifications. The F311 will function @ 1 GHz.

Industrial Version

DC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND (Note 3)

Symbol	Parameter	T_C = −40°C		T_C = 0°C to +85°C		Units	Conditions	
		Min	Max	Min	Max			
V_{OH}	Output HIGH Voltage	−1085	−870	−1025	−870	mV	V_{IN} = V_{IH} (Max) or V_{IL} (Min)	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1830	−1575	−1830	−1620	mV		
V_{OHC}	Output HIGH Voltage	−1095		−1035		mV	V_{IN} = V_{IH} or V_{IL} (Min)	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage		−1565		−1610	mV		
V_{BB}	Output Reference Voltage	−1395	−1255	−1380	−1260	mV	I_{VBB} = −300 μA	
V_{DIFF}	Input Voltage Differential	150		150		mV	Required for Full Output Swing	
V_{CM}	Common Mode Voltage	V_{CC} − 2.0	V_{CC} − 0.5	V_{CC} − 2.0	V_{CC} − 0.5	V		
V_{IH}	Input High Voltage	−1170	−870	−1165	−870	mV	Guaranteed HIGH Signal for All Inputs	

Industrial Version (Continued)

DC Electrical Characteristics (Continued)

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND (Note 3)

Symbol	Parameter	T_C = −40°C		T_C = 0°C to +85°C		Units	Conditions
		Min	Max	Min	Max		
V_{IL}	Input Low Voltage	−1830	−1480	−1830	−1475	mV	Guaranteed LOW Signal for All Inputs
I_{IL}	Input LOW Current	0.50		0.50		μA	V_{IN} = V_{IL} (Min)
I_{IH}	Input HIGH Current CLKIN, $\overline{CLKIN}$ $\overline{EN}$		 100 250		 100 250	μA	V_{IN} = V_{IH} (Max)
I_{CBO}	Input Leakage Current	−10		−10		μA	V_{IN} = V_{EE}
I_{EE}	Power Supply Current	−115	−57	−115	−57	mA	Inputs Open
V_{PP}	Minimum Input Swing	150		150		mV	
V_{CMR}	Common Mode Range	V_{CC}−2.0	V_{CC}−0.5	V_{CC}−2.0	V_{CC}−0.5	V	

Note 3: The specified limits represent the "worst case" value for the parameter. Since these values normally occur at the temperature extremes, additional noise immunity and guardbanding can be achieved by decreasing the allowable system operating ranges. Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

AC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = −40°C			T_C = +25°C			T_C = +85°C			Units	Conditions
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
f_{max}	Max Toggle Frequency CLKIN to Q_n	750			750			750			MHz	
t_{PLH} t_{PHL}	Propagation Delay, $CLKIN_n$ to CLK_n											
	Differential	0.72	0.81	0.92	0.77	0.86	0.95	0.84	0.93	1.04	ns	*Figure 3*
	Single-Ended	0.62	0.89	1.02	0.67	0.93	1.17	0.74	1.06	1.24		
t_{PLH} t_{PHL}	Propagation Delay SEL to Output	0.70	0.97	1.20	0.80	1.05	1.25	0.85	1.12	1.35	ns	*Figure 2*
t_{PS}	LH−HL Skew		10	30		10	30		10	30	ps	Notes 1, 4
t_{OSLH}	Gate−Gate Skew LH		20	50		20	50		20	50		Notes 2, 4
t_{OSHL}	Gate−Gate Skew HL		20	50		20	50		20	50		Notes 2, 4
t_{OST}	Gate−Gate LH−HL Skew		30	60		30	60		30	60		Notes 3, 4
t_S	Setup Time EN_n to $CLKIN_n$	250			250			300			ps	
t_H	Hold Time EN_n to $CLKIN_n$	0			0			0			ps	
t_R	Release Time EN_n to $CLKIN_n$	300			300			300			ps	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	275	500	750	275	480	750	275	460	750	ps	*Figure 4*

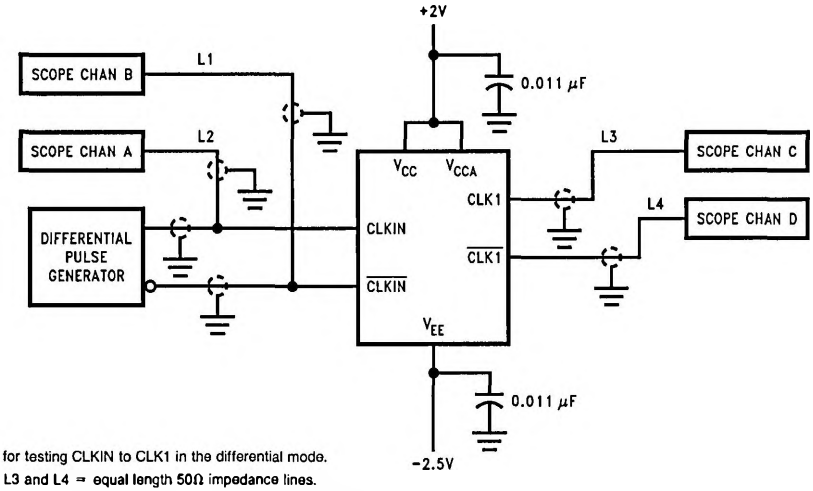
Note 1: t_{PS} describes opposite edge skews, i.e. the difference between the delay of a differential output signal pair's low to high and high to low propagation delays. With differential signal pairs, a low to high or high to low transition is defined as the transition of the true output or input pin.

Note 2: t_{OSLH} describes in-phase gate differential propagation skews with all differential outputs going low to high; t_{OSHL} describes the same conditions except with the outputs going high to low.

Note 3: t_{OST} describes the maximum worst case difference in any of the t_{PS}, t_{OSLH} or t_{OST} delay paths combined.

Note 4: The skew specifications pertain to differential I/O paths.

Test Circuit



Note 1: Shown for testing CLKIN to CLK1 in the differential mode.

Note 2: L1, L2, L3 and L4 = equal length 50Ω impedance lines.

Note 3: All unused inputs and outputs are loaded with 50Ω in parallel with ≤ 3 pF to GND.

Note 4: Scope should have 50Ω input terminator internally.

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FIGURE 1. AC Test Circuit

Switching Waveforms

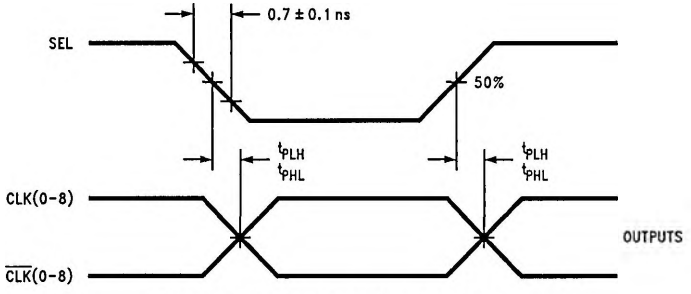

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FIGURE 2. Propagation Delay, $\overline{EN}$ to Outputs

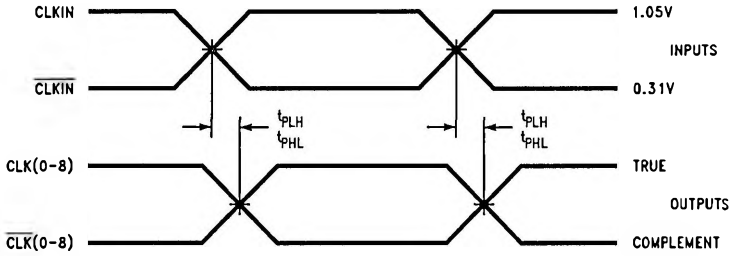

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FIGURE 3. Propagation Delay, CLKIN/CLKIN to Outputs

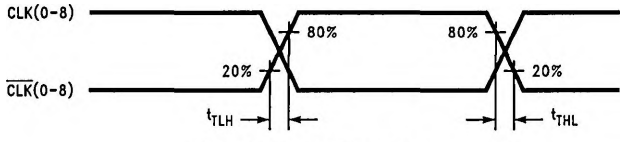

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FIGURE 4. Transition Times