signetics

# 4-WIDE 3,3,3,3-INPUT OR-AND/OR-AND-INVERT GATE

# 10121

10121B,F: –30 to +85°C

**DIGITAL 10,000 SERIES ECL**

## DESCRIPTION

The 10121 is a 4 wide 3-3-3-input OR-AND/OR-AND-INVERT gate. Pin 10 is common to two of the input gates. This function is particularly useful in data control and multiplexing. The 10121 is optimized for high performance applications and has an excellent speed power product. All inputs are terminated with a 50 kΩ resistor to $V_{EE}$ which eliminates the need to tie unused inputs low. The high impedance inputs and high output fanout is ideal for a transmission line environment.

## FEATURES

- **FAST PROPAGATION DELAY FOR 2 LOGIC LEVELS = 2.3 ns TYP**
- **LOW POWER DISSIPATION = 100 mW/PACKAGE TYP (NO LOAD)**
- **HIGH FANOUT CAPABILITY – CAN DRIVE TWO 50 Ω LINES**
- **HIGH Z INPUTS – INTERNAL 50 kΩ PULLDOWNS**
- **HIGH IMMUNITY FROM POWER SUPPLY VARIATIONS: $V_{EE}$ = –5.2 V ±5% RECOMMENDED**
- **OPEN EMITTER LOGIC AND BUSSING CAPABILITY**

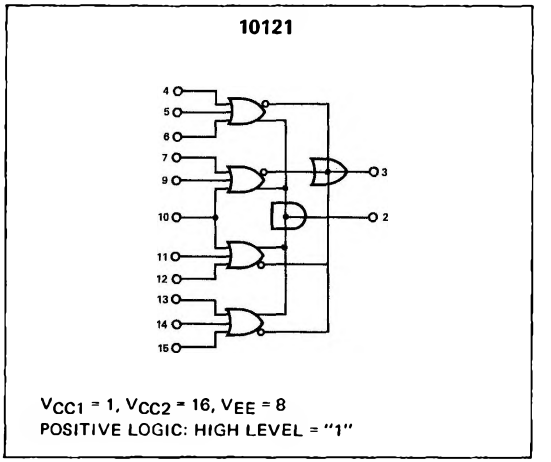
## EQUATIONS (Positive Logic)

$$2 = (4+5+6) \cdot (7+9+10) \cdot (10+11+12) \cdot (13+14+15)$$

$$3 = \overline{(4+5+6)} + \overline{(7+9+10)} + \overline{(10+11+12)} + \overline{(13+14+15)}$$

$$= \overline{(4+5+6) \cdot (7+9+10) \cdot (10+11+12) \cdot (13+14+15)}$$

## LOGIC DIAGRAM



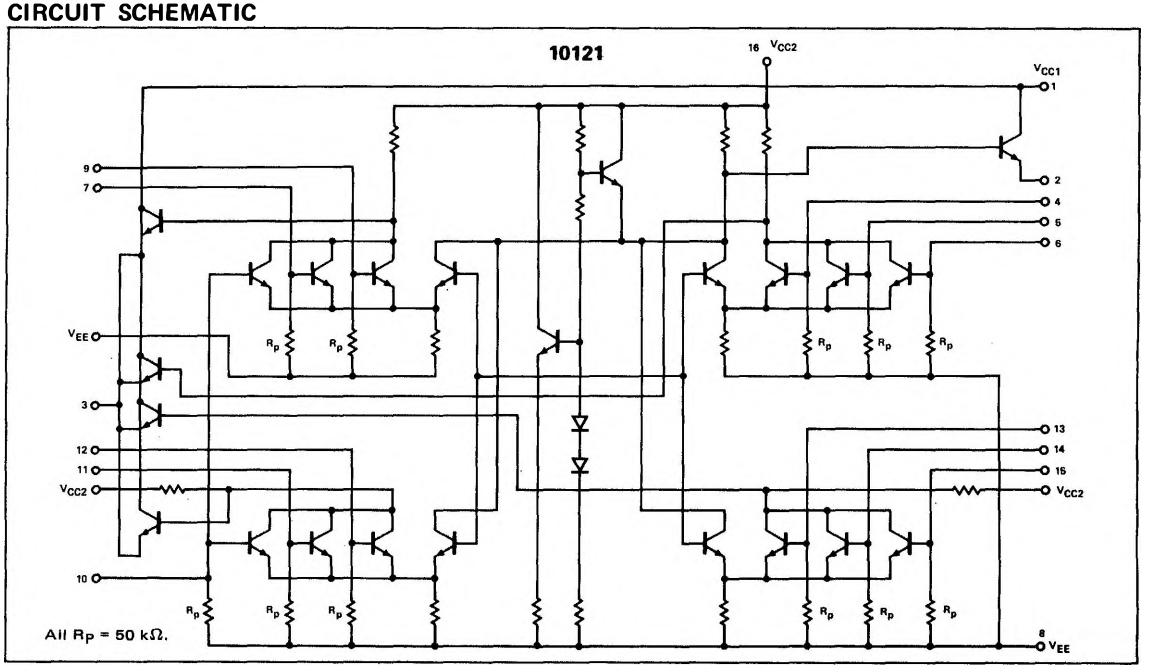

## TEMPERATURE RANGE

- –30 to +85°C Operating Ambient

## PACKAGE TYPE

B: 16-Pin Silicone DIP
F: 16-Pin CERDIP

## CIRCUIT SCHEMATIC



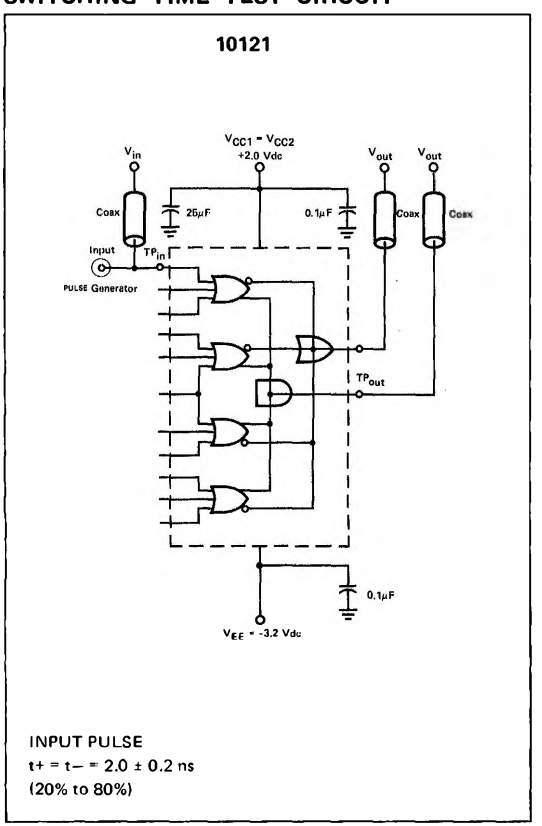
## ELECTRICAL CHARACTERISTICS
**(at Listed Voltage and Ambient Temperatures).**

| @ Test Temperature | TEST VOLTAGE VALUES (Volts) $V_{IH}$ max | $V_{IL}$ min | $V_{IHA}$ min | $V_{ILA}$ max | $V_{EE}$ |
|---|---|---|---|---|---|
| −30°C | −0.890 | −1.890 | −1.205 | −1.500 | −5.2 |
| +25°C | −0.810 | −1.850 | −1.105 | −1.475 | −5.2 |
| +85°C | −0.700 | −1.825 | −1.035 | −1.440 | −5.2 |

| Characteristic | Symbol | Pin Under Test | 10121 Test Limits −30°C Min | −30°C Max | +25°C Min | +25°C Typ | +25°C Max | +85°C Min | +85°C Max | Unit | TEST VOLTAGE APPLIED TO PINS LISTED BELOW: $V_{IH}$ max | $V_{IL}$ min | $V_{IHA}$ min | $V_{ILA}$ max | $V_{EE}$ | ($V_{CC}$) Gnd |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Power Supply Drain Current | $I_E$ | 8 | – | – | – | 20 | 26 | – | – | mAdc | – | – | – | – | 8 | 1,16 |
| Input Current | $I_{inH}$ | 7 | – | – | – | – | 265 | – | – | µAdc | 7 | – | – | – | 8 | 1,16 |
| | | 9 | – | – | – | – | 265 | – | – | ↓ | 9 | – | – | – | ↓ | ↓ |
| | | 10 | – | – | – | – | 370 | – | – | | 10 | – | – | – | | |
| | $I_{inL}$ | 7 | – | – | 0.5 | – | – | – | – | µAdc | – | 7 | – | – | 8 | 1,16 |
| | | 9 | – | – | ↓ | – | – | – | – | ↓ | – | 9 | – | – | ↓ | ↓ |
| | | 10 | – | – | – | – | – | – | – | | – | 10 | – | – | | |
| Logic "1" Output Voltage | $V_{OH}$ | 3 | −1.060 | −0.780 | −0.980 | – | −0.700 | −0.890 | −0.690 | Vdc | – | – | – | – | 8 | 1,16 |
| | | 2 | −1.060 | −0.890 | −0.960 | – | −0.810 | −0.890 | −0.700 | Vdc | 4,10,15 | – | – | – | 8 | 1,16 |
| Logic "0" Output Voltage | $V_{OL}$ | 3 | −1.890 | −1.675 | −1.850 | – | −1.650 | −1.825 | −1.615 | Vdc | 4,10,15 | – | – | – | 8 | 1,16 |
| | | 2 | −2.000 | −1.675 | −1.990 | – | −1.650 | −1.920 | −1.615 | Vdc | – | 4,10,15 | – | – | 8 | 1,16 |
| Logic "1" Threshold Voltage | $V_{OHA}$ | 3 | −1.080 | – | −0.980 | – | – | −0.910 | – | Vdc | 10,15 | – | – | 4 | 8 | 1,16 |
| | | 2 | −1.080 | – | −0.980 | – | – | −0.910 | – | Vdc | 10,15 | – | 4 | – | 8 | 1,16 |
| Logic "0" Threshold Voltage | $V_{OLA}$ | 3 | – | −1.655 | – | – | −1.630 | – | −1.595 | Vdc | 10,15 | – | 4 | – | 8 | 1,16 |
| | | 2 | – | −1.655 | – | – | −1.630 | – | −1.595 | Vdc | 10,15 | – | – | 4 | 8 | 1,16 |
| Switching Times * (50-ohm load) | | | | | | | | | | | +1.11 V | | Pulse In | Pulse Out | −3.2 V | +2.0 V |
| Propagation Delay | $t_{4+3-}$ | 3 | 1.4 | 3.9 | 1.4 | 2.3 | 3.4 | 1.4 | 3.8 | ns | 10,13 | – | 4 | 3 | 8 | 1,16 |
| | $t_{4-3+}$ | 3 | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | – | ↓ | 3 | ↓ | ↓ |
| | $t_{4+2+}$ | 2 | | | | | | | | | | – | | 2 | | |
| | $t_{4-2-}$ | 2 | | | | | | | | | | – | | 2 | | |
| Rise Time (20% to 80%) | $t_{3+}$ | 3 | 0.9 | 4.1 | 1.1 | 2.5 | 4.0 | 1.1 | 4.6 | | | – | | 3 | | |
| | $t_{2+}$ | 2 | | | | | | | | | | – | | 2 | | |
| Fall Time (20% to 80%) | $t_{3-}$ | 3 | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | | ↓ | – | ↓ | 3 | ↓ | ↓ |
| | $t_{2-}$ | 2 | | | | | | | | | | – | | 2 | | |

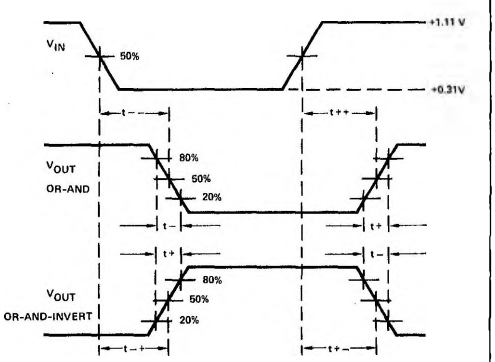
*Unused outputs connected to a 50-ohm resistor to ground.

## SWITCHING TIME TEST CIRCUIT




INPUT PULSE
t+ = t− = 2.0 ± 0.2 ns
(20% to 80%)

## PROPAGATION DELAY WAVEFORMS @ 25°C




NOTES:
1. Each ECL 10,000 series device has been designed to meet the DC specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Voltage levels will shift approximately 2 mV with an air flow of 200 linear fpm. Outputs are terminated through a 50-ohm resistor to 2.0 volts.
2. For AC tests, all input and output cables to the scope are equal lengths of 50-ohm coaxial cable. Wire length should be < 1/4 inch from $TP_{in}$ to input pin and $TP_{out}$ to output pin. A 50-ohm termination to ground is located in each scope input. Unused outputs are connected to a 50-ohm resistor to ground.
3. Test procedures are shown for only one input or set of input conditions. Other inputs are tested in the same manner.
4. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.