signetics

1 OF 8 DEMULTIPLEXER/DECODER (SELECTED OUTPUT IS HIGH) 10162

10162F: –30 to +85°C, CERDIP

DIGITAL 10,000 SERIES ECL

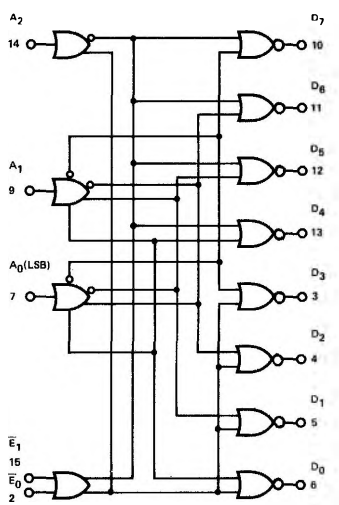
DESCRIPTION

The 10162 is a binary coded 3 line to 8 line decoder. Outputs are normally low with the selected output going high. Two enable inputs make it ideally suited for demultiplexer applications. One of the two enable inputs can be used as the data enable input. Either enable input when high, forces all outputs low.

The 10162 is a true parallel decoder using internal emitter dotting techniques. Hence it eliminates unequal delay times found in other decoders. The 10162 is a low power, high speed device with high Z input pulldown resistors and open emitter outputs.

LOGIC DIAGRAM

10162



(INTERNAL CONNECTIONS ARE EMITTER-DOT OR)

V_{CC1} = 1, V_{CC2} = 16, V_{EE} = 8
POSITIVE LOGIC: HIGH LEVEL = '1'

FEATURES

- FAST PROPAGATION DELAY
  = 4.0 ns TYP ADDRESS TO OUTPUT
  = 4.5 ns TYP ENABLE TO OUTPUT
- LOW POWER DISSIPATION = 295 mW/PACKAGE TYP (NO LOAD)
- HIGH FANOUT CAPABILITY – CAN DRIVE EIGHT 50 Ω LINES
- TRUE PARALLEL DECODER – ELIMINATES UNEQUAL DELAY TIMES
- HIGH IMMUNITY FROM POWER SUPPLY VARIATIONS: V_{EE} = –5.2 V ±5% RECOMMENDED
- HIGH Z INPUTS – INTERNAL 50 kΩ PULLDOWNS
- OPEN EMITTER OUTPUTS
- MEETS ECL 10,000 SERIES STANDARD INTERFACE SPECIFICATIONS

APPLICATIONS

- 1 of 8 Decoder
- 1 line to 8 line Demultiplexer

TRUTH TABLE

INPUTS					OUTPUTS							
$\overline{E1}$	$\overline{E0}$	A2	A1	A0	D0	D1	D2	D3	D4	D5	D6	D7
L	L	L	L	L	H	L	L	L	L	L	L	L
L	L	L	L	H	L	H	L	L	L	L	L	L
L	L	L	H	L	L	L	H	L	L	L	L	L
L	L	L	H	H	L	L	L	H	L	L	L	L
L	L	H	L	L	L	L	L	L	H	L	L	L
L	L	H	L	H	L	L	L	L	L	H	L	L
L	L	H	H	L	L	L	L	L	L	L	H	L
L	L	H	H	H	L	L	L	L	L	L	L	H
H	L	ϕ	ϕ	ϕ	L	L	L	L	L	L	L	L
L	H	ϕ	ϕ	ϕ	L	L	L	L	L	L	L	L
H	H	ϕ	ϕ	ϕ	L	L	L	L	L	L	L	L

ϕ = Don't Care.

TEMPERATURE RANGE

- –30 to +85°C Operating Ambient

PACKAGE TYPE

- F: 16-Pin CERDIP

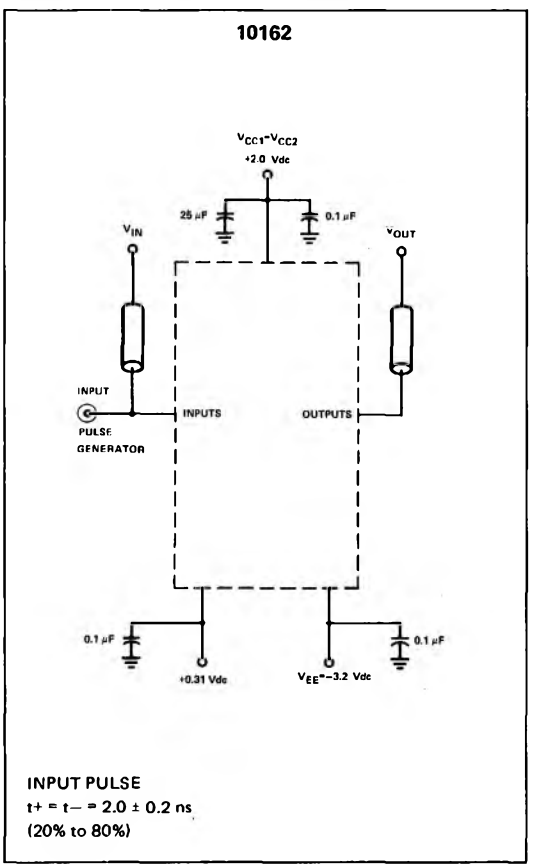
ELECTRICAL CHARACTERISTICS
(at Listed Voltages and Ambient Temperatures).

@ Test Temperature	TEST VOLTAGE VALUES (Volts) $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}
−30°C	0.890	−1.890	−1.205	−1.500	−5.2
+25°C	0.810	−1.850	−1.105	−1.475	−5.2
+85°C	0.700	−1.825	−1.035	−1.440	−5.2

Characteristic	Symbol	Pin Under Test	10162 Test Limits −30°C Min	−30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	–	–	57	72	–	–	mAdc	–	–	–	–	8	1,16
Input Current	I_{inH}	14	–	–	–	–	265	–	–	μAdc	14	–	–	–	8	1,16
	I_{inL}	14	–	–	0.5	–	–	–	–	μAdc	–	14	–	–	8	1,16
Logic "1" Output Voltage	V_{OH}	13	−1.060	−0.890	−0.960	–	−0.810	−0.890	−0.700	Vdc	14	–	–	–	8	1,16
Logic "0" Output Voltage	V_{OL}	13	−1.890	−1.675	−1.850	–	−1.650	−1.825	−1.615	Vdc	2	–	–	–	8	1,16
		13	−1.890	−1.675	−1.850	–	−1.650	−1.825	−1.615	Vdc	15	–	–	–	8	1,16
Logic "1" Threshold Voltage	V_{OHA}	13	−1.080	–	−0.980	–	–	−0.910	–	Vdc	–	–	14	–	8	1,16
Logic "0" Threshold Voltage	V_{OLA}	13	–	−1.655	–	–	−1.630	–	−1.595	Vdc	–	–	2	–	8	1,16
		13	–	1.655	–	–	−1.630	–	−1.595	Vdc	–	–	15	–	8	1,16
Switching Times * (50-ohm load)													Pulse In	Pulse Out	−3.2 V	+2.0 V
Propagation Delay	$t_{14+\ 13+}$	13	–	–	–	4.0	–	–	–	ns	–	–	14	13	8	1,16
	$t_{14-\ 13-}$	13	–	–	–	4.0	–	–	–	↓	–	–	↓	↓	↓	↓
Rise Time (20% to 80%)	t_+	13	–	–	–	2.0	–	–	–		–	–				
Fall Time (20% to 80%)	t_-	13	–	–	–	2.0	–	–	–		–	–				

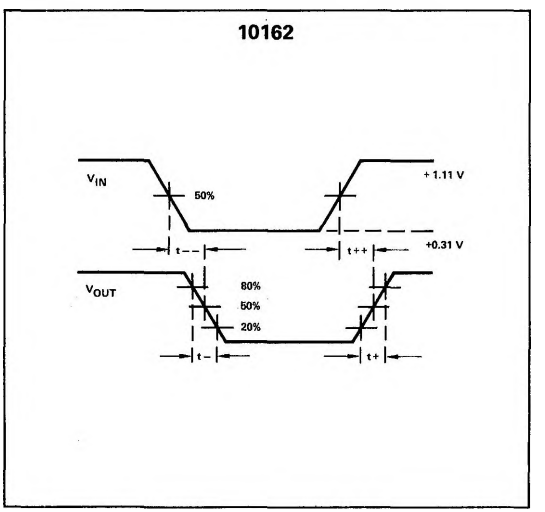
*Unused outputs connected to 50-ohm resistor to ground.

SWITCHING TIME TEST CIRCUIT



INPUT PULSE
$t_+ = t_- = 2.0 \pm 0.2$ ns
(20% to 80%)

PROPAGATION DELAY WAVEFORMS @ 25°C



NOTES:

1. Each ECL 10,000 series device has been designed to meet the DC specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 fpm is maintained. Voltage levels will shift approximately 5 mV with an air flow of 200 linear fpm. Outputs are terminated through a 50-ohm resistor to −2.0 volts.
2. For AC tests, all input and output cables to the scope are equal lengths of 50-ohm coaxial cable. Wire length should be < 1/4 inch from TP_{in} to input pin and TP_{out} to output pin. A 50-ohm termination to ground is located in each scope input. Unused outputs are connected to a 50-ohm resistor to ground.
3. Test procedures are shown for only one input or set of input conditions. Other inputs are tested in the same manner.
4. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.