signetics

QUAD 2 TO 1 MULTIPLEXER - LATCH 10173

10173F: –30 TO +85°C

DIGITAL 10,000 SERIES ECL

DESCRIPTION

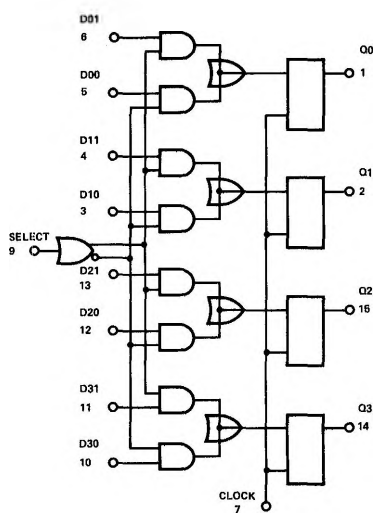
The 10173 is a quad clocked D-type latch with 2 to 1 data multiplexing.

Any change at the selected D input will be reflected at the output while the clock is low. The outputs are latched on the positive transition of the clock. While the clock is in the high state, a change in the information present at the data or select inputs will not affect the output information.

When the select input is false, the D_n0 inputs are selected and when select is true the D_n1 inputs are selected. As a quad 2-Input Multiplexer, with the added feature of a latch output, the 10173 provides the data select and store function in the same package. The result is a savings in system delay and package count.

LOGIC DIAGRAM

10173



V_{CC1} = 1, V_{CC2} = 16, V_{EE} = 8
POSITIVE LOGIC: HIGH LEVEL = '1'

FEATURES

- SIMULTANEOUS MULTIPLEXING AND LATCHING FUNCTION IMPROVES SYSTEM PERFORMANCE
- QUAD LATCH AND MULTIPLEXER ON ONE CHIP INCREASES SYSTEM DENSITY
- FAST PROPAGATION DELAY
  = 2.5 ns TYP (DATA TO OUTPUT)
  = 3.7 ns TYP (SELECT TO OUTPUT)
  = 4.3 ns TYP (CLOCK TO OUTPUT)
- LOW POWER DISSIPATION = 325 mW/PACKAGE TYP (NO LOAD)
- HIGH FANOUT CAPABILITY – CAN DRIVE 50 Ω LINES
- HIGH Z INPUTS – INTERNAL 50 kΩPULLDOWNS
- HIGH IMMUNITY FROM POWER SUPPLY VARIATIONS: V_{EE} = –5.2 V ±5% RECOMMENDED
- OPEN EMITTER OUTPUTS – ALLOW WIRE OR AND DATA BUSSING

APPLICATIONS

COMBINED MULTIPLEXER – REGISTER FOR:
- high speed central processors
- high speed peripherals
- high speed minicomputers
- communication systems
- instrumentation

TRUTH TABLE

D_n	C	Q_n (N + 1)
L	L	L
H	L	H
ϕ	H	Q_n (N)

$D_n = \overline{S} \cdot D_{n0} + S \cdot D_{n1}$
ϕ = Don't Care.

TEMPERATURE RANGE

- –30 to +85°C Operating Ambient

PACKAGE TYPE

- F: 16 Pin CERDIP

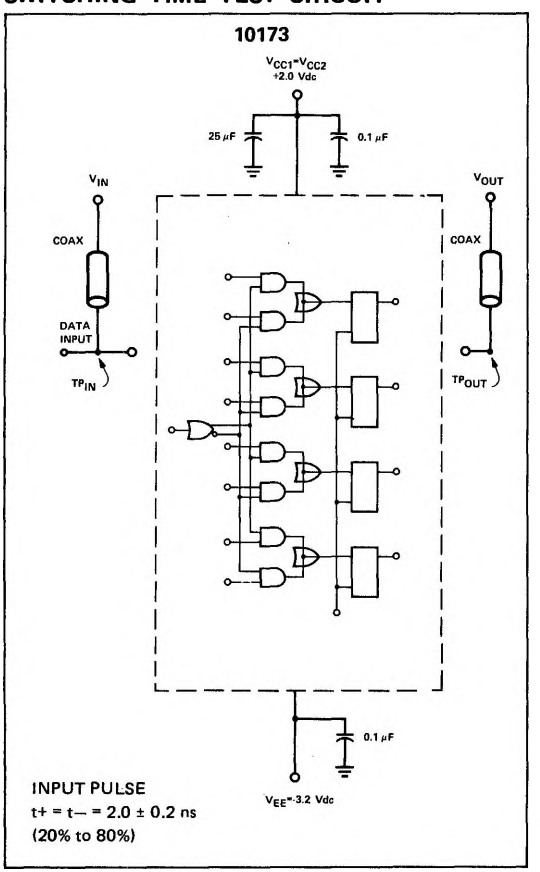
ELECTRICAL CHARACTERISTICS
(At Listed Voltages and Ambient Temperatures).

@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}
−30°C	−0.890	−1.890	−1.205	−1.500	−5.2
+25°C	−0.810	−1.850	−1.105	−1.475	−5.2
+85°C	−0.700	−1.825	−1.035	−1.440	−5.2

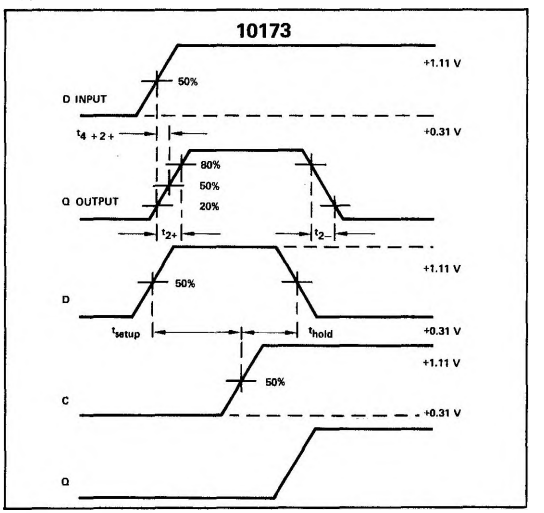
Characteristic	Symbol	Pin Under Test	10173 Test Limits −30°C Min	−30°C Max	+25°C Min	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}	Gnd
Power Supply Drain Current	I_E	8	–	–	–	78	–	–	mAdc	7,9	–	–	–	8	16
Input Current	$I_{in}H$	5	–	–	–	290	–	–	µAdc	5	–	–	–	8	16
		6	–	–	–	220	–	–		6	–	–	–		
		7	–	–	–	290	–	–		7	–	–	–		
		9	–	–	–	220	–	–		9	–	–	–		
	$I_{in}L$	4*	–	–	0.50	–	–	–	µAdc	–	4	–	–	8	16
Logic "1" Output Voltage	V_{OH}	2	−1.060	−0.890	−0.960	−0.810	−0.890	−0.700	Vdc	4	7,9	–	–	8	16
		2	−1.060	−0.890	−0.960	−0.810	−0.890	−0.700	Vdc	3,9	7	–	–	8	16
Logic "0" Output Voltage	V_{OL}	2	−1.890	−1.675	−1.850	−1.650	−1.825	−1.615	Vdc	–	4,7,9	–	–	8	16
		2	−1.890	1.675	−1.850	−1.650	−1.825	−1.615	Vdc	9	3,7	–	–	8	16
Logic "1" Threshold Voltage	V_{OHA}	2	−1.080	–	−0.980	–	−0.910	–	Vdc	–	7,9	4	–	8	16
		2	−1.080	–	0.980	–	−0.910	–	Vdc	9	7	3	–	8	16
Logic "0" Threshold Voltage	V_{OLA}	2	–	−1.655	–	−1.630	–	−1.595	Vdc	–	7,9	–	4	8	16
		2	–	−1.655	–	−1.630	–	−1.595	Vdc	9	7	–	3	8	16
Switching Times (50-ohm load) (See Figure 1)					Typ	Max				+1.11 V	+0.31 V	Pulse In	Pulse Out	−3.2 V	+2.0 V
Propagation Delay Data	t_{4+2+}	2	–	–	2.5	–	–	–	ns	9	7	4	2	8	16
Clock	t_{7-2+}		–	–	4.3	–	–	–		4,9	–	7			
Select	t_{9+2+}		–	–	3.7	–	–	–		4	7	9			
Setup Time Data	t_{setup}	2	–	–	1.5	–	–	–	ns	–	7,9	4	2	8	16
Select	t_{setup}	2	–	–	2.5	–	–	–	ns	3	7	9	2	8	16
Hold Time Data	t_{hold}	2	–	–	0.0	–	–	–	ns	–	7,9	4	2	8	16
Select	t_{hold}	2	–	–	−0.5	–	–	–	ns	3	7	9	2	8	16
Rise Time (20% to 80%)	t_{2+}	2	–	–	2.0	–	–	–	ns	–	7,9	4	2	8	16
Fall Time (20% to 80%)	t_{2-}	2	–	–	2.0	–	–	–	ns	–	7,9	4	2	8	16

*All other inputs tested in the same manner

SWITCHING TIME TEST CIRCUIT



PROPAGATION DELAY WAVEFORMS @ 25°C



NOTES:

1. Each ECL 10,000 series device has been designed to meet the DC specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 fpm is maintained. Voltage levels will shift approximately 6 mV with an air flow of 200 linear fpm. Outputs are terminated through a 50-ohm resistor to −2.0 volts.
2. For AC tests, all input and output cables to the scope are equal lengths of 50-ohm coaxial cable. Wire length should be < 1/4 inch from TP_{in} to input pin and TP_{out} to output pin. A 50-ohm termination to ground is located in each scope input. Unused outputs are connected to a 50-ohm resistor to ground.
3. Test procedures are shown for only one input or set of input conditions. Other inputs are tested in the same manner.
4. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.