DESCRIPTION

This family of Read/Write Random Access Memories is ideal for use in scratch pad and high-speed buffer memory applications.

These products are fully decoded memory arrays with separate input and output lines. They feature pnp inputs and 1 chip enable line for ease of memory expansion.

During Write, the outputs of each product assume a logic state by the output access time and the truth table.

The family is available in the commercial and military temperature ranges. For the commercial temperature range (0°C to +75°C) specify the N prefix, and for the military temperature range (-55°C to +125°C) specify the S prefix. The 54/74S89/189 military temperature range product is ordered as S54S89/189. The S grade product is supplied in the F package only.

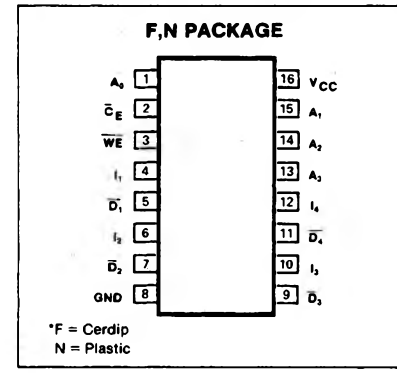
FEATURES

- **Output access time:**
  - **N82S25: 50ns**
  - **N3101A: 35ns**
  - **N54/74S89: 50ns**
  - **N54/74S189: 35ns**
- **Power dissipation: 6.25mW/bit, typ**
- **Input loading:**
  - **N grade: -100μA max**
  - **S grade: -150μA max**
- **On-chip address decoding**
- **Output options:**
  - **82S25: Open collector**
  - **3101A: Open collector**
  - **54/74S89: Open collector**
  - **54/74S189: Tri-state**
- **Schottky processed**
- **TTL compatible**

APPLICATIONS

- **Scratch pad memory**
- **Buffer memory**
- **Push down stacks**
- **Control store**

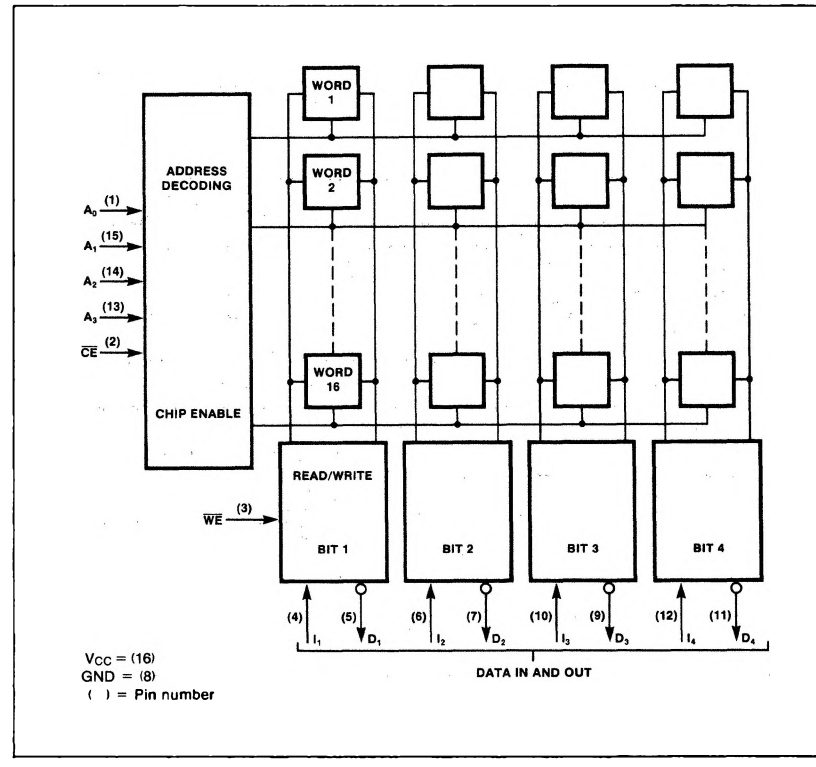
PIN CONFIGURATION



TRUTH TABLE

	$\overline{CE}$	$\overline{WE}$	D_{IN}	82S25	3101A	54/74S89	54/74S189
				DATA OUT			
Read	0	1	X	$\overline{\text{Stored data}}$	$\overline{\text{Stored data}}$	$\overline{\text{Stored data}}$	$\overline{\text{Stored data}}$
Write "0"	0	0	0	1	1	1	Hi-Z
Write "1"	0	0	1	1	1	0	Hi-Z
Disable	1	X	X	1	1	1	Hi-Z

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER[1]		RATING	UNIT
V_{CC}	Supply voltage	+7	Vdc
V_{IN}	Input voltage	+5.5	Vdc
	Output voltage		Vdc
V_{OH}	High	+5.5	
	Temperature range		°C
T_A	Operating		
	N grade	0 to +75	
	S grade	−55 to +125	
T_{STG}	Storage	−65 to +150	

DC ELECTRICAL CHARACTERISTICS

N grade: $0°C \le T_A \le +75°C$, $4.75V \le V_{CC} \le 5.25V$
S grade: $55°C \le T_A \le +125°C$, $4.5V \le V_{CC} \le 5.5V$

PARAMETER		TEST CONDITIONS	N GRADE			S GRADE			UNIT
			Min	Typ[2]	Max	Min	Typ[2]	Max	
	Input voltage								V
V_{IL}	Low	V_{CC} = Min			.85			.80	
V_{IH}	High	V_{CC} = Max	2.0			2.0			
V_{IC}	Clamp	I_{IN} = −12mA, V_{CC} = Min		−1.0	−1.5		−1.0	−1.5	
	Output voltage								V
V_{OL}	Low[3,4]	I_{OUT} = 16mA, V_{CC} = Min		0.35	0.45		0.35	0.5	
V_{OH}	High (54/74S189)	I_{OUT} = 2mA	2.4			2.4			
	Input current								μA
I_{IL}	Low	V_{IN} = 0.45V		−10	−100		−10	−150	
I_{IH}	High	V_{IN} = 5.5V			10			25	
	Output current								
I_{OLK}	Leakage	CE = high, V_{OUT} = 5.5V, V_{CC} = Min		<1	100		<1	100	μA
I_{OS}	Short circuit (54/74S189)	V_{OUT} = 0V		−30	−100	−30		−100	mA
$I_{O(OFF)}$	Hi-Z (54/74S189)	$2.4 \ge V_{OUT} \ge 0.4V$			±50			±50	μA
I_{CC}	Supply current[4]								mA
	82S25, 54/74S89			80	105		80	120	
	3101A			80	105		80	120	
	54/74S189			80	110		80	110	
	Capacitance	V_{CC} = 5.0V							pF
C_{IN}	Input	V_{IH} = 2.0V		5			5		
C_{OUT}	Output	V_{OUT} = 2.0V, CE = high		8			8		

AC ELECTRICAL CHARACTERISTICS

$R_1 = 270\Omega$, $R_2 = 600\Omega$, $C_L = 30pF$, See ac test load
N grade: $0°C \le T_A \le +75°C$, $4.75V \le V_{CC} \le 5.25V$
S grade: $-55°C \le T_A \le +125°C$, $4.5V \le V_{CC} \le 5.5V$

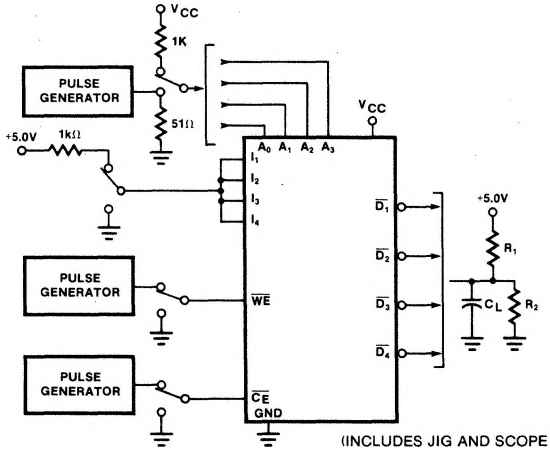
PARAMETER	TO	FROM	N82S25, N74S89			S82S25, S54S89			N3101A, N74S189			S3101A, S54S189			UNIT
			Min	Typ[2]	Max	Min	Typ[2]	Max	Min	Typ[2]	Max	Min	Typ[2]	Max	
Access time															ns
T_{AA} Address				35	50		35	60		25	35		25	50	
T_{CE} Chip enable				20	35		20	35		12	17		12	25	
T_{CD} Disable time	Output	Chip enable		20	35		20	35		12	17		12	25	ns
T_{WD} Response time	Output	Write enable		20	25		20	30		15	25		15	30	ns
T_{WR} Write recovery time				35	50		35	60		22	35		22	40	ns
Setup and hold time															ns
T_{WSA} Setup time	Write	Address	5	-8		10	-8		0			0			
T_{WHA} Hold time	enable		5	0		10	0		0			10			
T_{WSD} Setup time	Write	Data in	30	15		30	15		25			30			
T_{WHD} Hold time	enable		5	-3		10	-3		0			10			
T_{WSC} Setup time	Write	$\overline{CE}$	0	-5		0	-5		0			0			
T_{WHC} Hold time	enable		5	0		5	0		0			0			
Pulse width															ns
T_{WP} Write enable[5]			30	18		30	18		25			30	1		

NOTES

1. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
2. Typical values are at $V_{CC} = +5.0V$ and $T_A = +25°C$.
3. Output sink current is supplied through a resistor to V_{CC}.
4. All sense outputs in low state.
5. To guarantee a Write into the slowest bit.
6. Positive current is defined as into the terminal referenced.
7. Positive logic definition: high ≈ +5.0V, low ≈ GND.
8. Test each input one at a time.

TEST LOAD CIRCUIT

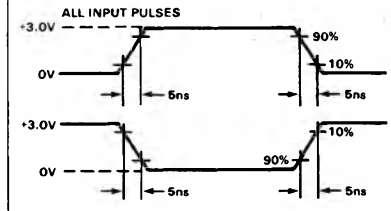
LOADING CONDITION



(INCLUDES JIG AND SCOPE CAPACITANCE)

VOLTAGE WAVEFORM

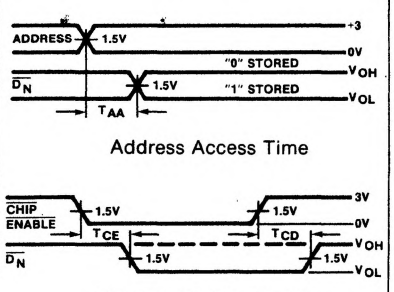
INPUT PULSES



Measurements: All circuit delays are measured at the +1.5V level of inputs and output.

TIMING DIAGRAMS

READ CYCLE



WRITE CYCLE