

3938

PRELIMINARY DATASHEET - 11/07/02

(Subject to change without notice)

THREE PHASE POWER MOSFET CONTROLLER

ABSOLUTE MAXIMUM RATINGS (at $T_A = +25^{\circ}\text{C}$)

Load Supply Voltage, V_{BB} 50 V
VREG (Transient) 15 V
Logic Input Voltage Range,
 V_{IN} -0.3 V to $V_{LCAP} + 0.3$ V
Sense Voltage, V_{SENSE} -5 to 1.5 V
Pins SA/SB/SC, -5 to 50 V
Pins GHA/GHB/GHC -5 to $V_{BB} + 17$ V
Pins CA/CB/CC SA/SB/SC+17 V

Operating Temperature Range,

T_A -20°C to +85°C
Junction Temperature, T_J +150°C
Storage Temperature Range,
 T_S -55°C to +150°C

Thermal Impedances, typ. ($T_A = +25^{\circ}\text{C}$)*

A3938SEQ, $R_{\theta JA}$ 37 °C/W
A3938KLQ, $R_{\theta JA}$ 44 °C/W

* JEDEC High K board.

The A3938 is a three-phase, brushless, DC-motor controller. The A3938's high current gate drive capability allows driving of a wide range of power MOSFETs and can support motor supply voltages to 50V. The A3938 integrates a bootstrapped high side driver to minimize the external component count required to drive N-channel MOSFET drivers.

Internal, fixed, off-time, PWM, current-control circuitry can be used to regulate the maximum load current to a desired value. The peak load current limit is set by the user's selection of an input reference voltage and external sensing resistor. A user-selected external RC timing network sets the fixed off-time pulse duration. For added flexibility, the PWM input can provide speed/torque control where the internal current control circuit sets a limit on the maximum current.

The A3938 includes Synchronous Rectification. This feature shorts out the current path through the power MOSFET's reverse body diodes during PWM off cycle current decay. This can minimize power dissipation in the MOSFETs, eliminate the need for external power clamp diodes, and potentially allow a more economical choice for the MOSFET drivers.

The A3938 provides commutation logic for Hall sensors configured for 120-degree spacing. The Hall input pins are pulled up to an internally generated 5V reference. Power MOSFET protection features includes bootstrap capacitor charging current monitor, regulator under-voltage monitor, motor lead short-to-ground, and thermal shutdown.

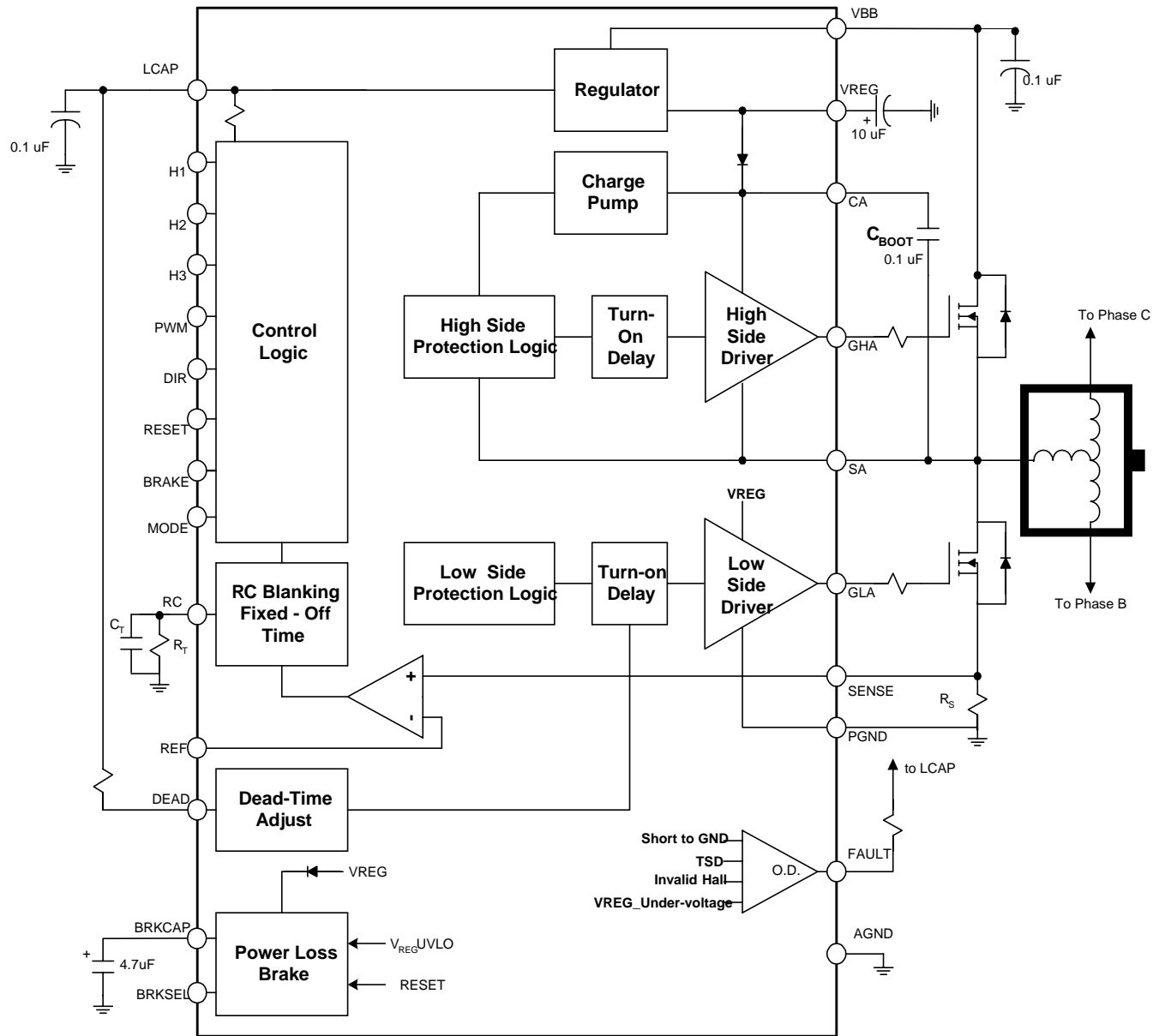
The A3938 is available in a choice of two packages: a 32-pin, rectangular PLCC suffix "EQ"; and 36-pin, QSOP, suffix "LQ".

FEATURES

- Drives Wide Range of N-channel MOSFETs
- Low-Side Synchronous Rectification
- Power MOSFET Protection
- Adjustable Dead-Time for Cross-Conduction Protection
- Selectable coast or dynamic brake on power-down or RESET input
- Fast/Slow Current Decay Modes
- Internal PWM Current Control
- Motor Lead Short-to-Ground Protection
- Internal 5V Regulator
- Fault Diagnostic Output
- Thermal Shutdown
- Under-voltage Protection

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Functional Block Diagram (1 of 3 outputs shown)



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Note: For 12V applications, VBB must be shorted to VREG. For this condition, the absolute max rating of 15V on VREG must be maintained to prevent damage to the 3938.

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ELECTRICAL CHARACTERISTICS: Unless noted, otherwise: $T_A = 25^\circ\text{C}$, $V_{bb} = 18$ to 50 V , C_{icap} , $C_{\text{boot}} = 0.1\ \mu\text{F}$, $C_{\text{vreg}} = 10\ \mu\text{F}$, $\text{PWM} = 22.5\ \text{kHz}$ sq. wave, two phases active. Typ. values for design use, only. Negative current flows out of designated pin.

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Quiescent Current	$I_{V_{BB}}$	RESET = 1, Coast mode, Stopped.			8.0	mA
LCAP Regulator	V_{LCAP}	$I_{\text{icap}} = -3.0\ \text{mA}$	4.75	5	5.25	V
VREG =VBB Supply Voltage Range	V_{REG}	VREG =VBB, observe max. rating = 15 V	10.8	–	13.2	V
VREG Output Voltage	V_{REG}	$V_{BB} = 13.2$ to $18\ \text{V}$, $I_{\text{vreg}} = -10\ \text{mA}$.		$V_{BB}-2.5$		V
		$V_{BB} = 18$ to 50V , $I_{\text{vreg}} = -10\ \text{mA}$.	12.4	13	13.6	V
VREG Load Regulation	$V_{REGLOAD}$	$I_{\text{vreg}} = -1$ to $-30\ \text{mA}$, Coast.		25		mV
VREG Line Regulation	V_{REGLIN}	$I_{\text{vreg}} = -10\ \text{mA}$, Coast.	–	40	–	mV

Control Logic

Logic Input Voltage	$V_{IN(1)}$	Minimum High Level for Logical (1)	2.0	–	–	V
	$V_{IN(0)}$	Maximum Low Level for Logical (0)	–	–	0.8	V
Logic Input Current	$I_{IN(1)}$	$V_{IN} = 2.0\ \text{V}$	-30		-90	μA
	$I_{IN(0)}$	$V_{IN} = 0.8\ \text{V}$	-50		-130	μA

Gate Drive

Low side drive, output high	V_{HGL}	$I_{gx} = 0$	$V_{REG}-.8$	$V_{REG}-.5$		V
High side drive, output high	V_{HGH}	$I_{gx} = 0$	10.4	11.6	12.8	V
Pull Up Switch Resistance	$R_{DS(ON)}$	$I_{gx} = -50\text{mA}$	–	14	–	Ω
Pull Down Switch Resistance	$R_{DS(ON)}$	$I_{gx} = 50\text{mA}$	–	4	–	Ω
Low side switching, 10/90 rise time	t_{rGL}	Load = 3300 pF	–	120	–	ns
Low side switching, 10/90 fall time	t_{fGL}	Load = 3300 pF	–	60	–	ns
High side switching, 10/90 rise time	t_{rGH}	Load = 3300 pF	–	120	–	ns
High side switching, 10/90 fall time	t_{fGH}	Load = 3300 pF	–	60	–	ns
Prop. Delay, GHx, GLx rising	T_{pr}	PWM to Gate Drive Out. Load = 3300 pF	-	220	-	nS
Prop. Delay, GHx, GLx falling	T_{pf}	PWM to Gate Drive Out. Load = 3300 pF	-	110	-	nS
Dead time, maximum	t_{DEAD}	$I_{DEAD} = 10\ \mu\text{A}$, GHx to GLx, Load =3300 pF.	–	5500	–	ns
Dead time, minimum	t_{DEAD}	$I_{DEAD} = 780\ \mu\text{A}$, GLx to GHx, Load =3300 pF.	–	100	–	ns

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Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Units
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Bootstrap Capacitor

Bootstrap Capacitor Voltage	V_{CAP}	$I_{CX} = 0$, $V_{SX} = 0$, $V_{REG} = 13$ V.	10.4	11.6	12.8	V
Bootstrap Capacitor R_{OUT}	R_{CAP}	$I_{CX} = -50$ mA		9	12	Ω
Charge Current	I_{CX}		100			mA

Current Limit Circuitry

Input Offset Voltage	V_{IO}	0 V < V_{cmr} < 1.5 V	-5	0	5	mV
Input Current , Sense pin	I_B	0 V < V_{cm} , V_{diff} < 1.5 V. [200K pull-up]		-25		μ A
Input Current , Ref. pin	I_B	0 V < V_{cm} , V_{diff} < 1.5 V		0		μ A
Blank Time	t_{BLANK}	$R=56k$, $C=470pf$.91		μ s
RC Charge Current	I_{RC}		-0.9	-1	-1.1	mA
RC Voltage Threshold	V_{RCL}		1.0	1.1	1.2	V
	V_{RCH}		2.7	3.0	3.3	V

Protection Circuitry

Bootstrap Charge Threshold	$I_{BOOTCHG}$	GHx turns ON, GLx turns OFF at $I_{BOOTCHG}$		-9		mA
Short to Ground, Drain-Source Monitor	$UVLO_{DS}$	$V_{BB} - V_{SX}$, High Side ON	1.3	2.0	2.7	V
VREG Under-voltage Threshold	$UVLO$	V_{REG} low to High	9.2	9.7	10.2	V
	$UVLO$	V_{REG} High to Low	8.6	9.1	9.6	V
Fault Output Voltage	V_{OUT}	$I_{OL} = 1$ mA			0.5	V
Brake Capacitor Supply Current	I_{BRAKE}	$V_{BB} = 8$ V, $BRKSEL = 1$		30		μ A
Low Side Gate Voltage	V_{GLBH}	$V_{BB}=0$, $BRKCAP = 8$ V		6.6		V
Thermal Shutdown Temp.	T_J		-	165	-	$^{\circ}$ C
Thermal Shutdown Hysteresis	ΔT_J		-	10	-	$^{\circ}$ C

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Pin Descriptions

RESET. A logic input that enables the device. Has internal 50K pull-up to LCAP. RESET=1 will coast or brake the motor depending on the state of the BRKSEL pin. RESET=0 will enable gate drive to follow commutation logic. RESET = 1 will override the BRAKE pin.

GLC/GLB/GLA. Low-side gate drive outputs for external MOSFET drivers. External series gate resistors can be used to control slew rate seen at the power driver gate, thereby, controlling the di/dt and dv/dt of S outputs.

SC/SB/SA. Directly connected to the motor terminals, these pins sense the voltages switched across the load. The pins are also connected to the negative side of the bootstrap capacitors and the negative supply connections for the floating high-side drivers.

GHC/GHB/GHA. High-side gate drive outputs for N-channel MOSFET drivers. External series gate resistors can be used to control slew rate seen at the power driver gate, thereby, controlling the di/dt and dv/dt of S outputs.

CC/CB/CA. High-side connections for bootstrap capacitors, positive supply for high-side gate drivers. The bootstrap capacitors are charged to approximately VREG when the output Sx terminals go low. When the output swings high, the voltage on these pins rise with the outputs to provide the boosted gate voltages needed for N-channel power MOSFETs.

MODE. Logic input to set current decay method. In response to PWM Off command: Slow Decay Mode (MODE=1) switches off the high-side FET, Fast Decay Mode (MODE=0) switches off the high-side and low-side FETs. Has internal, 50K pull-up to LCAP.

H1/H2/H3. Hall sensor inputs with internal, 50K pull-ups to LCAP. Configured for 120-degree electrical spacing.

DIR. Logic input to reverse rotation, see Commutation Logic Table. Has internal, 50K pull-up to LCAP.

FAULT. Open collector output to indicate fault condition. Will be pulled HIGH (usually by 5.1K external pull-up) for any of the following fault conditions:

- 1) Invalid HALL input code.
- 2) Under-voltage condition detected at VREG.
- 3) Thermal Shutdown.
- 4) Motor lead (SA/SB/SC) connected to ground.

Faults will force a COAST condition that turns all power MOSFETs off except a “Short-to-Ground” Fault that only turns off the high-side drivers. Only the “Short-to-Ground” Fault is latched but is cleared at each commutation. If the motor has stalled due to a short to ground being detected, toggling the RESET pin or repeating a power-up sequence will clear the fault.

BRAKE. Logic input for braking function. BRAKE=1 will turn on sink-side MOSFETs, turn off the source-side MOSFETs. This will effectively short the BEMF in the windings and brake the motor. Internal, 50K pull-up to LCAP. RESET=1 overrides this BRAKE pin. See BRKSEL.

BRKCAP. This pin is for connection of the reservoir capacitor used to provide positive power supply for the sink drive outputs for a power down condition. This will allow predictable braking, if desired. A 4.7 μ F capacitor will provide 6.5V gate drive for 300ms. If power down braking option is not needed (i.e., BRKSEL=0) then this pin should be tied to VREG.

BRKSEL. Logic input to enable/disable braking upon power down condition or RESET =1. Internal, 50K pull-up to LCAP. BRKSEL: 0 = Coast, 1 = Brake.

PWM. Speed control input. PWM=1 will turn on MOSFETs selected by Hall input logic. PWM=0 turns off the selected MOSFETs. The PWM input held high to utilize internal current control circuitry. Internal, 50K pull-up to LCAP.

RC. Analog input. Connection for R_T and C_T to set the fixed off-time. The C_T will also set the BLANK time. (see Applications Information). It is recommended that the fixed off-time should not be less than 10 μ S. The resistor should be in the range 10K to 500K.

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PIN DESCRIPTIONS (continued)

VREG. Regulated 13 V supply for low-side gate drive and bootstrap capacitor charge circuit. As a regulator, use 10 uF decoupling/storage capacitor (ESR < 1 ohm) from this pin to AGND, as close to the device pins as possible. Some auxiliary external load current may be drawn, if desired, depending on what is left over from that required by bridge FETs and PWM freq. Pin should be shorted to VBB for 12V applications.

V_{BB}. Motor power supply connection for A3938 and power MOSFETs. Pin should be shorted to VREG for 12V applications. It is good practice to connect a decoupling capacitor from this pin to AGND, as close to the device pins as possible.

REF. Analog input to current limit comparator. Voltage applied here sets the peak load current according to the equation: $I_{TRIP} = V_{REF}/R_{SENSE}$.

LCAP. 5V reference to power internal logic and low current for Dead-time pin and FAULT pin. Connection for **0.1 uF** external capacitor for decoupling.

DEAD. Analog input. A resistor between DEAD and LCAP is selected to adjust turn-off to turn-on time. This delay is needed to prevent cross-conduction in the external power FETs. The resistor allowable range is 5.6k to 470k, which converts to control logic dead-time of 100 nS to 5.5 uS.

$$T_{DEAD} \cong 11e-12 * (R_{DEAD} + 500)$$

Gate driver dead-times will depend on Gate Driver RC loading, as well.

SENSE. Analog input to the current limit comparator. Voltage representing load current appears on this pin. Voltage transients seen at this pin when the drivers turn on are ignored for time, T_{BLANK}.

AGND. Analog reference ground.

PGND. Return for low-side gate drivers. This should be connected to PCB power ground.

Commutation Truth Table

H1	H2	H3	DIR	GLA	GLB	GLC	GHA	GHB	GHC	SA	SB	SC
1	0	1	1	0	0	1	1	0	0	HI	Z	LO
1	0	0	1	0	0	1	0	1	0	Z	HI	LO
1	1	0	1	1	0	0	0	1	0	LO	HI	Z
0	1	0	1	1	0	0	0	0	1	LO	Z	HI
0	1	1	1	0	1	0	0	0	1	Z	LO	HI
0	0	1	1	0	1	0	1	0	0	HI	LO	Z
1	0	1	0	1	0	0	0	0	1	LO	Z	HI
1	0	0	0	0	1	0	0	0	1	Z	LO	HI
1	1	0	0	0	1	0	1	0	0	HI	LO	Z
0	1	0	0	0	0	1	1	0	0	HI	Z	LO
0	1	1	0	0	0	1	0	1	0	Z	HI	LO
0	0	1	0	1	0	0	0	1	0	LO	HI	Z

INPUT LOGIC

MODE	PWM	RESET	Quadrant	Mode of Operation
0	0	0	Fast decay	PWM chop – current decay with opposite of selected drivers ON
0	1	0	Fast Decay	Peak Current limit – selected drivers ON
1	0	0	Slow decay	PWM chop – current decay with both Low side drivers ON
1	1	0	Slow Decay	Peak Current limit – selected drivers ON
X	X	1	X	All gate drive outputs to 0V – Clear fault logic (BRKSEL=0)

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APPLICATION INFORMATION

Synchronous Rectification. To reduce power consumption in the external MOSFETs, the 3938 control logic will turn on the *appropriate low-side driver during the load current recirculation, PWM “off” cycle*. The reverse body diode of the power MOSFET will conduct only during the dead-time required at each PWM transition.

Dead Time. It is required to have a delay between a high or low-side turn off and the next turn on event to prevent cross-conduction. The potential for cross-conduction occurs with synchronous rectification, direction changes or PWM, and after a bootstrap capacitor charging cycle. This dead-time is set via a resistor from the DEAD pin to LCAP and can be varied from 100ns to 5.5us. The choice of power MOSFET and external gate resistance determines the selection of the dead-time resistor. The dead-time should be made long enough to cover the variation of the MOSFET capacitance and gate resistor (both external and internal to the 3938) tolerances.

Decoupling. The internal reference VREG supplies current for the gate drive circuit. As the gates are driven high they will require current from an external decoupling capacitor to support the transients. This capacitor should be placed as close as possible to the VREG pin. The value of the capacitor should be at least 20 times larger than the bootstrap capacitor. Additionally, a 1nF (or larger) ceramic monolithic capacitor should be connected between LCAP and AGND as close to the device pins as possible.

Protection Circuitry. The A3938 has several protection features

- 1) **Bootstrap Monitor.** The bootstrap capacitor is charged whenever a sink side FET is on, an Sx output goes low, or load current recirculates. This happens constantly during normal operation. The high side will not be allowed to turn on before the charging has decayed to less than approximately 9 mA.
- 2) **Undervoltage.** VREG supplies the low-side gate driver and the bootstrap charge current. It is critical to ensure that the voltages are at a proper level before enabling any of the outputs. The undervoltage circuit is active during power up and will signal a fault and coast the motor (all gate drives LOW) until VREG is greater than approximately 10V.
- 3) **Hall Invalid.** Illegal codes for the hall inputs (000/111) will force a fault and coast the motor. Noisy Hall lines may cause Hall code errors and, therefore, faults. Additional, external pull-up loading and filtering may be required in some systems. [Hint: Use dividers to the VREG, which has more current capability, than to the LCAP.]
- 4) **Thermal Shutdown.** Junction temperature greater than 165°C will signal a fault and coast the motor.
- 5) **Motor Lead.** The 3938 will signal a fault if the motor lead is shorted to ground. A short to ground is assumed after a high side is turned on and greater than 2V is measured between the drain (VBB) and source (SA/SB/SC) of the high-side power MOSFET. This fault is cleared at the beginning of each commutation. If a stalled motor results from a fault, the fault can only be cleared by toggling the RESET pin or by a power up sequence.

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Current Regulation. Load current can be regulated by an internal, fixed off-time, PWM control circuit. When the outputs of the MOSFETs are turned on, current increases in the motor winding until it reaches a value given by:

$$I_{TRIP} = V_{REF} / R_{SENSE}$$

At the trip point, the sense comparator resets the source enable latch, turning off the source driver. At this point, load inductance causes the current to recirculate for the fixed off-time period. The current path during recirculation is determined by the configuration of the MODE and SR input pins. The fixed off time is determined by an external resistor (R_T) and capacitor (C_T) connected in parallel from the RC terminal to AGND. The fixed off-time is approximated by:

$$t_{OFF} = R_T * C_T$$

T_{OFF} should be in the range 10 uS to 50 uS. Larger values for T_{OFF} could result in audible noise problems. For proper circuit operation, $10K < R_T < 500K$.

Torque control can be implemented by varying the REF input voltage as long as the PWM input stays high. If direct control of the torque/current is desired by PWM input, a voltage can be applied to the REF pin to set an absolute maximum current limit.

PWM Blank. The capacitor (C_T) also serves as the means to set the BLANK time duration. At the end of a PWM off cycle, a high-side gate selected by the commutation logic will turn on. At this time, large current transients can occur during the reverse recovery time (t_{rr}) of the intrinsic body diodes of the power MOSFETs. To prevent false tripping of the sense comparator, the BLANK function will disable the comparator for a time defined by:

$$T_{BLANK} = 1.9 * C_T / (1E-03 - [2/ R_T])$$

The user must ensure that the C_T is large enough to cover the current spike duration.

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Braking. The 3938 will dynamically brake the motor by forcing all low-side, power MOSFETs on, and all high-side, power MOSFETs off. This will effectively short-circuit the BEMF and brake the motor. During braking the load current can be approximated by:

$$I_{\text{BRAKEPEAK}} = V_{\text{BEMF}}/R_{\text{LOAD}}$$

As the current does not flow through the sense resistor during a dynamic brake, care should be taken to ensure that the power MOSFETs maximum ratings are not exceeded. [On its rising edge, the RESET =1 overrides the BRAKE input pin and latches the condition selected by the BRKSEL pin.]

Power Loss Brake. The BRKCAP and BRKSEL pins provide a power down braking option. By applying a logic level to input pin, BRKSEL, the system can determine if the motor will be dynamically braked or allowed to coast upon an under-voltage event on VREG or a RESET=1 rising edge. The reservoir capacitor on the BRKCAP pin provides the positive voltage that force the low-side gates of the power MOSFETs “high” keeping them ON, even after supply voltage is lost. Logic “1” to BRKSEL will brake the motor, logic “0” will coast it.

Brake Control

BRAKE	BRKSEL	Normal Operation	Power Loss Brake trigger event VREG Undervoltage or RESET = HIGH
0	0	Normal Run Mode	Coast – All gate drive outputs OFF
0	1	Normal Run Mode	Brake – All Low-Side Gate Driver ON
1	0	Brake – All Low-Side Gate Driver ON	Coast – All gate drive outputs OFF
1	1	Brake – All Low-Side Gate Driver ON	Brake – All Low-Side Gate Driver ON

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Terminal List

Pin Name	Pin Description	PLCC-32	36L QSOP
PGND	Low Side gate drive return	1	36
RESET	Control Input	2	1
GLC	Low Side C Gate Drive Output	3	2
SC	Motor Phase C Connection	4	3
GHC	High Side C Gate Drive Output	5	6
CC	Bootstrap Capacitor C	6	7
GLB	Low Side B Gate Drive Output	7	8
SB	Motor Phase C Connection	8	9
GHB	High Side B Gate Drive Output	9	10
CB	Bootstrap Capacitor B	10	11
GLA	Low Side A Gate Drive Output	11	12
SA	Motor Phase A Connection	12	13
GHA	High Side A Gate Drive Output	13	14
CA	Bootstrap Capacitor A	14	15
VREG	Gate Drive Supply	15	16
LCAP	5V Output	16	17
FAULT	Diagnostic Output	17	19
MODE	Control Input	18	20
VBB	Load Supply	19	21
H1	Hall Control Input	20	22
H3	Hall Control Input	21	24
H2	Hall Control Input	22	25
DIR	Control Input	23	26
BRAKE	Control Input	24	27
BRKCAP	Power Loss Brake Reservoir Capacitor Connection	25	28
BRKSEL	Control Input	26	29
PWM	Control Input	27	30
RC	Connection for fixed offtime R,C	28	31
SENSE	Sense resistor Connection	29	32
REF	Current Limit Adjust	30	33
DEAD	Deadtime Adjust Connection	31	34
AGND	Ground	32	35
N/C	Not Connected		4,5,18,23