

REFER TO PAGE 13 FOR Y PACKAGE PIN CONFIGURATION.

DIGITAL 8000 SERIES TTL/MSI

DESCRIPTION

The 8205 and 8204 are high performance bipolar ROM's incorporating the storage output or memory data register into the chip. Data is addressed by applying address information to the address lines. After valid data appears at the output of the memory array, (typically 35ns after the address is applied) and if the circuit is enabled, the strobe pulse will enter data into the 8 bit output latch register. A D-type latch (L) is used to enable the tri-state output drivers. If the circuit enable signals are valid, the strobe will set the latch. This turns on the output stage. The latch will remain set and keep the output enabled until the chip is disabled and the next strobe pulse occurs. If the strobe line is held high, the ROM will function in a conventional mode. The output will be controlled solely by the chip enable and the output latches will be bypassed.

See page 195 for ASCII (ADDRESS) to EBCDIC (DATA) and EBCDIC (ADDRESS) to ASCII (DATA) and 197/198 for ORDERING BLANKS.

FEATURES

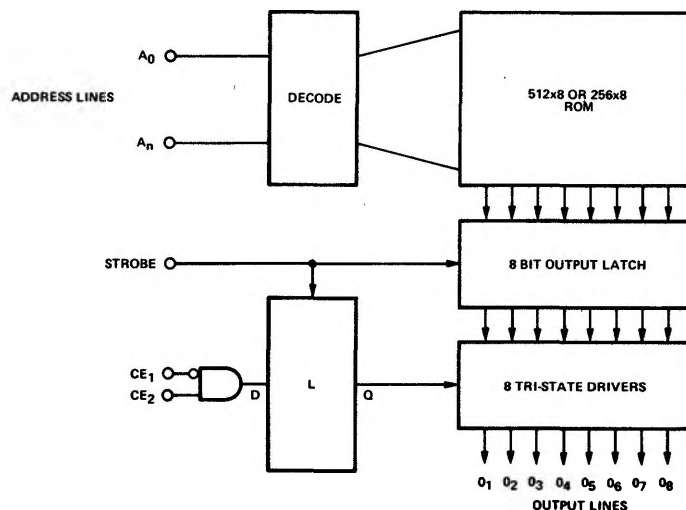
- MICROPROGRAMMING
- HARDWARE ALGORITHMS
- CHARACTER GENERATION
- CONTROL STORE

APPLICATIONS

- BUFFERED ADDRESS LINES
- ON THE CHIP DECODING
- ON THE CHIP STORAGE LATCHES
- TRI-STATE OUTPUT
- PROTECTED INPUTS

BLOCK DIAGRAM

256 x 8 AND 512 x 8 MEMORY ORGANIZATION



ELECTRICAL CHARACTERISTICS (Over Recommended Operating Temperature And Voltage)

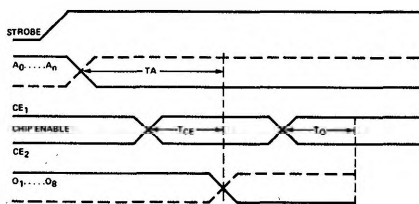
CHARACTERISTICS	LIMITS			UNIT	TEST CONDITIONS	NOTES
	MIN.	TYP.	MAX.			
Input '0' Current			-100	μA	$V_{in} = 0.45 V$	
Input '1' Current			25	μA	$V_{in} = 5.25 V$	
Input (0) Threshold Voltage	0.85			V		
Input (1) Threshold Voltage		2		V		
Input Clamp Voltage	-1.0			V	$I_{in} = -5.0 mA$	
Output (0)		0.2	0.45	V	$I_{out} = 9.6 mA$	
Output (1) Current	2.7	3.3		V	$I_{out} = -2.0 mA$	
Output (1) Short Circuit Current	-20	-35	-70	mA	$V_{out} = 0V, V_{CC} = 5.0V$	2
Input Capacitance		5		pF	$V_{IH} = 2.0V, V_{CC} = 5.0V$	
Output Capacitance		8		pF	$V_{out} = 2.0V, V_{CC} = 5.0V$	5
Power Supply Current		135	170	mA	$V_{CC} = 5.0V$	
Output (1) off Leakage Current (Chip Disabled)			100	μA	$V_{in} = 2.7V$	
Output (0) off Leakage Current (Chip Disabled)			-50	μA	$V_{in} = 0.45V$	

NOTES:

1. Positive current is defined as into the terminal referenced.
2. No more than one output should be grounded at the same time and strobe should be disabled. Strobe is in "1" state.
3. Manufacturer reserves the right to make design and process changes and improvements.
4. Applied voltages must not exceed 6.0V
Input currents must not exceed ±30 mA
Output currents must not exceed ±100 mA
Storage temperature must be between -60°C to +150°C.
5. Chip disabled

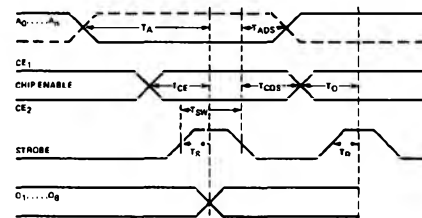
MEMORY TIMING

READ MODE I (OUTPUT LATCHES NOT USED)



If the strobe is high, the device functions in a manner identical to conventional bipolar ROM's. The timing diagram shows valid data will appear T_A nanoseconds after the address has changed and T_{CE} nanoseconds after the output circuit is enabled. T_O is the time required to disable the output and switch it to an 'off' or high impedance state after it has been enabled.

READ MODE II (OUTPUT LATCHES USED)



In Read Mode II, the address is applied to the memory element T_A ns before output details desired. Applying the chip enable does not directly enable the outputs. When the strobe is applied T_S nanoseconds before the output, data from the memory array is copied into the output latches and the chip enable signal is copied into the delay latch L. The latch L in turn enables the output. After the strobe reaches the strobe level, both the chip enable and address lines may be altered but the output data stored in the latches will remain unchanged and the output of the circuit will remain enabled. The output will stay enabled until another strobe copies a Not chipenable signal into the latch L. The switching of the output to the "off" or high impedance state occurs T_R nanoseconds after the strobe.