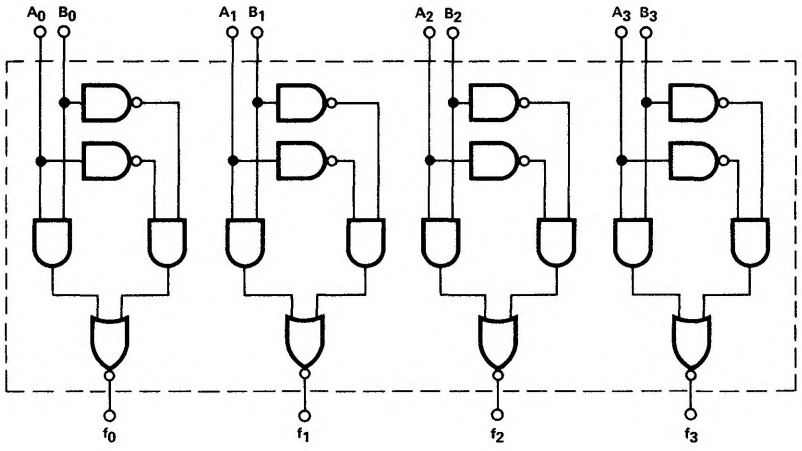
DESCRIPTION

The 8241 contains four independent gating structures to perform the Exclusive-OR function on two input variables. The output of the 8241 employs the totem-pole structure characteristic of TTL devices.

The 8242 contains four independent Exclusive-NOR gates which may be used to implement digital comparison functions. The 8242 outputs are bare collector to facilitate implementation of multiple-bit comparisons; a 4-bit comparison is made by connecting the outputs of the four independent gates together.

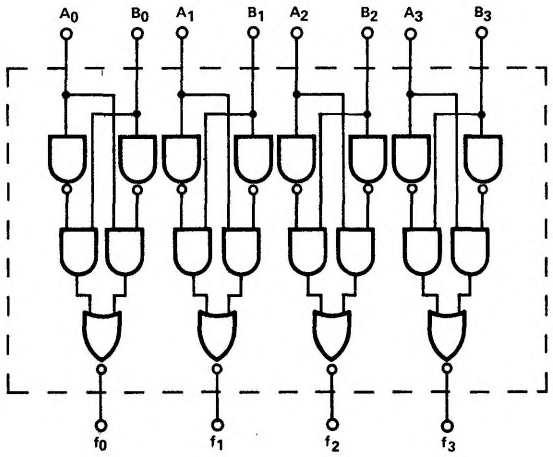
LOGIC DIAGRAMS AND TRUTH TABLES

8241 QUAD EXCLUSIVE – OR



A	B	f
0	0	0
1	0	1
0	1	1
1	1	0

8242 4-BIT DIGITAL COMPARATOR



A	B	f
0	0	1
1	0	0
0	1	0
1	1	1

ELECTRICAL CHARACTERISTICS (Over Recommended Operating Temperature And Voltage) (8241)

CHARACTERISTICS	LIMITS				TEST CONDITIONS			NOTES
	MIN.	TYP.	MAX.	UNITS	INPUTS A	INPUTS B	OUTPUTS	
Output "1" Voltage	2.6	3.5		V	2.0	0.8	800μA	7
Output "0" Voltage			0.4	V	2.0	2.0	16mA	8
Input "1" Current			80	μA	4.5	4.5V		13
Input "0" Current	-0.1		-3.2	mA	0.4	0.4		14
Power/Current Consumption		225/42.4	300/57.1	mW/mA				
Output Short Circuit Current	-20		-70	mA			0V	6
Input Latch Voltage								
A Input	5.5			V	10mA	0V		10
B Input	5.5			V	0V	10mA		10

$T_A = 25°C$ and $V_{CC} = 5.0V$ (8241)

CHARACTERISTICS	LIMITS				TEST CONDITIONS			NOTES
	MIN.	TYP.	MAX.	UNITS	INPUTS A	INPUTS B	OUTPUTS	
Propagation Delay		12	20	ns				9

ELECTRICAL CHARACTERISTICS (Over Recommended Operating Temperature And Voltage) (8242)

CHARACTERISTICS	LIMITS				TEST CONDITIONS			NOTES
	MIN.	TYP.	MAX.	UNITS	INPUTS A	INPUTS B	OUTPUT	
Output "1" Leakage Current			25	μA	2.0	2.0		12
Output "0" Voltage			0.4	V	2.0	0.8	25mA	8
Input "1" Current			80	μA	4.5	4.5V		13
Inpute "0" Current	-0.1		-3.2	mA	0.4	0.4		14
Power/Current Consumption		170/32	250/47.5	mW/mA	0.4	0.4		15
Input Latch Voltage								
A Input	5.5			V	10mA	0V		
B Input	5.5			V	0V	10mA		10

$T_A = 25°C$ and $V_{CC} = 5.0V$ (8242)

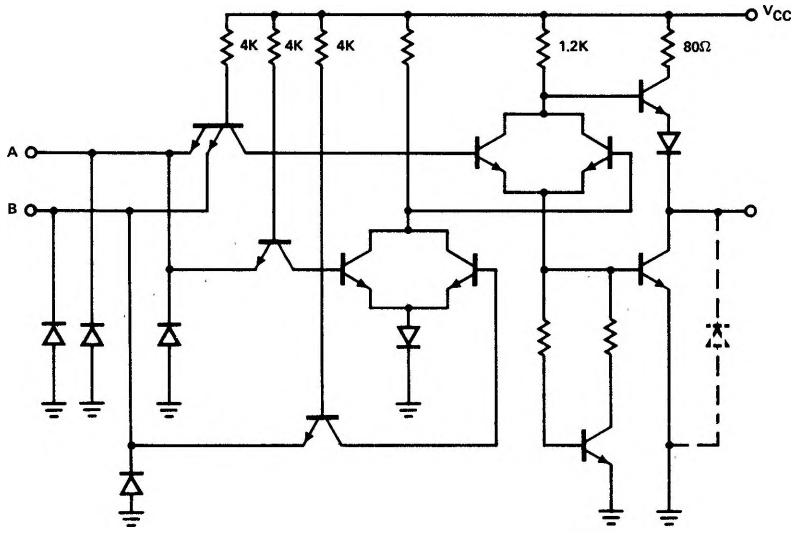
CHARACTERISTICS	LIMITS				TEST CONDITIONS			INPUTS
	MIN.	TYP.	MAX.	UNITS	INPUTS A	INPUTS B	OUTPUTS	
Propagation Delay		18	25	ns				9

NOTES:

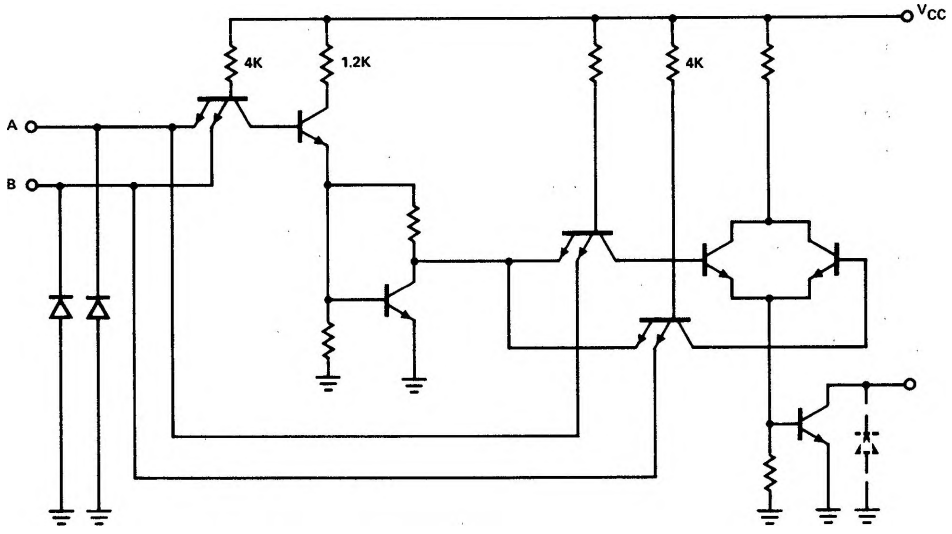
1. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
2. All measurements are taken with ground pin tied to zero volts.
3. Positive current flow is defined as into the terminal referenced.
4. Positive NAND logic definition: "UP" Level = "1", "DOWN" Level = "0".
5. Precautionary measures should be taken to ensure current limiting in accordance with Absolute Maximum Ratings should the isolation diodes become forward biased.
6. Measurements apply to each gate element independently.
7. Output source current is supplied through a resistor to ground.
8. Output sink current is supplied through a resistor to V_{CC}.
9. Refer to AC Test Figure.
10. This test guarantees operation free of input latch-up over the specified operating supply voltage range.
11. Manufacturers reserves the right to make design and process changes and improvements.
12. Connect an external 1K ±1% resistor from V_{CC} to the output terminal for this test.
13. A and B are tested separately. When A is 4.5V, B is 0V, and vice versa.
14. A and B are tested separately. When A is 0.4V, B is 5.25V, and vice versa.
15. V_{CC} = 5.25V.

SCHEMATIC DIAGRAMS

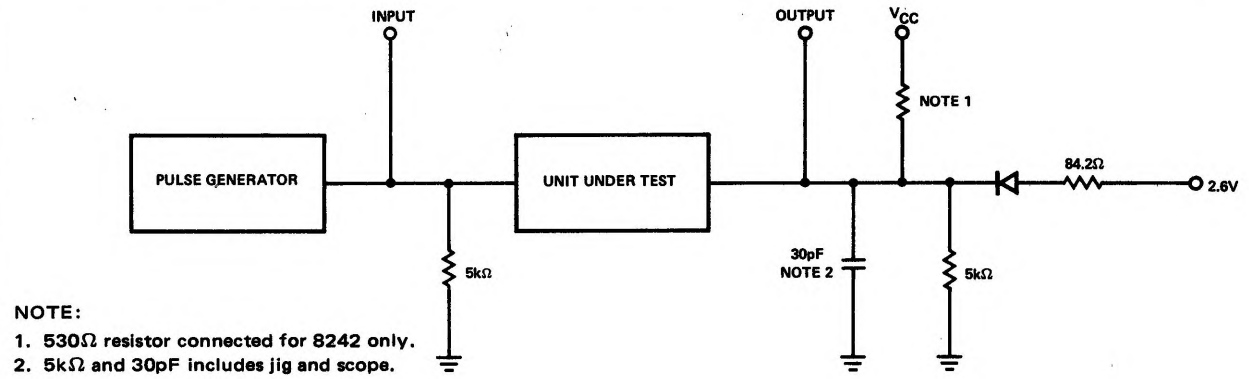
8241



8242

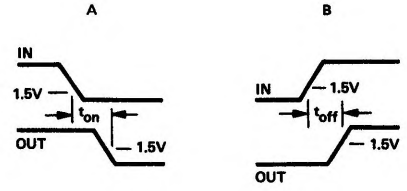


AC TEST FIGURE AND WAVEFORMS

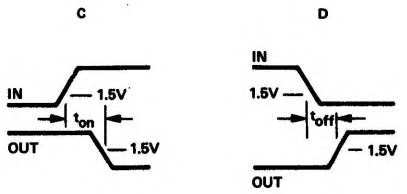


NOTE:
1. 530Ω resistor connected for 8242 only.
2. 5kΩ and 30pF includes jig and scope.

NON-INVERTING PATHS

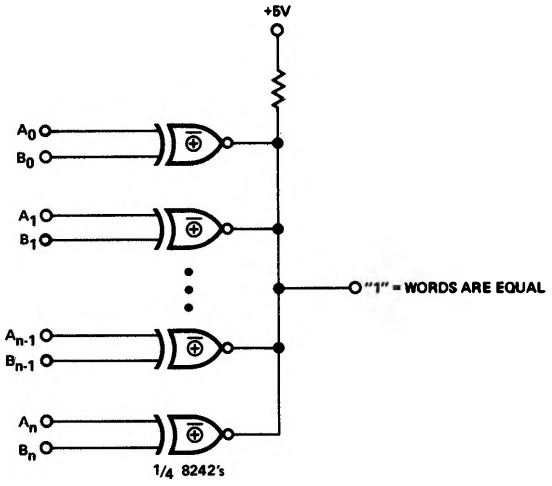


INVERTING PATHS



TYPICAL APPLICATIONS

EQUALITY GATE USED FOR COMPARISON



PARITY GENERATOR/TESTER