SONY

Transmission Digital Signal Processor IC for Infrared Spatial Digital Audio Communication

CXD4016R

Description

The CXD4016R is an IC that processes the transmitted digital signals used for infrared spatial digital audio communication (based on the IEC61603-8-1 standard) in consumer products. This IC contains the digital-to-analog converter (DAC) and a PLL circuit for RF signal. RF signal is processed by digital signal processing, so the operation is stable without any adjustments.

Features

- ◆ Performs all the transmitted digital signal processing on a single chip
- ◆ Supports the infrared spatial digital audio communication system formats for consumer uses
- ◆ Support the three audio sampling frequencies (32kHz, 44.1kHz, 48kHz)
- ◆ Direct output of RF signals enabled by on-chip DAC
- ◆ External RAM and PLL circuit not required

< Audio I/F Block >

- ◆ Interfaces for various audio ADCs

< Parity Generator Block >

- ◆ Automatic generation of Reed-Solomon parity for the infrared spatial digital audio communication system format

< Modulator Block >

- ◆ Digital processing throughout enables the transmitted RF signals in the infrared spatial digital audio communication system formats to be processed directly
- ◆ External analog circuit can be simplified by on-chip digital filter and on-chip DAC for RF signal applications
- ◆ Generation of subcarrier processed digitally

< Controller Block >

- ◆ Simple pin setting mode
- ◆ Serial interface provided by serial bus

< PLL Block >

- ◆ On-chip analog PLL circuit for generating the clock signals (640fs) required by the infrared spatial digital audio communication system formats

Package

64 pin LQFP (Plastic)

Structure

Silicon gate CMOS IC

Absolute Maximum Ratings

◆ Supply voltage	V_{DD}	– 0.5 to + 3.0	V
◆ Input voltage	V_I	– 0.5 to V_{DD} + 0.5 (≤ 3.0V)	V
◆ Output voltage	V_O	– 0.5 to V_{DD} + 0.5 (≤ 3.0V)	V
◆ Storage temperature	Tstg	– 55 to + 125	˚C

Recommended Operating Conditions

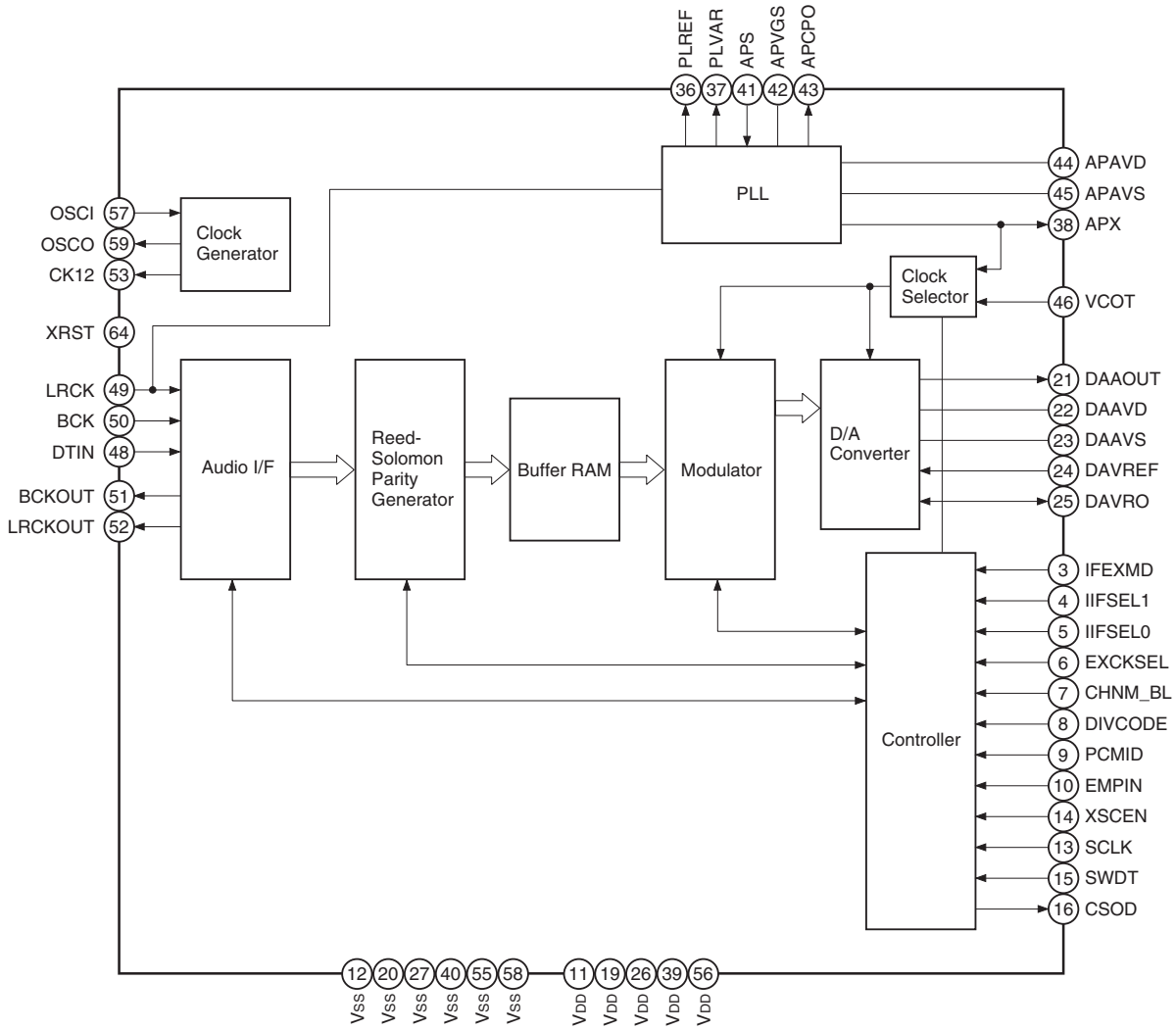
◆ Supply voltage	V_{DD}	2.5 ± 0.2	V
◆ D/A supply voltage	V_{DA}	2.5 ± 0.2	V
◆ PLL supply voltage	V_{PLL}	2.5 ± 0.2	V
◆ Operating temperature	Topr	– 40 to + 85	˚C
◆ Sampling frequency precision		Within ± 0.1%	

Input/Output Capacitance

◆ Input capacitance	C_{IN}	16 (max.)	pF
◆ Output capacitance	C_{OUT}	16 (max.)	pF
◆ Input/Output capacitance	$C_{I/O}$	16 (max.)	pF

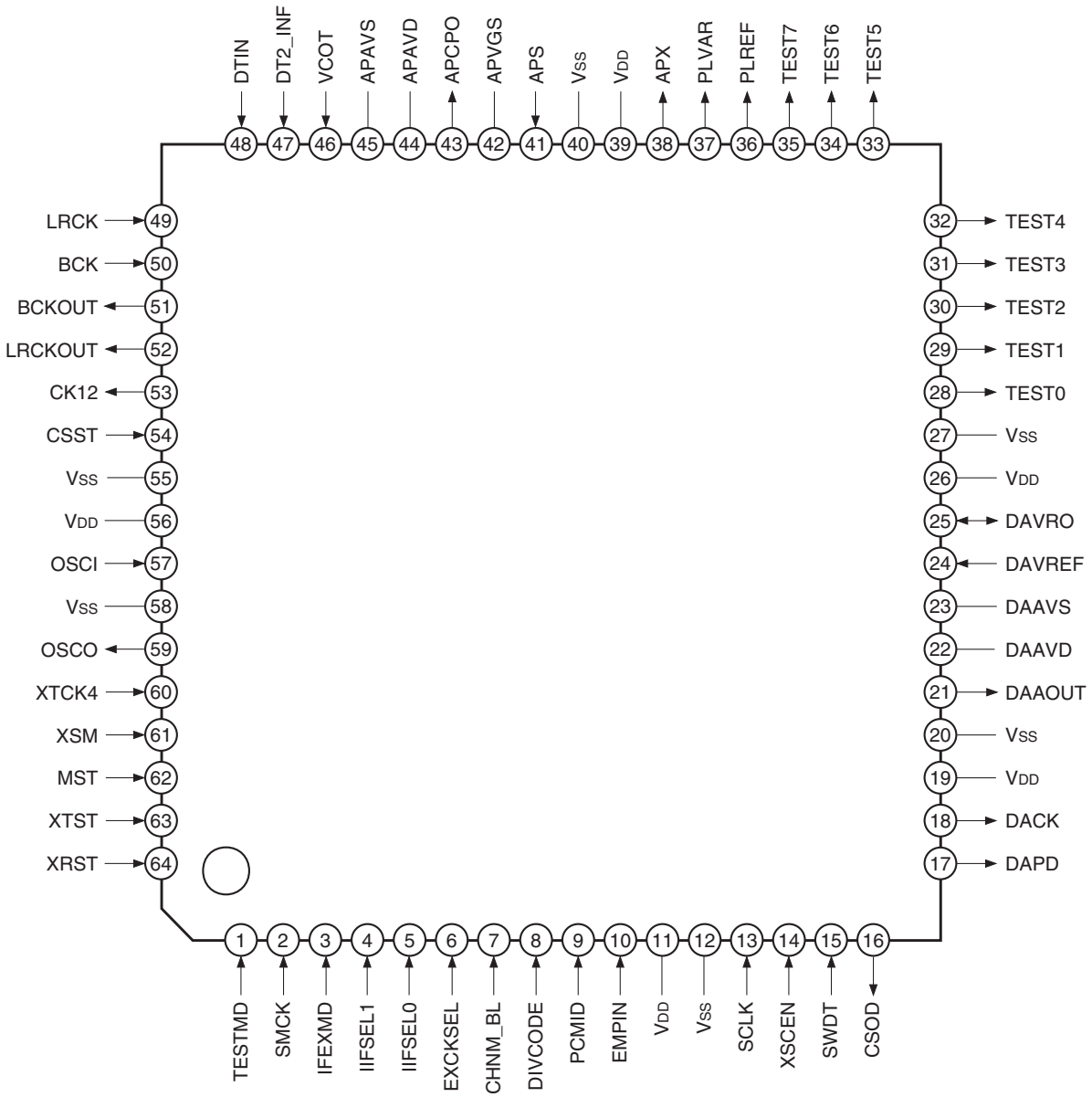
Note) Measurement conditions : Tj = 25˚C, V_{DD} = V_I = 0V, f = 1MHz

Block Diagram



* Test pins not shown.

Pin Configuration



Pin Description

Pin No.	Symbol	I/O	Description
1	TESTMD	I	Test mode selector, normally fixed “L”.
2	SMCK	I	SCAN test pin, normally fixed “H”.
3	IFEXMD	I	IIF extension mode. (L : Normal mode, H : Extension mode)
4	IIFSEL1	I	Audio input mode selection.
5	IIFSEL0	I	Audio input mode selection.
6	EXCKSEL	I	Clock selection for modulation. (L : APX internal connection, H : VCOT pin input)
7	CHNM_BL	I	Half-band : Channel number selection. (L : 0ch, H : 1ch) Full-band : Bit length control. (L : Full bit, H : 16-bit limited)
8	DIVCODE	I	Full/Half-band mode selection. (L : Full-band, H : Half-band)
9	PCMID	I	Source_info pcm_id input, normally fixed “L”. (L : PCM data)
10	EMPIN	I	Source_info emphasis input, (L : No emphasis, H : Emphasis)
11	V_{DD}	—	Digital power supply.
12	V_{SS}	—	Digital GND.
13	SCLK	I	Serial interface data clock input.
14	XSCEN	I	Serial interface enable input (negative logic).
15	SWDT	I	Serial interface data write input.
16	CSOD	O	Chapter start delay output.
17	DAPD	O	Test pin.
18	DACK	O	Test pin.
19	V_{DD}	—	Digital power supply.
20	V_{SS}	—	Digital GND.
21	DAAOUT	O	RF DAC output.
22	DAAVD	—	Analog power supply for RF DAC.
23	DAAVS	—	Analog GND for RF DAC.
24	DAVREF	I	RF DAC reference voltage input, apply 1.1V (typ.)
25	DAVRO	I/O	RF DAC internal current setting.
26	V_{DD}	—	Digital power supply.
27	V_{SS}	—	Digital GND.
28	TEST0	O	Test output pin.
29	TEST1	O	Test output pin.
30	TEST2	O	Test output pin.
31	TEST3	O	Test output pin.
32	TEST4	O	Test output pin.
33	TEST5	O	Test output pin.
34	TEST6	O	Test output pin.
35	TEST7	O	Test output pin.
36	PLREF	O	PLL reference output.

Pin No.	Symbol	I/O	Description
37	PLVAR	O	PLL frequency-divided output (APX output or VCOT input divided by 640).
38	APX	O	PLL VCO output, 640fs.
39	V_{DD}	—	Digital power supply.
40	V_{SS}	—	Digital GND.
41	APS	I	PLL reset pin.
42	APVGS	—	PLL guard band GND.
43	APCPO	O	PLL charge pump output.
44	APAVD	—	PLL power supply.
45	APAVS	—	PLL GND.
46	VCOT	I	External clock input for modulation.
47	DT2_INF	I	Test pin, normally fixed “L”.
48	DTIN	I	Audio data input.
49	LRCK	I	LR clock input.
50	BCK	I	Bit clock input.
51	BCKOUT	O	Bit clock output (3.072MHz).
52	LRCKOUT	O	LR clock output (48kHz).
53	CK12	O	Frequency-divided clock output for master clock (12.288MHz).
54	CSST	I	Test pin, normally fixed “L”.
55	V_{SS}	—	Digital GND.
56	V_{DD}	—	Digital power supply.
57	OSCI	I	Crystal oscillator circuit input for master clock (24.576MHz).
58	V_{SS}		Digital GND.
59	OSCO	O	Crystal oscillator circuit output for master clock (24.576MHz).
60	XTCK4	I	Test pin, normally fixed “L”.
61	XSM	I	Test pin for SCAN, normally fixed “H”.
62	MST	I	Test pin for SCAN, normally fixed “L”.
63	XTST	I	Test pin for SCAN, normally fixed “H”.
64	XRST	I	Asynchronous reset input. While power supply is “ON”, be sure to reset by fixing “L” after power supply is stabilized.

Electrical Characteristics

1. DC characteristics
(V_{DD} = 2.5 ± 0.2V, V_{SS} = 0V, Topr = – 40 to + 85℃)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit	Applicable pins
High level input voltage	V_{IH}		1.7	—	V_{DD} + 0.3	V	*1
Low level input voltage	V_{IL}		– 0.3	—	0.7		
High level output voltage	V_{OH}	I_{OH} = – 100μA	V_{DD} – 0.2	—	V_{DD}		*2
Low level output voltage	V_{OL}	I_{OL} = 100μA	0	—	0.2		
High level output current	I_{OH}	V_{OH} = V_{DD} – 0.4V	– 4.0	—	—	mA	*2
Low level output current	I_{OL}	V_{OL} = 0.4V	4.0	—	—		*2
Input leakage current	I_L		—	—	± 5	μA	*1
PLL supply voltage	V_{PLL}		2.3	2.5	2.7	V	*3
PLL charge pump output current	I_{CPO}			500		μA	*4
DAC supply voltage	V_{DA}		2.3	2.5	2.7	V	*5
DAC reference voltage	V_{REF}		1.05	1.10	1.15	V	*6
DAC full-scale adjusting resistor	R_{REF}	Between DAVRO and DAAVS	2.4	2.7		kΩ	*7
DAC output current	I_{DAC}	V_{REF} = 1.10V, R_{REF} = 2.7kΩ Full-scale Zero-scale LSB-scale	 4.67 0	 5.194 2 20.3	 5.71 20	 mA μA μA	*8
DAC load resistance	R_L	Between DAAOUT and DAAVS		150	160	Ω	*8
Supply current of digital block	I_{DD}	V_{DD} = 2.5V fs = 44.1kHz Full-band mode		12		mA	*9
Supply current of D/A block	I_{DA}	$V_{(DAAVD)}$ = 2.5V fs = 44.1kHz Full-band mode		6.5		mA	*5
Supply current of PLL block	I_{PLL}	$V_{(APAVD)}$ = 2.5V fs = 44.1kHz Full-band mode		3.5		mA	*3

Applicable pins

*1 TESTMD, SMCK, IFEXMD, IIFSEL1, IIFSEL0, EXCKSEL, CHNM_BL, DIVCODE, PCMID, EMPIN, SCLK, XSCEN, SWDT, APS, VCOT, DT2_INF, DTIN, LRCK, BCK, CSST, XTCK4, XSM, MST, XTST, XRST

*2 CSOD, DAPD, DACK, TEST0, TEST1, TEST2, TEST3, TEST4, TEST5, TEST6, TEST7, PLREF, PLVAR, APX, BCKOUT, LRCKOUT, CK12

*3 APAVD

*4 APCPO

*5 DAAVD

*6 DAVREF

*7 DAVRO

*8 DAAOUT

*9 V_{DD} (Pins 11, 19, 26, 39, 56)

2. AC characteristics

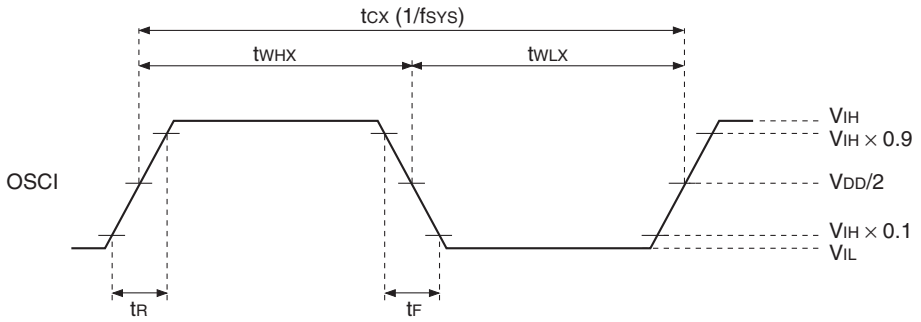
(1) OSCI, OSCO pins

(a) When using self-excited oscillation
(V_{DD} = 2.5 ± 0.2V, V_{SS} = 0V, Topr = – 40 to + 85℃)

Item	Symbol	Min.	Typ.	Max.	Unit
Oscillation frequency	f_{SYS}	—	24.576	—	MHz

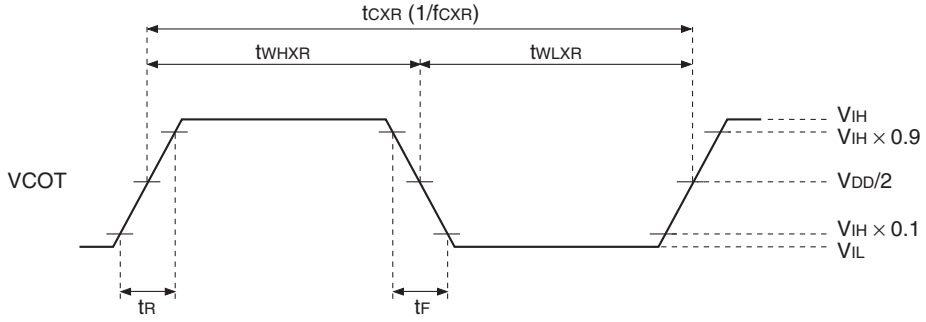
(b) When inputting pulses to OSCI
(V_{DD} = 2.5 ± 0.2V, V_{SS} = 0V, Topr = – 40 to + 85℃)

Item	Symbol	Min.	Typ.	Max.	Unit
Pulse frequency	f_{SYS}	24.330	24.576	24.600	MHz
High level pulse width	t_{WHX}	—	20.345	—	ns
Low level pulse width	t_{WLX}	—	20.345	—	ns
Rise time/fall time	t_R, t_F			2	ns



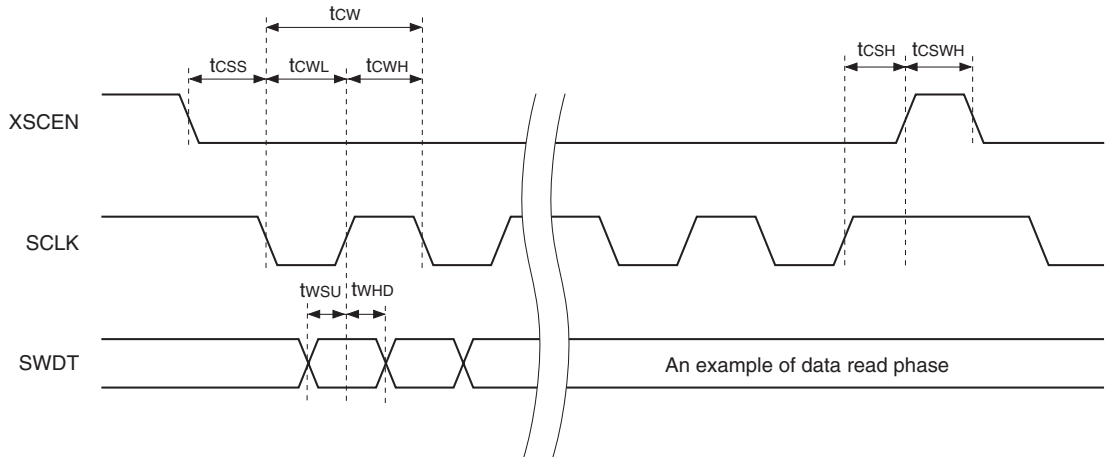
(2) VCOT pin
(V_{DD} = 2.5 ± 0.2V, V_{SS} = 0V, Topr = – 40 to + 85℃)

Item	Symbol	Min.	Typ.	Max.	Unit
Pulse frequency	f_{CXR}	20.275	—	31.027	MHz
High level pulse width	t_{WHXS}	0.45 × t_{CXR}	—	0.55 × t_{CXR}	ns
Low level pulse width	t_{WLXR}	0.45 × t_{CXR}	—	0.55 × t_{CXR}	ns



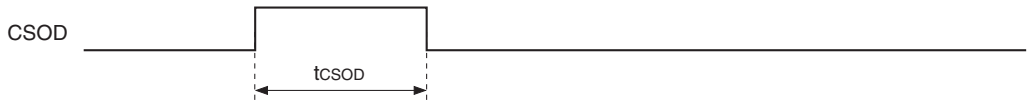
(3) SCLK, XSCEN, SWDT, SRDT pins
(V_{DD} = 2.5 ± 0.2V, V_{SS} = 0V, Topr = – 40 to + 85°C)

Item	Symbol	Min.	Typ.	Max.	Unit
Clock period	t_{CW}	200	—	—	ns
Clock pulse width, high	t_{CWH}	100	—	—	ns
Clock pulse width, low	t_{CWL}	100	—	—	ns
Enable signal pulse width	t_{CSWH}	170	—	—	ns
Enable signal setup time	t_{CSS}	0	—	—	ns
Enable signal hold time	t_{CSH}	100	—	—	ns
SWDT Setup time	t_{WSU}	20	—	—	ns
SWDT Hold time	t_{WHD}	100	—	—	ns



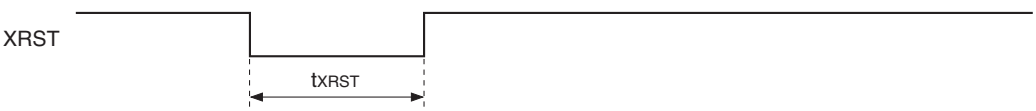
(4) CSOD pin
(V_{DD} = 2.5 ± 0.2V, V_{SS} = 0V, Topr = – 40 to + 85°C)

Item	Symbol	Min.	Typ.	Max.	Unit
CSOD pulse width	t_{CSOD}	260	—	—	µs



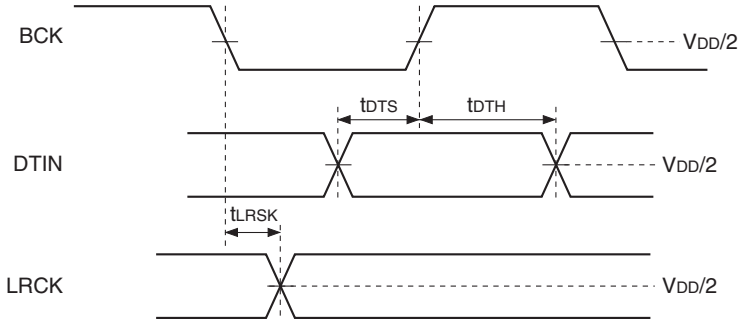
(5) XRST pin
(V_{DD} = 2.5 ± 0.2V, V_{SS} = 0V, Topr = – 40 to + 85°C)

Item	Symbol	Min.	Typ.	Max.	Unit
XRST pulse width	t_{XRST}	100.0	—	—	ns



(6) BCK, DTIN, LRCK pins
(V_{DD} = 2.5 ± 0.2V, V_{SS} = 0V, Topr = – 40 to + 85°C)

Item	Symbol	Min.	Typ.	Max.	Unit
DTIN setup time	t_{DTS}	10	—	—	ns
DTIN hold time	t_{DTH}	100	—	—	ns
LRCK skew time	t_{LRSK}	—	—	± 20	ns



Description of Functions

Description of clock generator

1. This LSI chip can generate the system clock pulse by connecting a 24.576MHz crystal oscillator to the OSCI pin and OSCO pin. Also, it incorporates 1MΩ (typ.) feedback resistor between the OSCI and OSCO pins.
2. It functions as the system clock by inputting a 24.576MHz external oscillation clock pulse to the OSCI pin while keeping the OSCO pin open.
3. Please keep the frequency precision for system clock within 24.576MHz ± 100ppm.

Description of PLL circuit

1. In addition to supplying the system clock pulse using the OSCI pin, this LSI requires the modulation clock pulse which is provided by the PLL circuit. The PLL circuit provided on the LSI chip can be used for this purpose.
2. If the sampling frequency of the digital audio input signals is fs, then the modulation clock pulse provided by the PLL circuit has a frequency of 640fs.
3. When the PLL circuit on the LSI is used, input a low level to the EXCKSEL pin and VCOT pin. Furthermore, an external lag-lead filter must be connected to the LSI for the charge pump current output APCPO pin of the PLL circuit. Ensure that the wiring involved is kept as short as possible.
4. When the PLL circuit on the LSI is not used, the LSI chip must be provided with an external PLL circuit. Input a high level to the EXCKSEL pin and the modulation clock pulse to the VCOT pin. The reference signal of the PLL circuit for generating the clock pulses is output to the PLREF pin, and its frequency is set to fs. At this time, the frequency of the clock pulse which has been input to the VCOT pin is divided by 640 inside the LSI, and the pulse with the resulting frequency is output to the PLVAR pin.

Pin setting/serial data interface

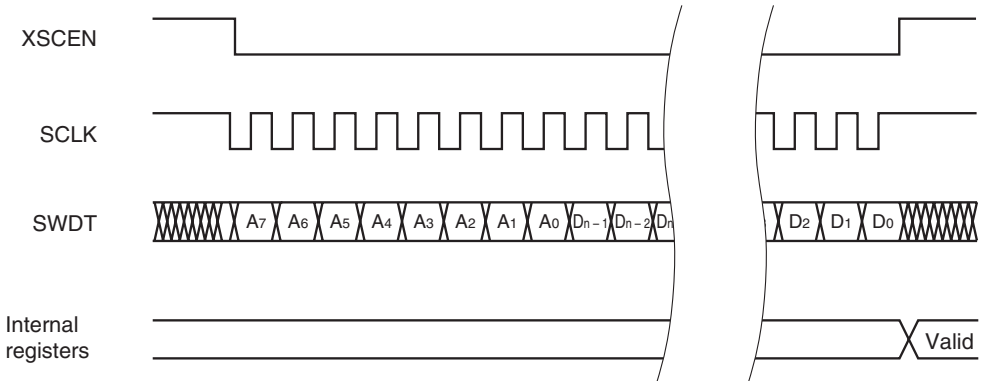
The setting modes of this LSI can be broadly classified into two : the pin setting mode and the serial data interface mode. By setting serial data interface mode, switching between pin setting mode and serial data interface mode is enabled. For example, setting SCEN01 bit to “0” validate pin setting mode and setting it to “1” validate serial data interface setting mode during Address 01 in serial data interface mode. (See “(3) Serial setting command table” on the next page.) Followings are pins which can be set even in the serial data interface mode.

EXCKSEL pin, DIVCODE pin, CHNM_BL pin, IFEXMD pin, IIFSEL1 pin, IIFSEL0 pin, PCMID pin, EMPIN pin.

Description of serial data interface

1. Serial data interface timings
   This LSI enables the various LSI operations to be changed by the SCLK pin, SWDT pin and XSCEN pin. The interface timing chart for each code group is presented below. Also, the SCLK pin should not be used with other devices. Normal communication cannot be performed.

2. XRST pin
   All the internal registers are initialized to “Default value” presented in the “Serial data interface setting command table” when reset by setting the XRST pin to low.



3. Method for disabling the CXD4016R's FSLOCK signal
   The LRCK input to the CXD4016R must be a stable clock with no jitter. A PLL that uses LRCK as the reference is formed inside the CXD4016R, and this PLL generates a 640fs clock. However, the signal (FSLOCK) that indicates the PLL lock status is generated inside this LSI, and RF generation is temporarily stopped when the lock is lost. This lock detection logic has strict conditions, so if the LRCK jitter is large, the jitter of the clock generated by the PLL is also large, and the lock may be judged as lost.
   Using a LRCK with large jitter is not recommended, but when a LRCK with large jitter must be used, this LSI has a test mode that can reduce the RF generation stoppage frequency by disabling the FSLOCK signal as follows.
   FSLOCK can be enabled or disabled by sending the command indicated in the Serial Setting Command Table. At the default setting, FSLOCK operates according to the lock detection logic.
   To forcibly set the FSLOCK status, send address 71h and data 0Fh by the serial setting command.
   In addition, to return to the default setting, send address 71h and data 03h by the serial setting command. Performing this process is highly recommended.

4. Serial setting command table

Address (HEX)	Default value	Length [bit]	Signal name	Signal length [bit]	Value	Effect
01h	00h	8	SCEN01	1	0 1	Invalidate serial setting of Address 01. Validate serial setting of Address 01.
			EXCKSEL	1	0 1	APX internal connection. VCOT pin input.
			DIVCODE	1	0 1	Full-band mode. Half-band mode.
			CHNM_BL	1	0 1	0ch/full-bit. 1ch/16-bit limited.
			IFEXMD	1	0 1	Normal mode. Extension mode.
			IIFSEL1	1	—	Audio input interface mode select 1.
			IIFSEL0	1	—	Audio input interface mode select 0.
			res.	1	0	Be sure to set the value to “0”.
02h	40h	8	SCEN02	1	0 1	Invalidate serial setting mode of Address 02. Validate serial setting mode of Address 02.
			CRC_FLG	1	0 1	CRC off. CRC on (default).
			VALID_FLG	1	0 1	Source_block is error free. Source_block contains some errors.
			PCM_ID	1	0 1	Data is Linear PCM. Data is used for other purposes.
			CPRGT_FLG	1	0 1	Copyright is asserted. No copyright is asserted.
			EMPHASIS	1	0 1	No emphasis. Emphasis.
			res.	2	00	Reserved.
03h	69h	8	CATEGORY	8	—	Source_info Byte 3 category codes.
71h	03h	8	res.	4	0000	Be sure to set the value to “0000”.
			FSLOCK_EN	1	0 1	Invalidate serial setting mode of FSLOCK. Validate serial setting mode of FSLOCK.
			FSLOCK	1	0 1	Set to unlocked logic forcibly. Set to locked logic forcibly.
			res.	2	11	Be sure to set the value to “11”.

Description of audio I/F

1. As shown below, the audio ADC can be directly coupled in this LSI.

   DTIN : Connect the data output from ADC

   BCK : Connect the bit clock output from ADC (64fs)

   LRCK : Connect the sample clock output from ADC (fs)

   The sampling frequencies (fs) which can correspond to this LSI are 32kHz, 44.1kHz, 48kHz. Also, the precision of fs is within ± 1000ppm. If it gets beyond this range even for a second, the normal operation might not be performed. So care should be taken.

2. This LSI has the LRCKOUT pin, BCKOUT pin and CK12 pin in order to use the audio ADC into which sample clock and bit clock are required to be input.

   LRCKOUT pin : sample clock (48kHz)

   BCKOUT pin : bit clock (48kHz × 64)

   CK12 pin : master clock (12.288MHz (48kHz × 256))

   Connect the LRCKOUT pin to the sample clock of ADC and the LRCK pin of this LSI. And connect the BCKOUT pin to the bit clock pin of ADC and the BCK pin of this LSI.

3. Sixty-four BCK cycles are contained in one LRCK cycle.

4. The DTIN input format can be changed by the setting of resistor with address 01h, or the IFEXMD pin, IIFSEL1 pin and IIFSEL0 pin.

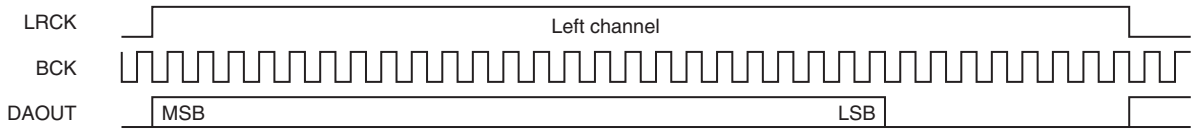
Name of iif_mode	IFEXMD	IIFSEL [1 : 0]	Data input format
mode-0	0	00	MSB first, Left Justified 24 bits
mode-1	0	01	I^2S 24 bits
mode-2	0	10	LSB first, Right Justified 24 bits
mode-3	0	11	MSB first, Right Justified 24 bits
mode-4	1	00	MSB first, Right Justified 20 bits
mode-5	1	01	MSB first, Right Justified 16 bits

Note) 1. When CHNM_BL is set to “1” by the CHNM_BL pin or address 01h of serial data interface, only high-order 16 bits are validated during Full-band mode.

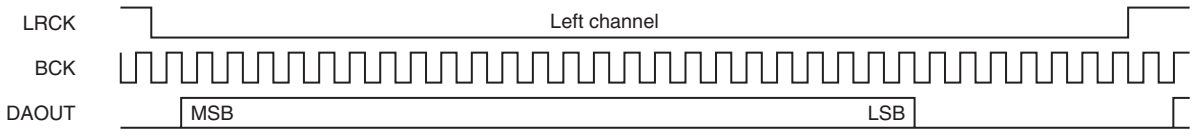
2. Only high-order 16 bits are validated during Half-band mode.

Timing charts covering what has been described above are presented below.

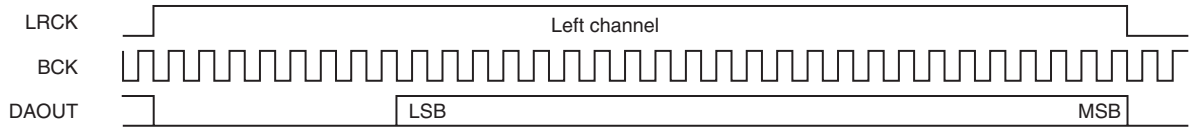
Audio ADC interface timing charts



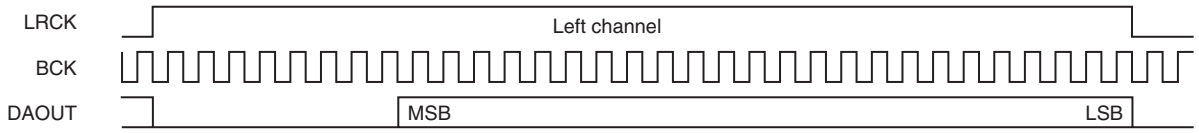
mode-0



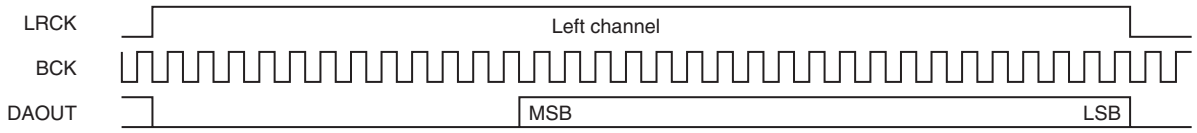
mode-1



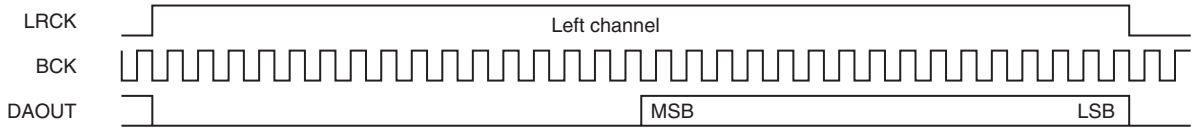
mode-2



mode-3

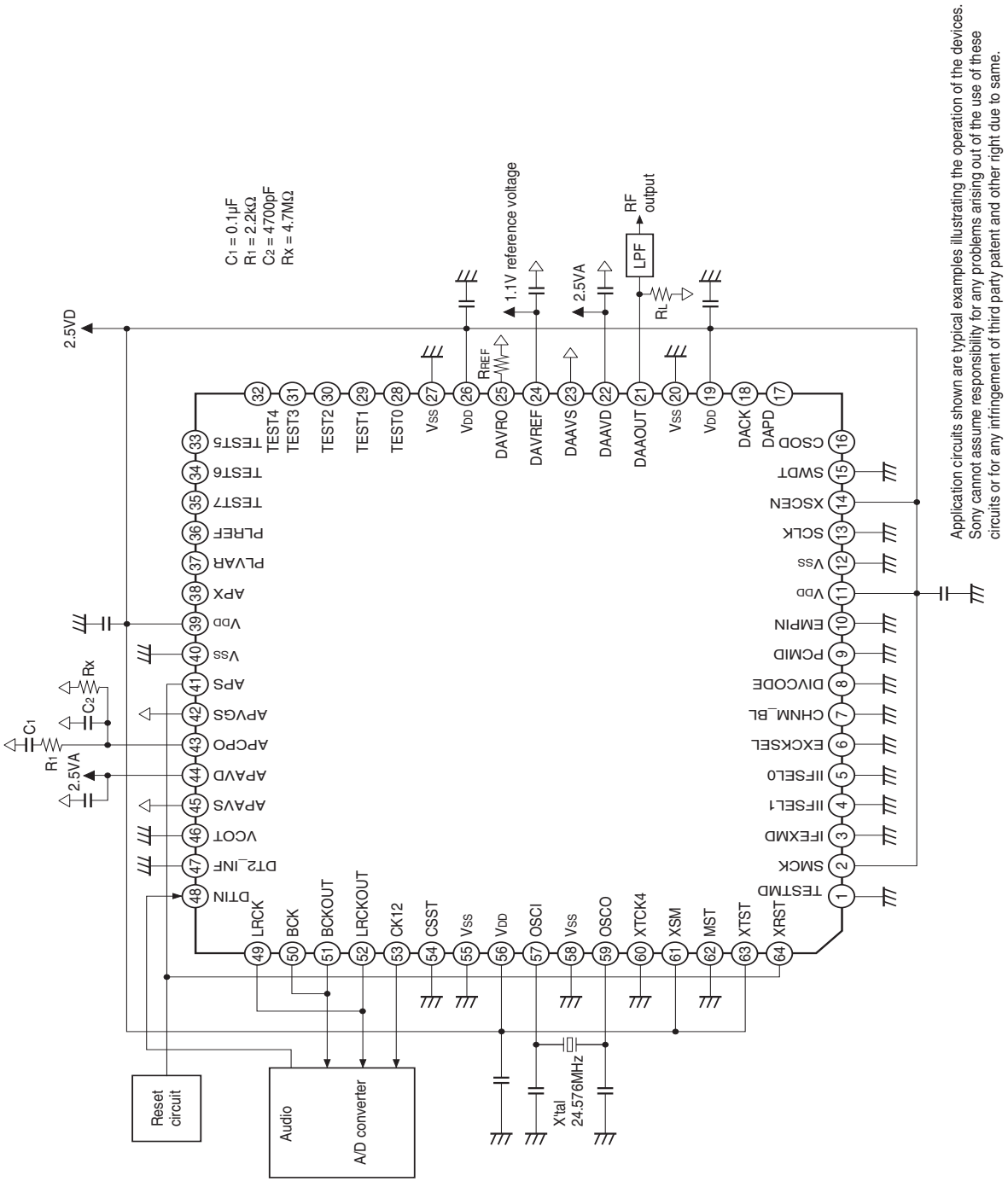


mode-4



mode-5

Application Circuit



Notes on Operation

◆ The loop filter portion of the PLL block is important for the characteristics. Therefore, the loop filter should be located as close to the IC pin as possible and surrounded by AGND. In addition, temperature compensation parts should be used for the loop filter capacitor and resistor.

◆ The CXD4016R generates a delay during transmission. Labeling the sampling frequency as fs, the delay time is 192/fs [s] in full-band mode. For example, when fs = 48kHz, the delay time is 4ms. In addition, in half-band mode the delay time is 384/fs [s]. In this case for example, when fs = 48kHz, the delay time is 8ms. Note that a delay is also generated during reception by the receive side IC CXD4017R. See the CXD4017R data sheet for details.

CXD4016R Evaluation Board

Description

The CXD4016R evaluation board is a dedicated board designed to allow easy evaluation of the CXD4016R which was developed for transmission of infrared spatial digital audio communication. Optical digital and analog (pin jack) circuits are mounted, and can be switched by a switch.
The input audio signal is converted to an infrared spatial digital audio communication system format RF signal by the CXD4016R, and output from a SMB connector.

Features

◆ Supply voltage : + 5V single power supply
◆ Analog and optical digital audio input can be selected

Operating Conditions

◆ Supply voltage : + 5V (typ.)
◆ Current consumption : 150mA (typ.)
◆ Input signal : Analog or optical digital audio signal

Operation Method

The CXD4016R evaluation board allows easy evaluation simply by providing the power supply and inputting an analog or optical digital audio signal. The evaluation procedure is as follows.

1. Connect the power supply to the power supply connection pin J5.
2. SW1 is the manual reset switch. A reset is applied automatically during power-on, but this switch is used to perform reset manually.
3. The DIVCODE pin can be set by DIP switch S2-1. The DIVCODE pin is set low when this switch is OFF, and high when ON.
4. The CHNM_BL pin can be set by DIP switch S2-2. The CHNM_BL pin is set low when this switch is OFF, and high when ON.
5. The IFEXMD pin can be set by DIP switch S2-4. The IFEXMD pin is set low when this switch is OFF, and high when ON
6. The IIFSEL1 pin can be set by DIP switch S2-5. The IIFSEL1 pin is set low when this switch is OFF, and high when ON.
7. The IIFSEL0 pin can be set by DIP switch S2-6. The IIFSEL0 pin is set low when this switch is OFF, and high when ON.
8. The audio signal can be selected by DIP switch S2-7. The optical digital audio signal is selected when this switch is OFF, and the analog audio signal when ON.
9. Connect the optical digital audio signal to the U8 square optical connector.
10. Connect the analog audio signal to the J1 pin jack.

11. When the analog audio signal is selected, the sampling frequency can be changed by DIP switch S2-8. 48kHz is set when this switch is OFF, and 44.1kHz when ON.
12. Always set DIP switches other than noted above to OFF. The above contents are listed in the tables below for reference.

S1	Mode
1	Always OFF
2	Always OFF
3	Always OFF
4	Always OFF
5	Always OFF
6	Always OFF
7	Always OFF
8	Always OFF

S2	Mode
1	OFF : DIVCODE = L, ON : DIVCODE = H
2	OFF : CHNM_BL = L, ON : CHNM_BL = H
3	Always OFF
4	OFF : IFEXMD = L, ON : IFEXMD = H
5	OFF : IIFSEL1 = L, ON : IIFSEL1 = H
6	OFF : IIFSEL0 = L, ON : IIFSEL0 = H
7	OFF : Optical digital, ON : Analog
8	OFF : 48kHz, ON : 44.1kHz (only when the analog audio signal is selected)

13. Light emitting diode D1 is off when DIVCODE is low, and lighted when DIVCODE is high.
14. Light emitting diode D2 is off when CHNM_BL is low, and lighted when CHNM_BL is high.
15. Light emitting diodes D3 and D4 indicate the sampling frequency of the audio signal. This relationship is shown in the table below.

D3, D4	Sampling frequency
Off, off	44.1kHz
Off, lighted	48kHz
Lighted, lighted	32kHz
Flashing, flashing	Unlock

16. Light emitting diodes D5 to D8 are not used.
17. The infrared spatial digital audio communication system format RF signal is output from SMB connector J8.
18. J2 and J3 are not used.

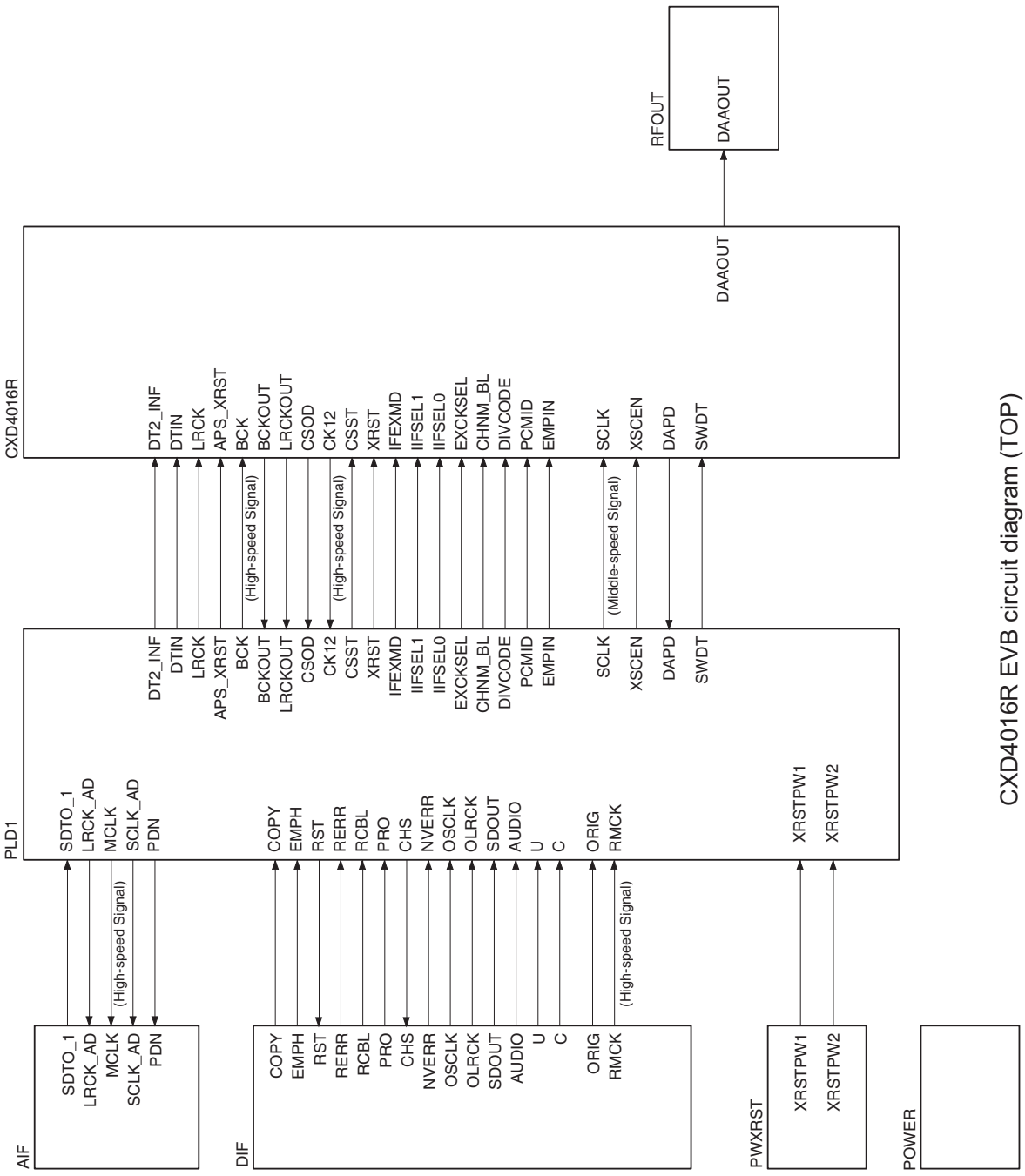
CXD4016R EVB Semiconductor Parts List

Parts No.	Product name	Manufacturer
U1, 3	NJM2100M	New Japan Radio
U2	AK5353VT	Asahi Kasei Microsystems
U4, 21	TC74LCX541F	Toshiba
U5	CXD4016R	SONY
U6	TC74VHC04F	Toshiba
U7	CS8415A-CZ	Cirrus Logic
U8	TORX141P	Toshiba
U9	FXO-31FL 24.576MHz	Kyocera Kinseki
U10	EP1K100QI208-2	ALTERA
U11	EPC2LI20	ALTERA
U12	FXO-31FL 22.5792MHz	Kyocera Kinseki
U13, 14, 15, 16, 17, 18	LM317A	National Semiconductor
U19, 20	TL7705CP	Texas Instruments
U22	AD8057ART	Analog Devices
Q1	2SC2223L	NEC
D1, 2	TLG124	Toshiba
D3, 4	TLY124	Toshiba
D5, 6	TLO124	Toshiba
D7, 8	TLR124	Toshiba
D9 to 20	1S1588	Toshiba

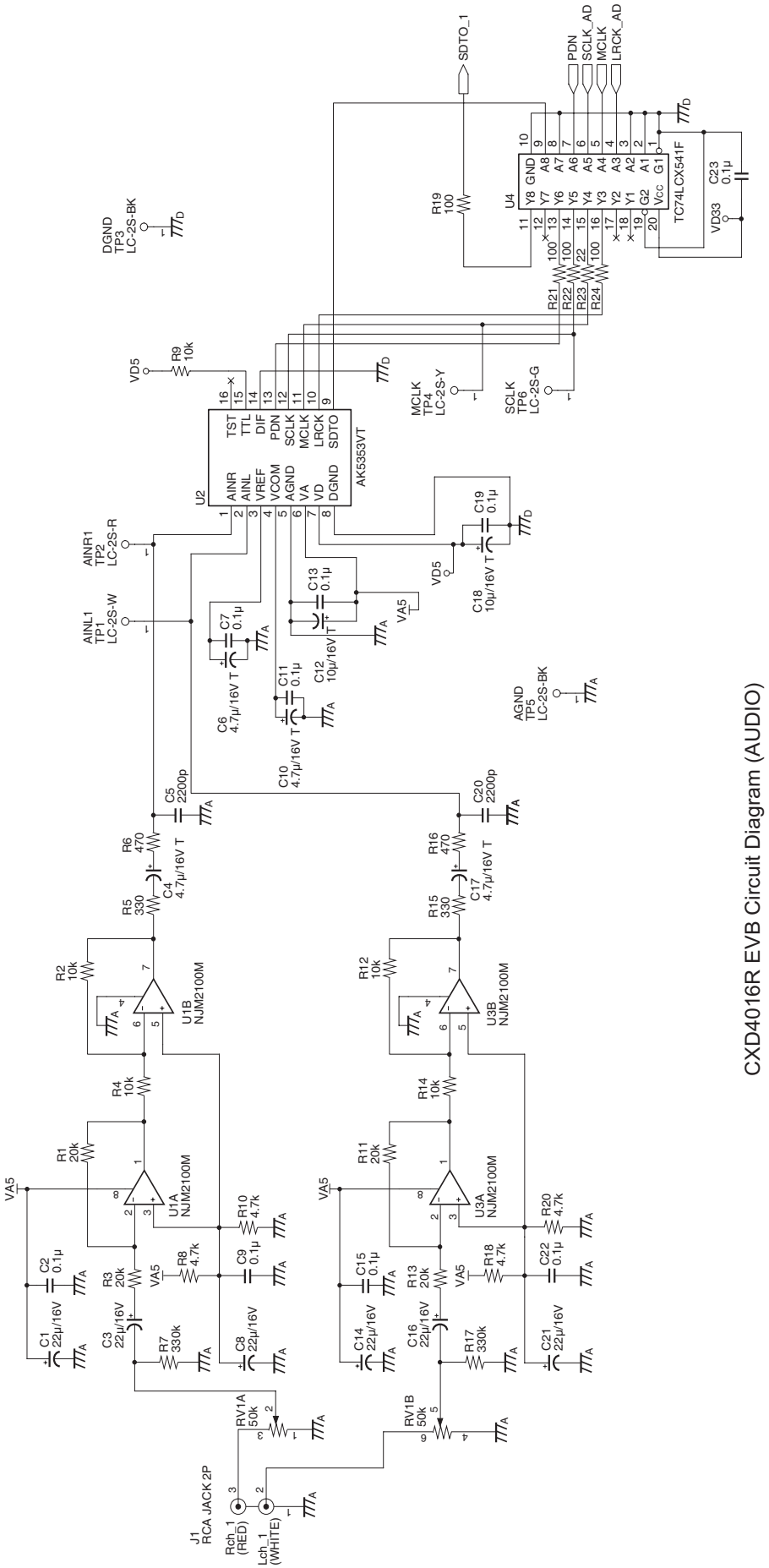
FPGA Operation

1. Selects the optical digital audio signal or the analog audio signal selected by S2-7.
2. Converts the selected audio signal to the DTIN pin input format set by S2-4, S2-5 and S2-6.
3. Detects the sampling frequency.

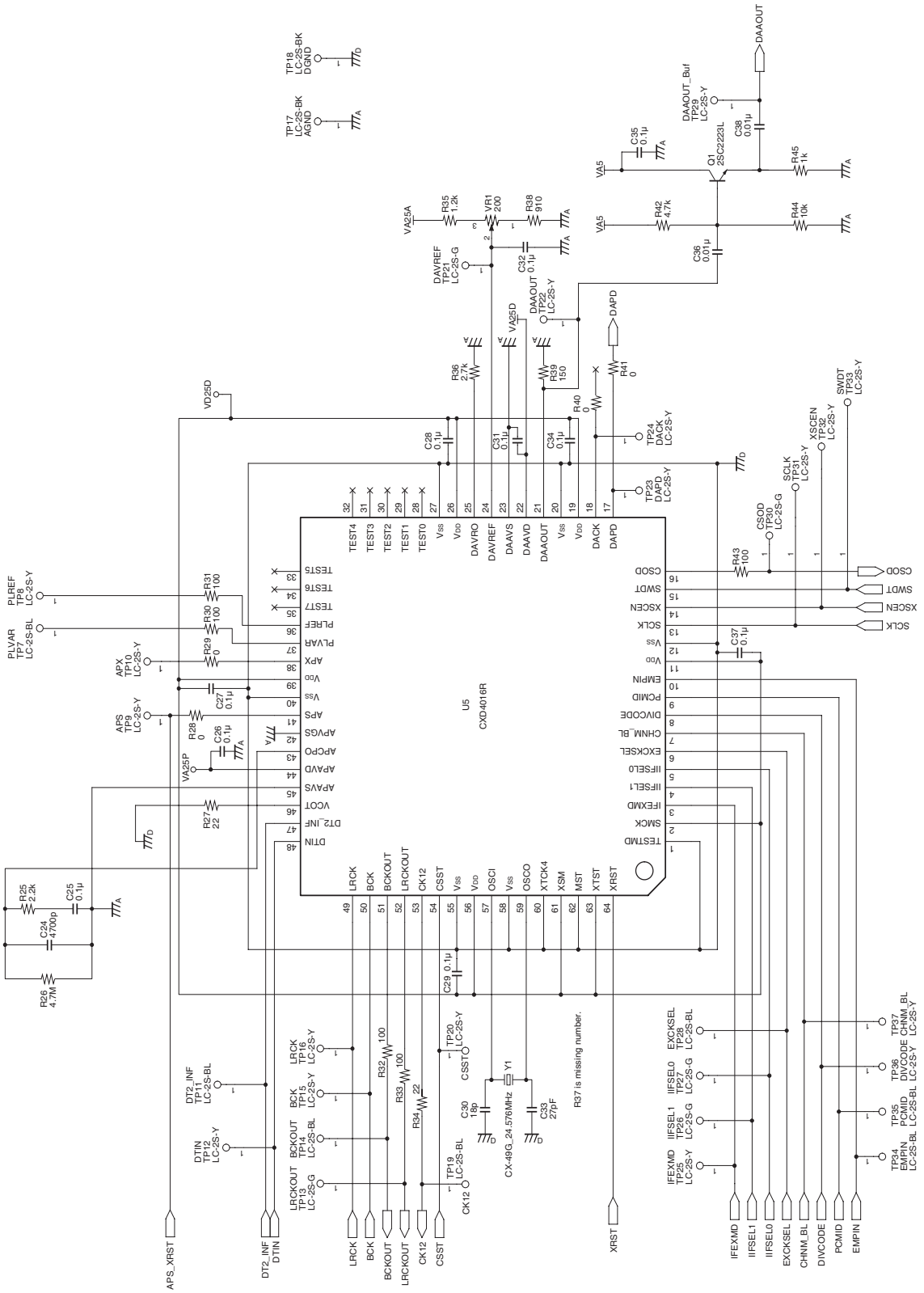
Circuit Diagram



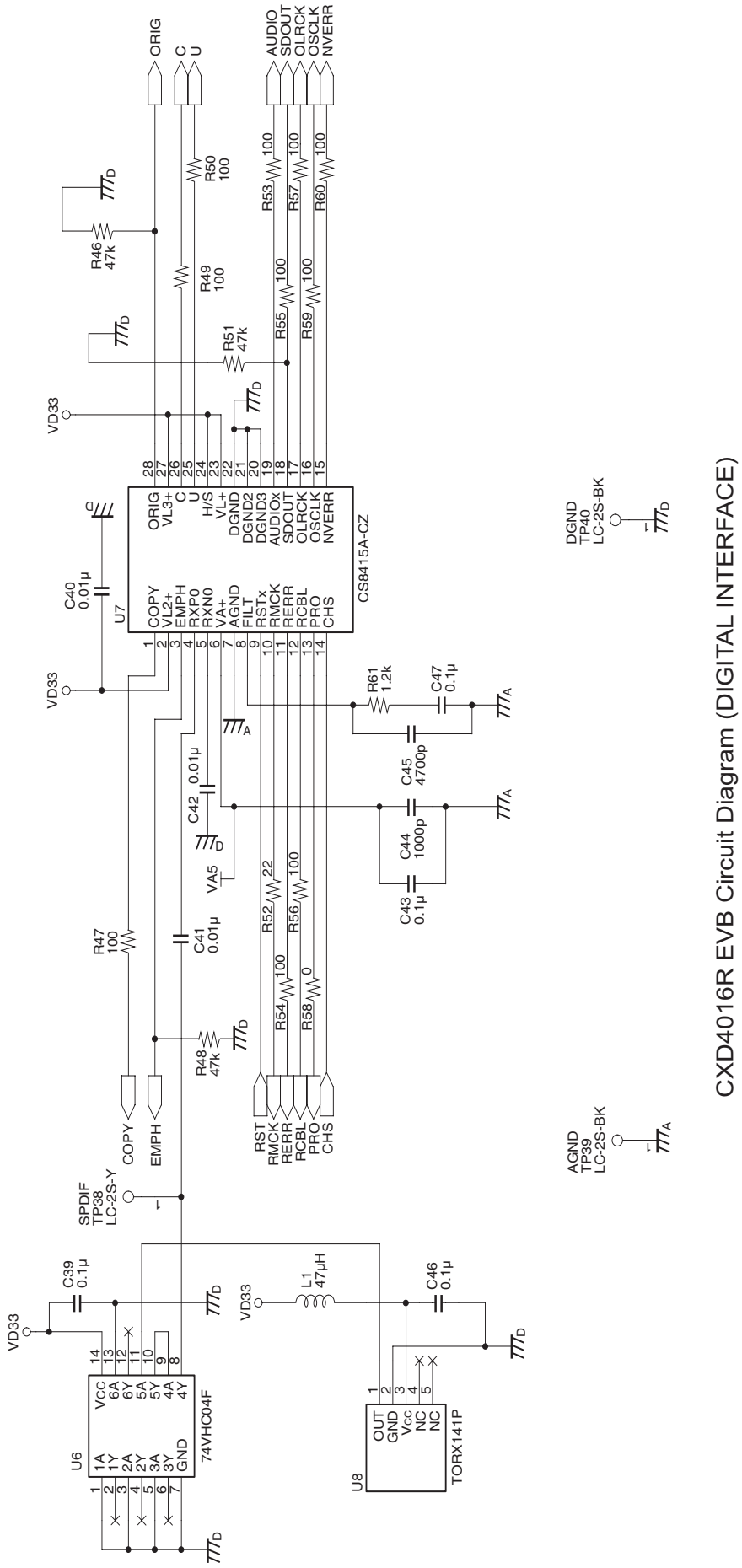
CXD4016R EVB circuit diagram (TOP)

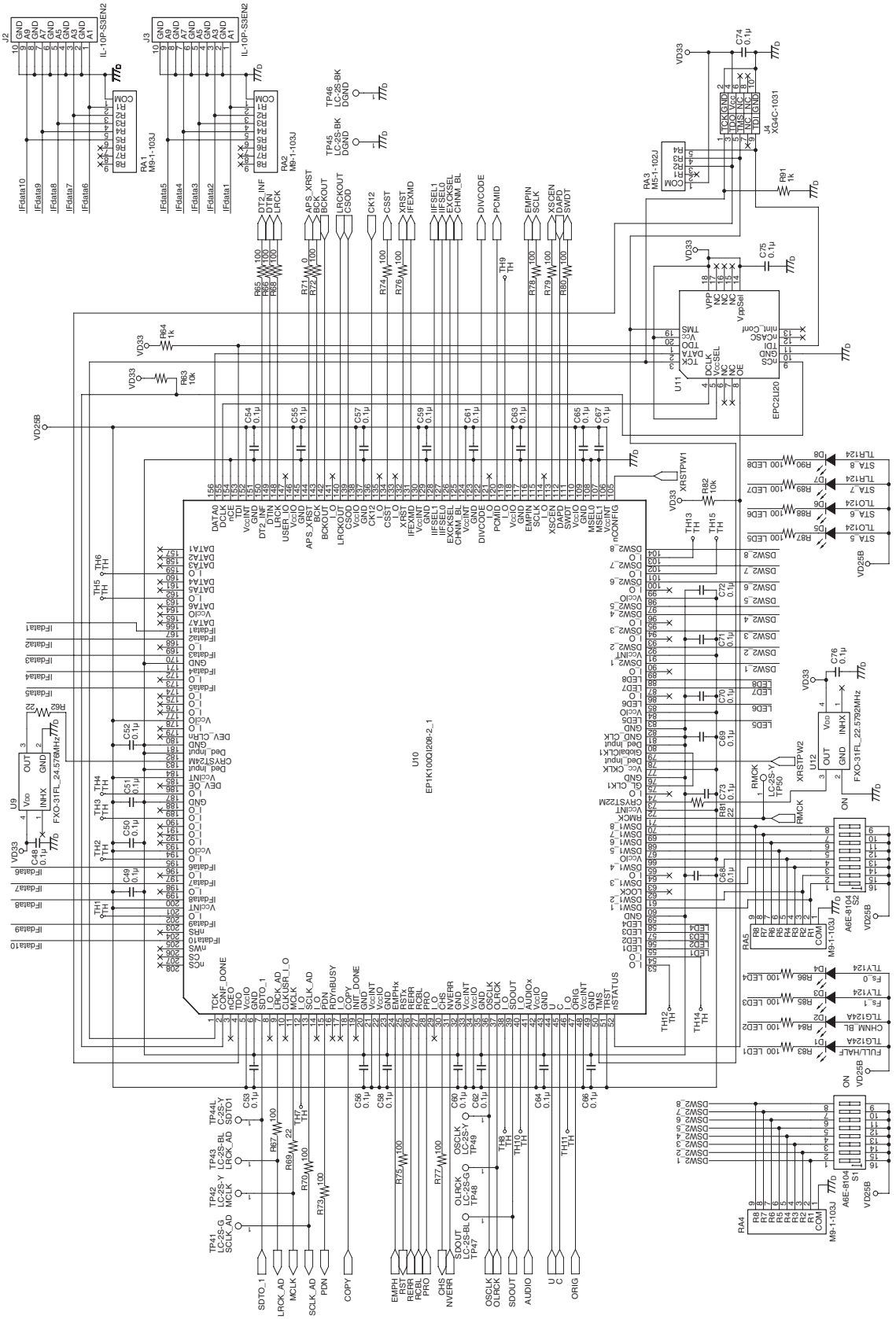


CXD4016R EVB Circuit Diagram (AUDIO)

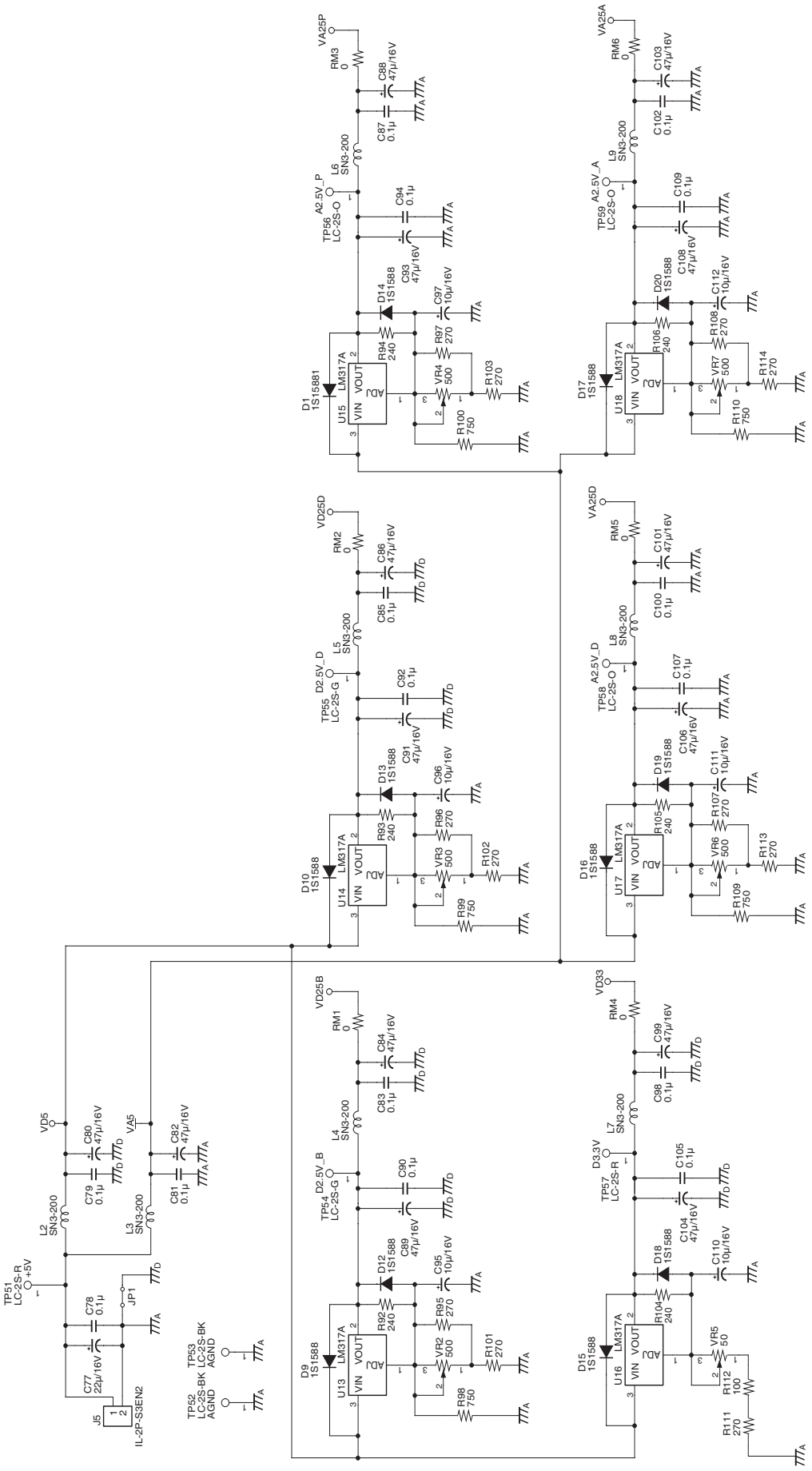


CXD4016R EVB Circuit Diagram (MAIN)

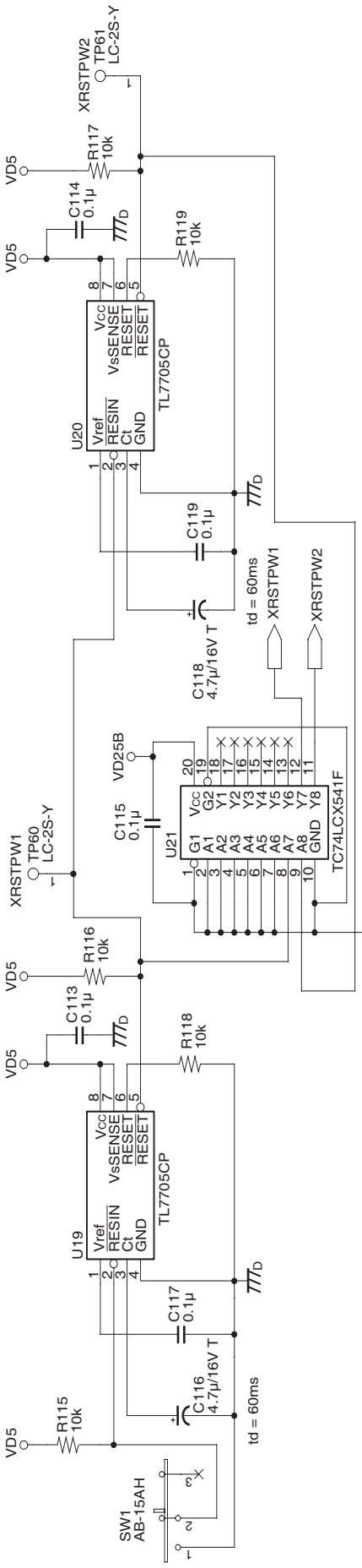

CXD4016R EVB Circuit Diagram (DIGITAL INTERFACE)
U7
CS8415A-CZ
U6
74VHC04F
U8
TORX141P
VD33
ORIG
C
U
AUDIO
SDOUT
OLRCK
OSCLK
NVERR
COPY
EMPH
RST
RMCK
RERR
RCBL
PRO
CHS
SPDIF TP38 LC-2S-Y
DGND TP40 LC-2S-BK
AGND TP39 LC-2S-BK
C40 0.01µ
C41 0.01µ
C42 0.01µ
C43 0.1µ
C44 1000p
C45 4700p
C46 0.1µ
C47 0.1µ
C39 0.1µ
L1 47µH
R46 47k
R47 100
R48 47k
R49 100
R50 100
R51 47k
R52 22
R53 100
R54 100
R55 100
R56 100
R57 100
R58 0
R59 100
R60 100
R61 1.2k
VA5



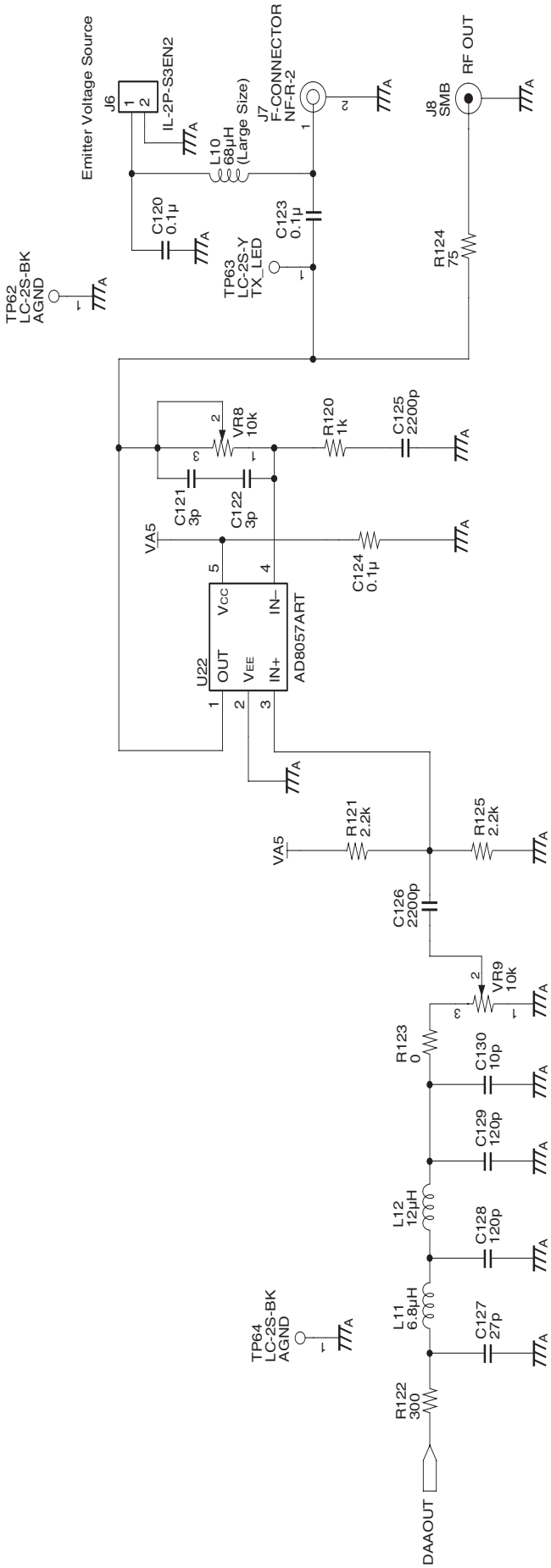
CXD4016R EVB Circuit Diagram (PLD)



CXD4016R EVB Circuit Diagram (POWER)

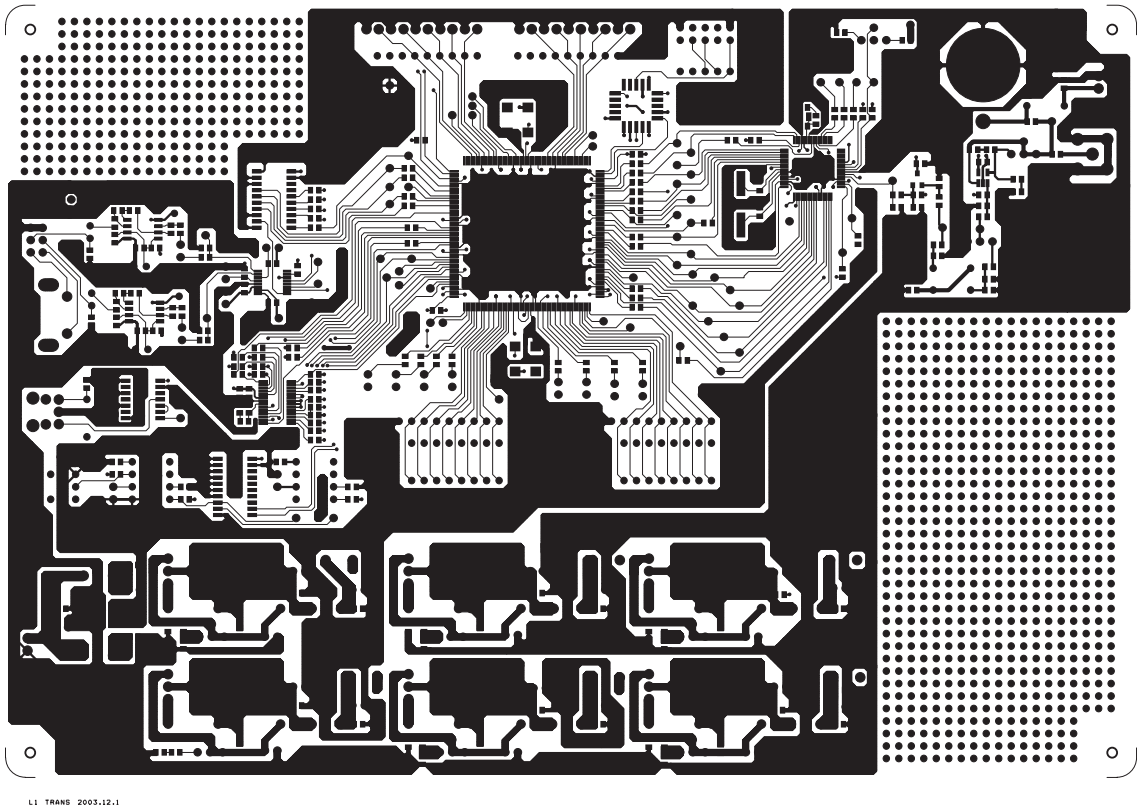


CXD4016R EVB Circuit Diagram (RESET)

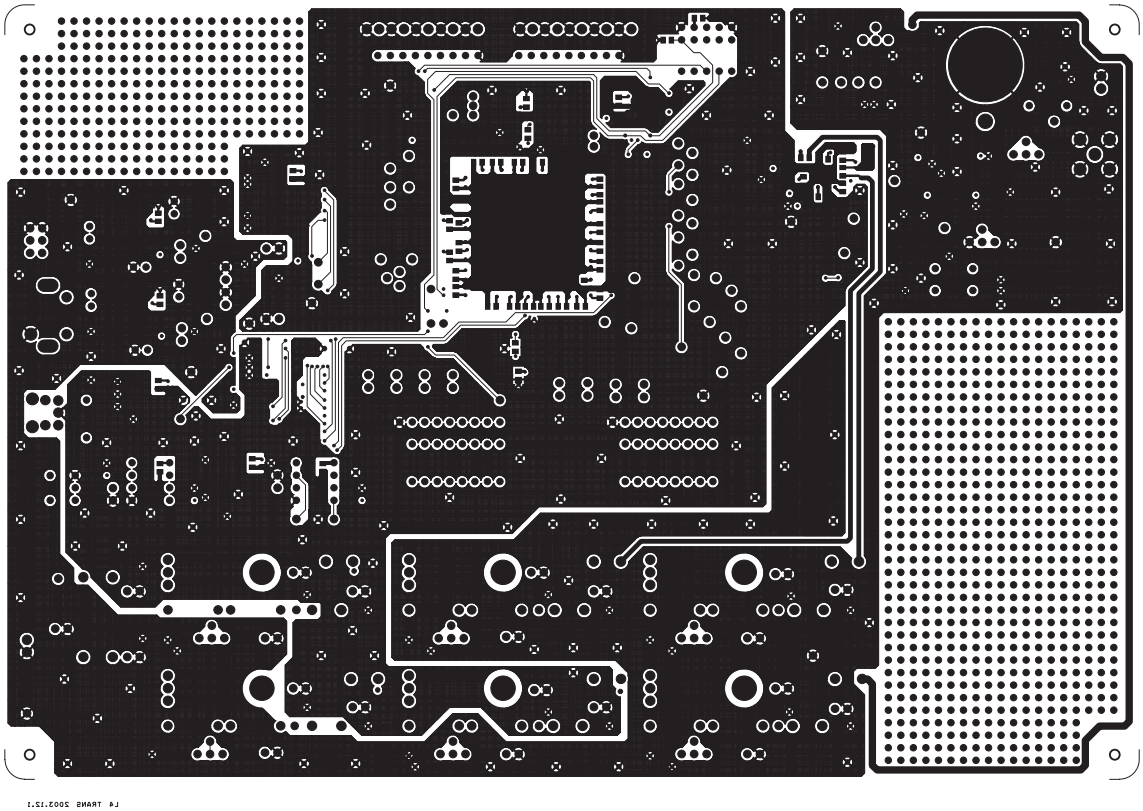


CXD4016R EVB Circuit Diagram (RFOUT)

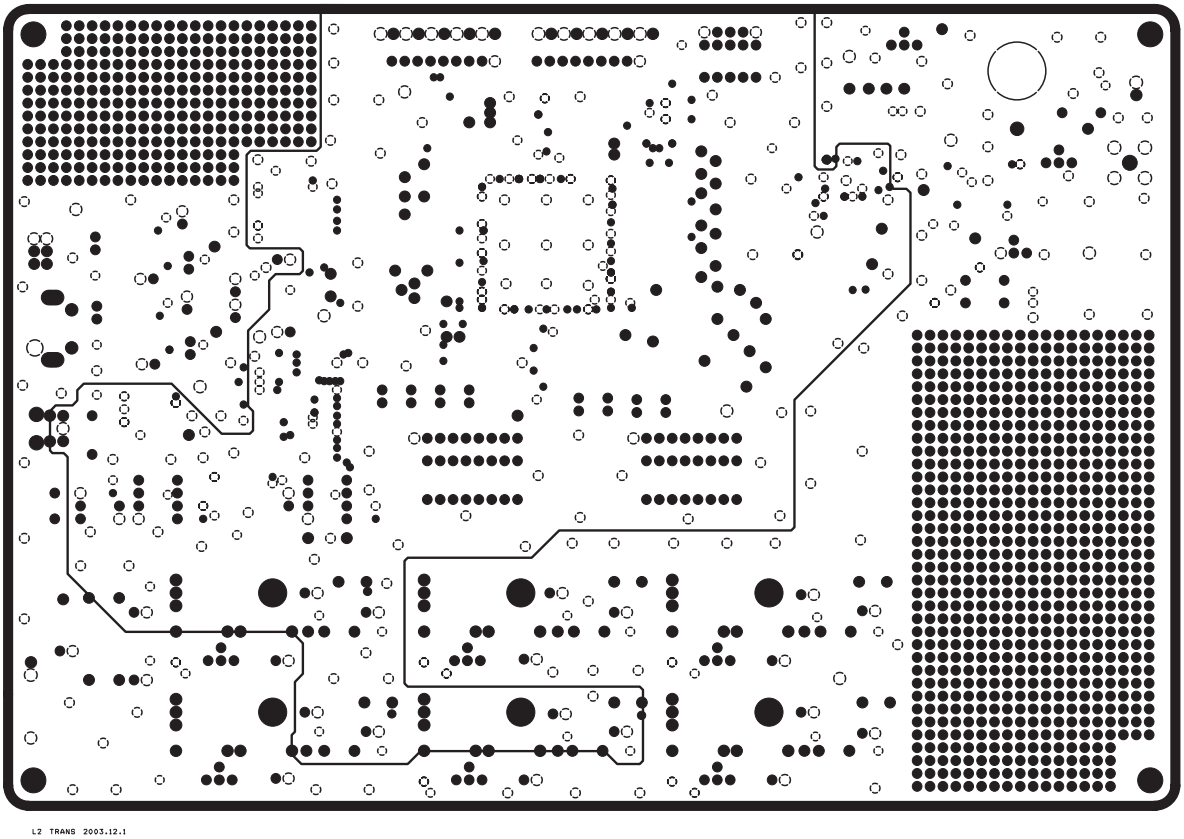
Pattern Diagram



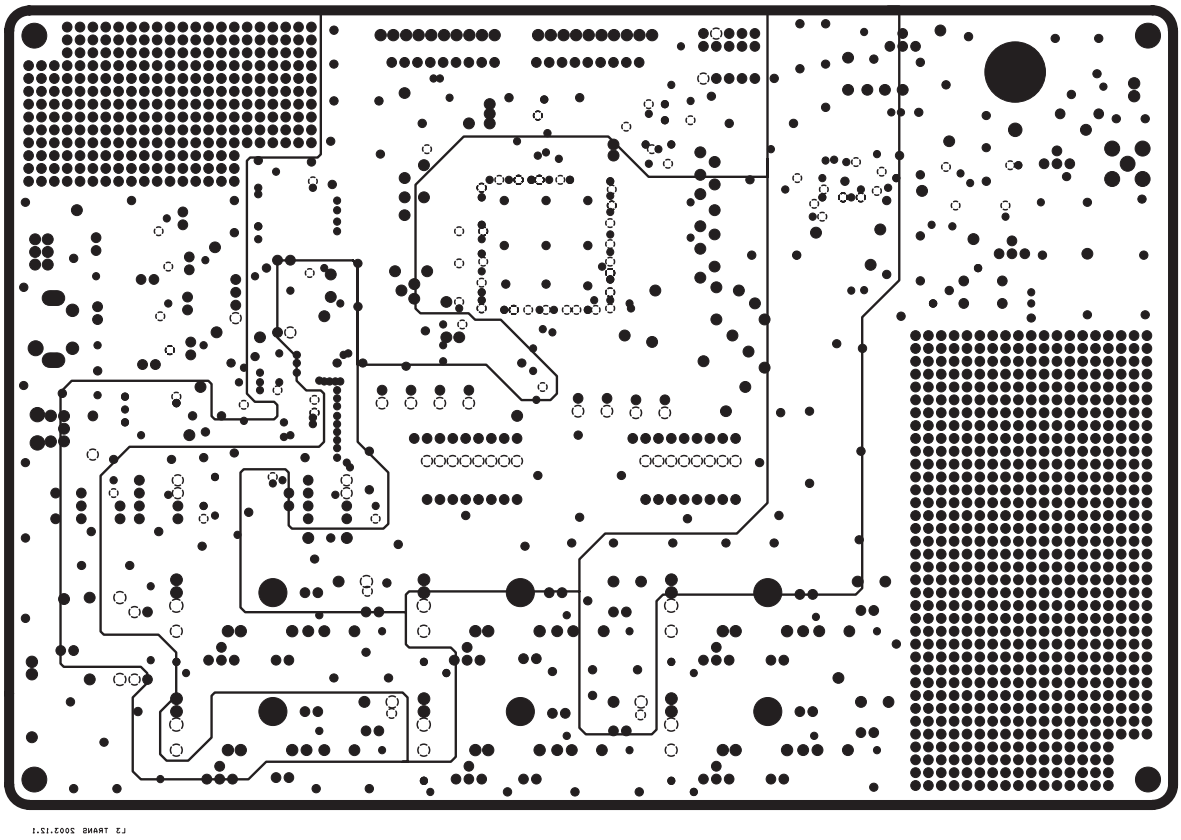
CXD4016R EVB A Side Pattern Diagram



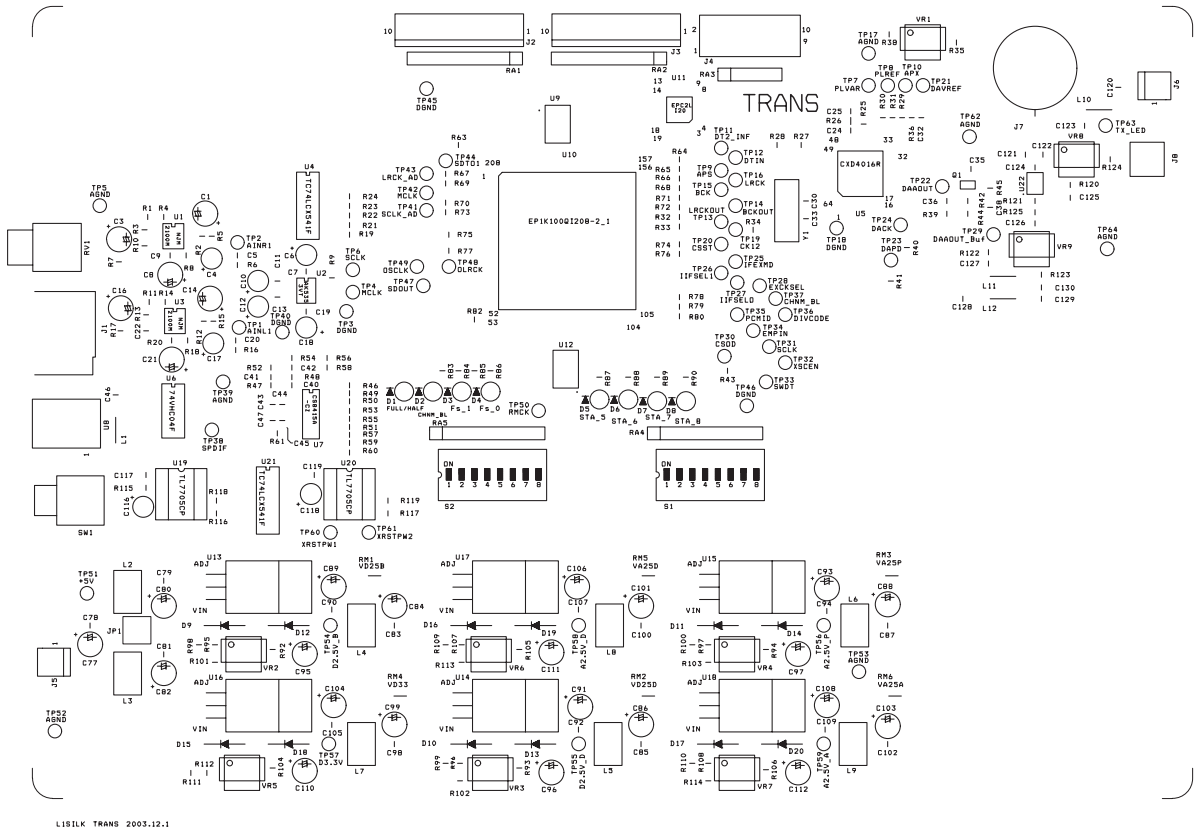
CXD4016R EVB B Side Pattern Diagram



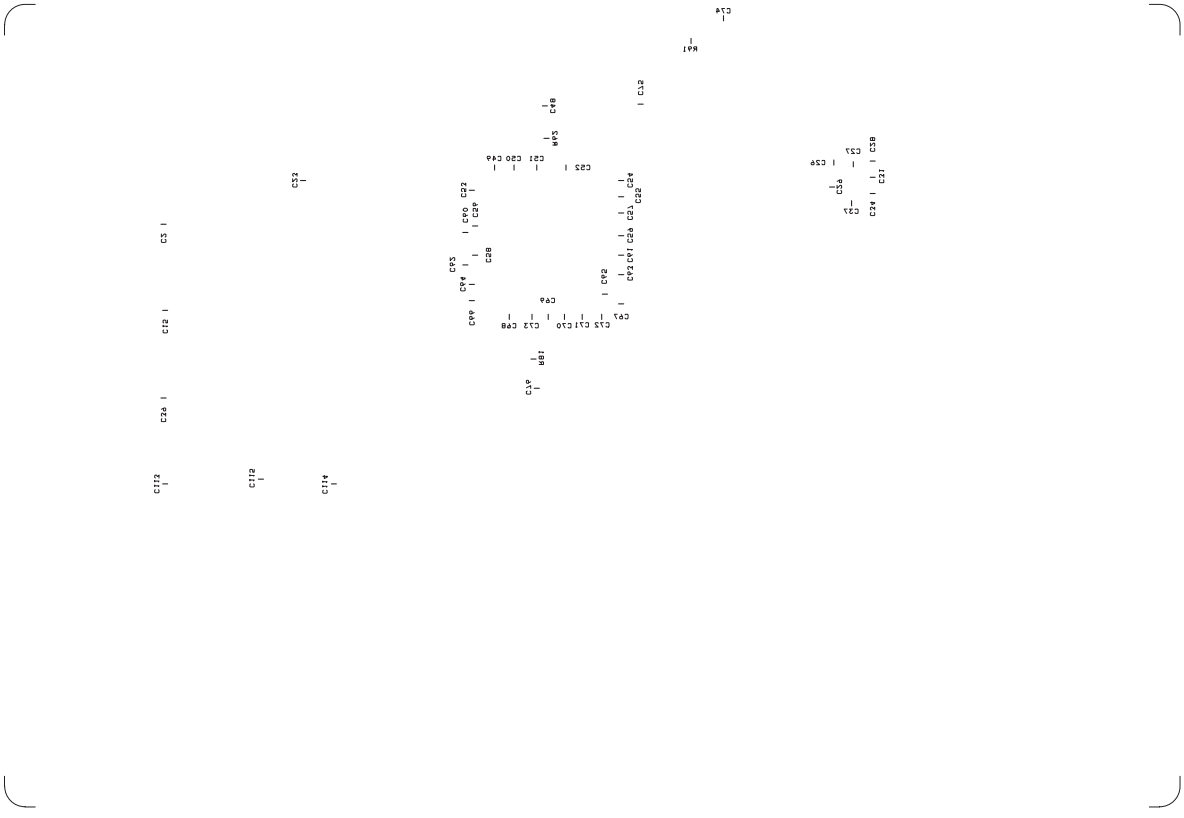
CXD4016R EVB GND Layer Pattern Diagram



CXD4016R EVB Power Supply Layer Pattern Diagram



CXD4016R EVB A Side Silk Diagram

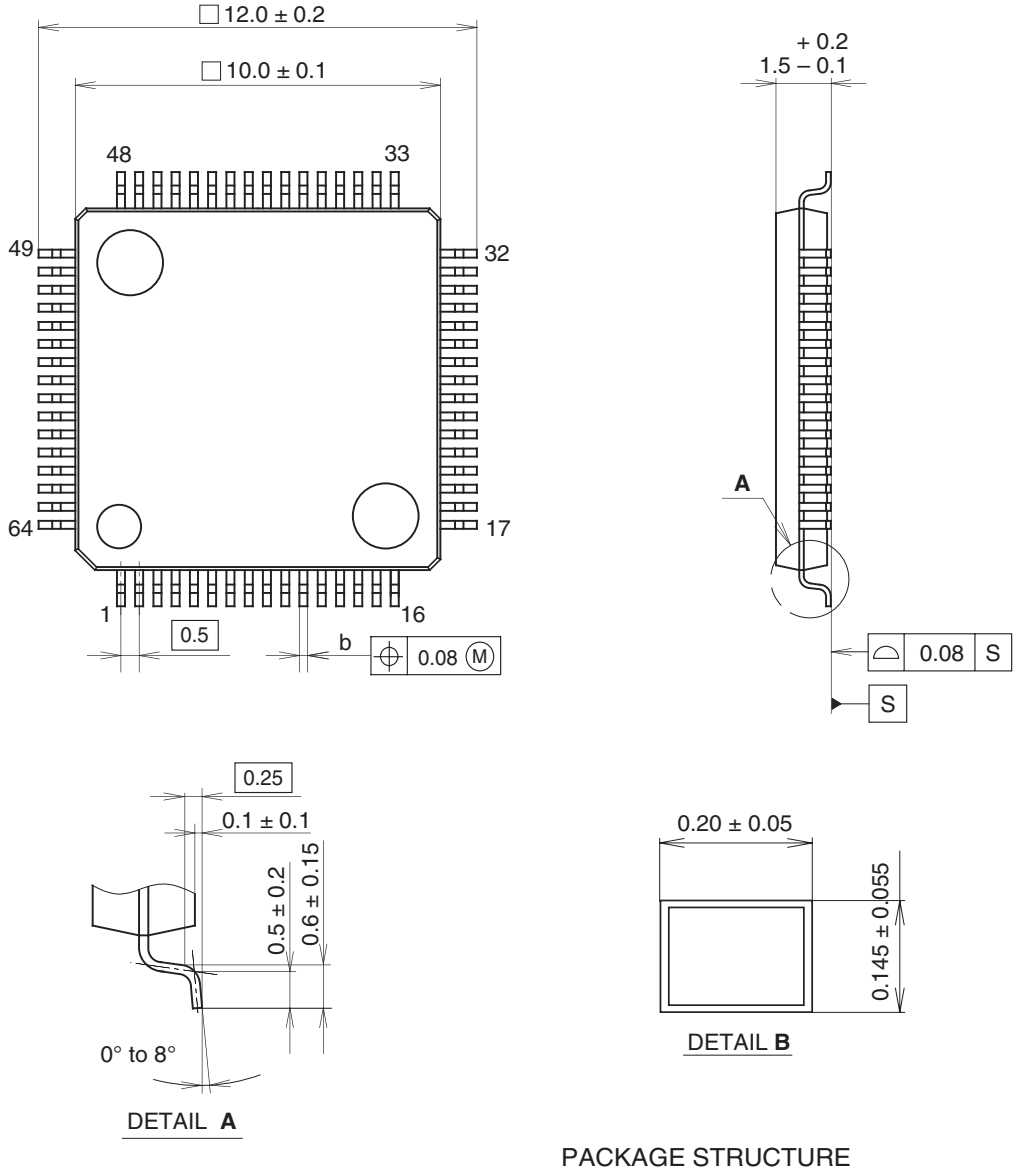


CXD4016R EVB B Side Silk Diagram

Package Outline

(Unit : mm)

64PIN LQFP (PLASTIC)



SONY CODE	LQFP-64P-L023
JEITA CODE	P-LQFP64-10X10-0.5
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
TERMINAL TREATMENT	SOLDER PLATING
TERMINAL MATERIAL	42 ALLOY
PACKAGE MASS	0.32g

LEAD PLATING SPECIFICATIONS

ITEM	SPEC.
LEAD MATERIAL	42 ALLOY
SOLDER COMPOSITION	Sn-2%Bi
PLATING THICKNESS	5-20µm