SONY

CXD3057R

CD Digital Signal Processor with Built-in RF Amplifier and Digital Servo + Digital High & Bass Boost

Description

The CXD3057R is a digital signal processor LSI for CD players. This LSI incorporates a RF amplifier and digital servo, high & bass boost, 1-bit DAC and analog low-pass filter.

Features

- All digital signal processing during playback is performed with a single chip
- Highly integrated mounting possible due to a built-in RF amplifier

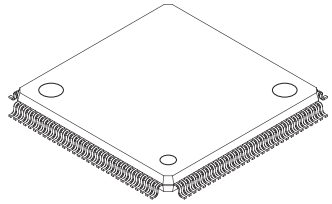
RF Block
- Supports 4× speed playback CD
- RF system equalizer
- Supports pickup built-in RF summing amplifier
- Gain level switch
- TE balance adjustment function

Digital Signal Processor (DSP) Block
- Supports CAV (Constant Angular Velocity) playback
  - Frame jitter free
  - 0.5× to 4× speed continuous playback possible
  - Allows relative rotational velocity readout
- Supports variable pitch playback
- The bit clock, which strobes the EFM signal, is generated by the digital PLL.
- EFM data demodulation
- Enhanced EFM frame sync signal protection
- Refined super strategy-based powerful error correction
  C1: double correction, C2: quadruple correction
  Supported during 4× speed playback
- Noise reduction during track jumps
- Auto zero-cross mute
- Subcode demodulation and subcode-Q data error detection
- Digital spindle servo
- 16-bit traverse counter
- Asymmetry correction circuit
- CPU interface on serial bus
- Error correction monitor signal, etc. output from CPU interface
- Servo auto sequencer
- Fine search performs track jumps with high accuracy
- Digital audio interface outputs
- Digital level meter, peak meter
- Bilingual compatible
- VCO control mode
- CD TEXT data demodulation

Digital Servo (DSSP) Block
- Microcomputer software-based flexible servo control
- Offset cancel function for servo error signal
- Auto gain control function for servo loop
- E:F balance, focus bias adjustment functions
- Surf jump function supporting micro two-axis
- Tracking filter: 6 stages,
  Focus filter: 5 stages

Digital Filter, DAC and Analog Low-pass Filter Blocks
- Digital dynamic bass boost and high boost
  Bass Boost: 4th-order IIR 24dB/Oct
  +10dB/+14dB/+18dB/+22dB
  High Boost: Second-order IIR 12dB/Oct
  +4dB/+6dB/+8dB/+10dB
- Independent turnover frequency selection possible
  Bass Boost: 125Hz/160Hz/200Hz
  High Boost: 5kHz/7kHz

120 pin LQFP (Plastic)



- Digital dynamics (compressor)
  Volume increased by +5dB at low level
- 8× oversampling digital filter
  (attenuation: 61dB, ripple within band: ±0.0075dB)
- Digital signal output possible after boost
- Serial data format selectable from (output)
  20 bits/18 bits/16 bits (rearward truncation, MSB first)
- Digital attenuation: –∞, –60 to +6dB, 2048 steps (linear)
- Soft mute
- Digital de-emphasis

Applications

CD players

Structure

Silicon gate CMOS IC

Absolute Maximum Ratings (Ta = 25°C)

• Supply voltage 1	V_{DD}, XV_{DD}	V_{SS} – 0.5 to +3.5	V
• Input voltage 1	$V_{I}1$	V_{SS} – 0.3 to V_{DD} + 0.3	V
• Output voltage 1	$V_{O}1$	V_{SS} – 0.3 to V_{DD} + 0.3	V
• Supply voltage 2	IOV_{DD}0 to 2, AV_{DD}0 to 5		
		IOV_{SS} – 0.5 to +4.5	V
• Input voltage 2	$V_{I}2$	IOV_{SS} – 0.3 to IOV_{DD} + 0.3	V
• Output voltage 2	$V_{O}2$	IOV_{SS} – 0.3 to IOV_{DD} + 0.3	V
• Storage temperature			
	Tstg	–55 to +150	°C
• Supply voltage difference			
	IOV_{SS}, AV_{SS}, XV_{SS} – V_{SS}		
		–0.3 to +0.3	V
	XV_{DD} – V_{DD}	–0.3 to +0.3	V
	IOV_{DD}, AV_{DD}, XV_{DD} – V_{DD}		
		–0.3 to +0.3	V
		(IOV_{DD}, AV_{DD}, XV_{DD} < 2.3V)	

Recommended Operating Conditions

• Supply voltage 1	V_{DD}, XV_{DD}	2.5 ± 0.2	V
• Supply voltage 2	IOV_{DD}0 to 2, AV_{DD}0 to 5		
		3.3 ± 0.3	V
• Operating temperature			
	Topr	–40 to +85	°C

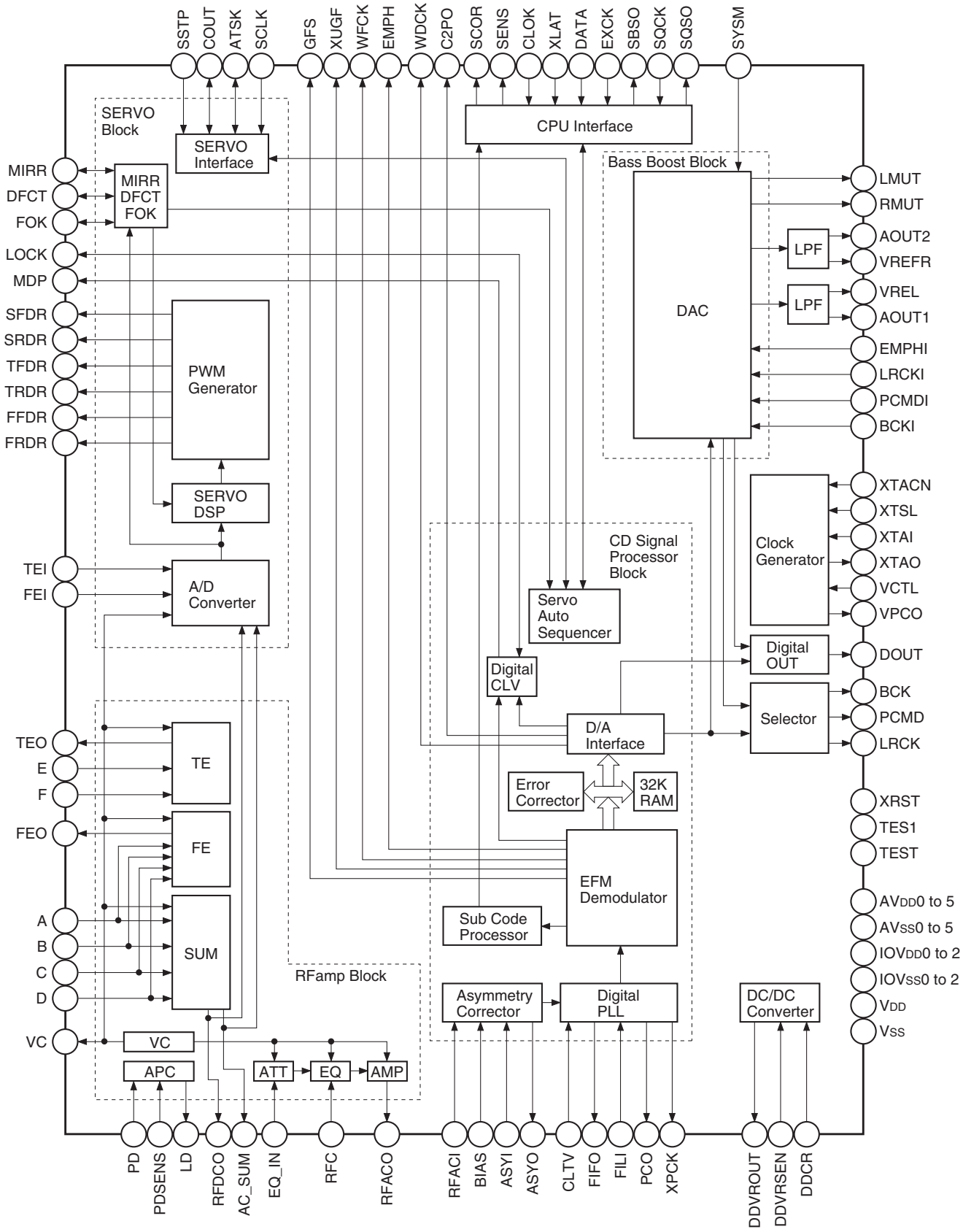
I/O Pin Capacitance

• Input capacitance	C_I	7 (Max.)	pF
• Output capacitance	C_O	7 (Max.)	pF
• I/O capacitance	$C_{I/O}$	7 (Max.)	pF

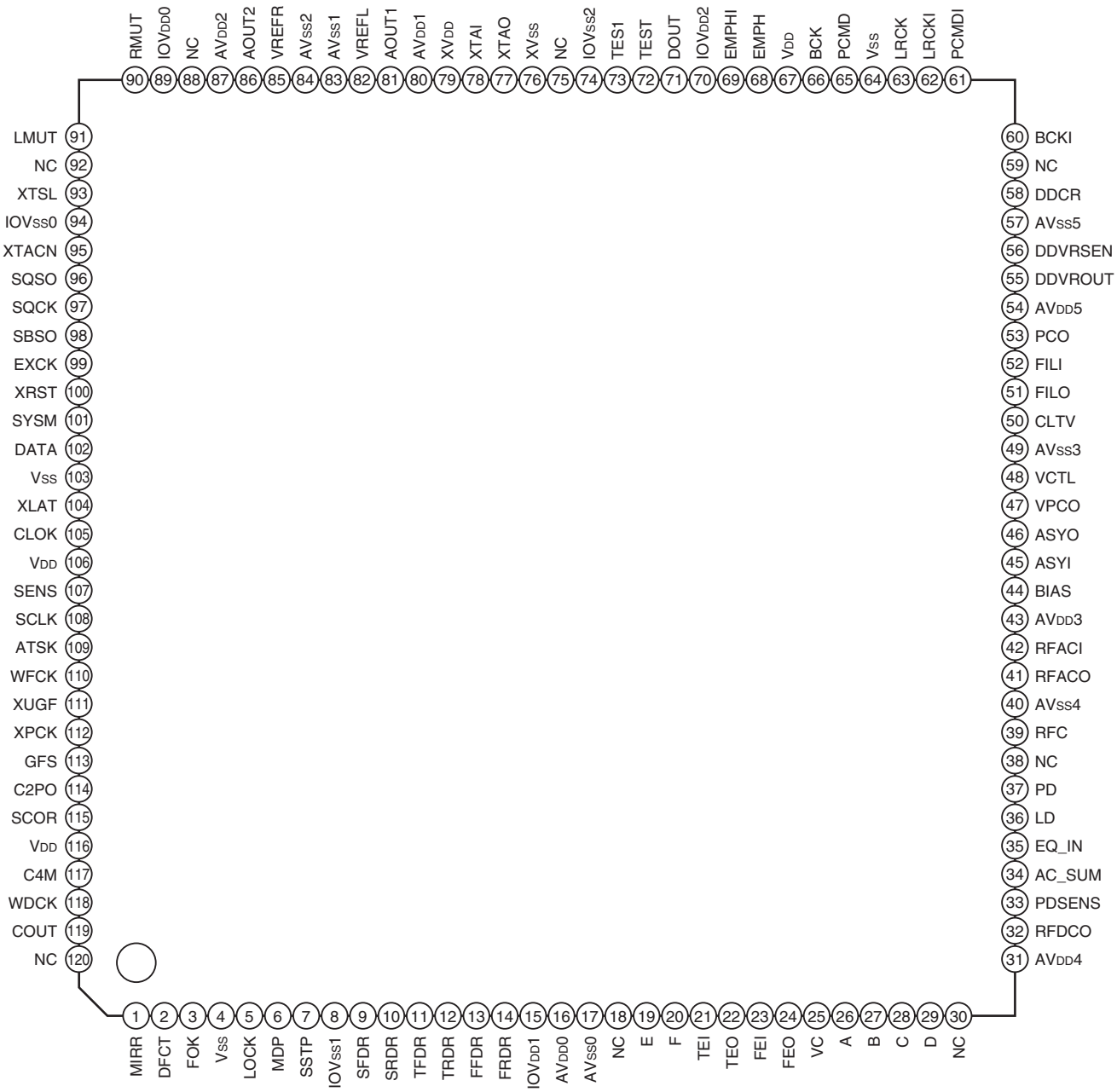
Note) Measurement conditions V_{DD} = V_I = 0V
f_M = 1MHz

E04250A22

Block Diagram



Pin Configuration



Pin Description

Power supply	Pin No.	Symbol	I/O		Description
Digital I/O = 3.3V Internal = 2.5V	1	MIRR	I/O	1, 0	Mirror signal input/output.
	2	DFCT	I/O	1, 0	Defect signal input/output.
	3	FOK	I/O	1, 0	Focus OK signal input/output.
	4	V_{SS}	—	—	Internal digital GND.
	5	LOCK	I/O	1, 0	GFS is sampled at 460Hz; when GFS is high, this pin outputs a high signal. If GFS is low eight consecutive samples, this pin outputs low. Or this pin inputs when LKIN = "1".
	6	MDP	O	1, Z, 0	Spindle motor servo control output.
	7	SSTP	I		Disk innermost detection signal input.
	8	$IOV_{SS}1$	—	—	I/O digital GND.
	9	SFDR	O	1, 0	Sled drive output.
	10	SRDR	O	1, 0	Sled drive output.
	11	TFDR	O	1, 0	Tracking drive output.
	12	TRDR	O	1, 0	Tracking drive output.
	13	FFDR	O	1, 0	Focus drive output.
	14	FRDR	O	1, 0	Focus drive output.
	15	$IOV_{DD}1$	—	—	I/O digital power supply.
A/D 3.3V	16	$AV_{DD}0$	—	—	Analog power supply.
	17	$AV_{SS}0$	—	—	Analog GND.
—	18	NC	—	—	
RFamp 3.3V	19	E	I		E signal input.
	20	F	I		F signal input.
	21	TEI	I		Tracking error signal input to DSSP block.
	22	TEO	O		Tracking error signal output from RF amplifier block.
	23	FEI	I		Focus error signal input to DSSP block.
	24	FEO	O		Focus error signal output from RF amplifier block.
	25	VC	I/O		Center voltage output from RF amplifier block. Center voltage input to DSSP block by command switch.
	26	A	I		A signal input.
	27	B	I		B signal input.
	28	C	I		C signal input.
	29	D	I		D signal input.
	30	NC	—	—	
	31	$AV_{DD}4$	—	—	Analog power supply.
	32	RFDCO	I/O		RFDC signal output. RFDC signal input to DSSP block by command switch.
	33	PDSENS	I		Reference voltage pin for PD.
	34	AC_SUM	O	Analog	RFAC summing amplifier output.

Power supply	Pin No.	Symbol	I/O		Description
RFamp 3.3V	35	EQ_IN	I		Equalizer circuit input.
	36	LD	O		APC amplifier output.
	37	PD	I		APC amplifier input.
	38	NC	—	—	
	39	RFC	I		Equalizer cut-off frequency adjustment pin.
	40	$AV_{SS}4$	—	—	Analog GND.
	41	RFACO	O		RFAC signal output.
ASYM 3.3V	42	RFACI	I		RFAC signal input or EFM signal input.
	43	$AV_{DD}3$	—	—	Analog power supply.
	44	BIAS	I		Asymmetry circuit constant current input.
	45	ASYI	I		Asymmetry comparator voltage input.
	46	ASYO	O	1, 0	EFM full-swing output. (Low = V_{SS}, High = V_{DD})
	47	VPCO	O	1, Z, 0	Wide-band EFM PLL charge pump output.
	48	VCTL	I		Wide-band EFM PLL VCO2 control voltage input.
	49	$AV_{SS}3$	—	—	Analog GND.
	50	CLTV	I		Multiplier VCO1 control voltage input.
	51	FILO	O	Analog	Master PLL (slave = digital PLL) filter output.
	52	FILI	I		Master PLL filter input.
	53	PCO	O	1, Z, 0	Master PLL charge pump output.
DC/DC 3.3V	54	$AV_{DD}5$	—	—	Analog power supply.
	55	DDVROUT	O		DC/DC converter output. Leave open when not using.
	56	DDVRSEN	I		DC/DC converter output voltage monitor pin. Connect to analog power supply when not using.
	57	$AV_{SS}5$	—	—	Analog GND.
	58	DDCR	I		Test pin. Normally GND.
—	59	NC	—	—	
Digital I/O = 3.3V Internal = 2.5V	60	BCKI	I		D/A interface bit clock input.
	61	PCMDI	I		D/A interface serial data input. (2's COMP, MSB first)
	62	LRCKI	I		D/A interface LR clock input.
	63	LRCK	O	1, 0	D/A interface LR clock output. f = Fs
	64	V_{SS}	—	—	Internal digital GND.
	65	PCMD	O	1, 0	D/A interface serial data output. (2's COMP, MSB first)
	66	BCK	O	1, 0	D/A interface bit clock output.
	67	V_{DD}	—	—	Internal digital power supply.
	68	EMPH	O	1, 0	High when the playback disc has emphasis, low it has not.
	69	EMPHI	I		High when de-emphasis is ON, low when input OFF.

Power supply	Pin No.	Symbol	I/O		Description
Digital I/O = 3.3V Internal = 2.5V	70	$IOV_{DD}2$	—	—	I/O digital power supply.
	71	DOUT	O	1, 0	Digital Out output.
	72	TEST	I		Test pin. Normally GND.
	73	TES1	I		Test pin. Normally GND.
	74	IOVss2	—	—	I/O digital GND.
—	75	NC	—	—	
X'tal 2.5V	76	XV_{SS}	—	—	Master clock GND.
	77	XTAO	O		Crystal oscillation circuit output.
	78	XTAI	I		Crystal oscillation circuit input.
	79	XV_{DD}	—	—	Master clock power supply.
Lch 3.3V	80	$AV_{DD}1$	—	—	Analog power supply.
	81	AOUT1	O		Lch analog output.
	82	VREFL	O		Lch reference voltage.
	83	$AV_{SS}1$	—	—	Analog GND.
Rch 3.3V	84	$AV_{SS}2$	—	—	Analog GND.
	85	VREFR	O		Rch reference voltage.
	86	AOUT2	O		Rch analog output.
	87	$AV_{DD}2$	—	—	Analog power supply.
—	88	NC	—	—	
Digital I/O = 3.3V Internal = 2.5V	89	$IOV_{DD}0$	—	—	I/O digital power supply.
	90	RMUT	O	1, 0	Rch "0" detection flag.
	91	LMUT	O	1, 0	Lch "0" detection flag.
	92	NC	—	—	
	93	XTSL	I		Crystal selection input. Low when the crystal is 16.9344MHz; high when the crystal is 33.8688MHz.
	94	$IOV_{SS}0$	—	—	I/O digital GND.
	95	XTACN	I		Oscillation circuit control. Self-oscillation when high, oscillation stop when low.
	96	SQSO	O	1, 0	Subcode Q 80-bit and PCM peak and level data output. CD TEXT data output.
	97	SQCK	I		SQSO readout clock input.
	98	SBSO	O	1, 0	Subcode P to W serial output.
	99	EXCK	I		SBSO readout clock input.
	100	XRST	I		System reset. Reset when low.
	101	SYSM	I		Mute input. Muted when high.
	102	DATA	I		Serial data input from CPU.
	103	V_{SS}	—	—	Internal digital GND.
	104	XLAT	I		Latch input from CPU. The serial data is latched at the falling edge.

Power supply	Pin No.	Symbol	I/O		Description
Digital I/O = 3.3V Internal = 2.5V	105	CLOK	I		Serial data transfer clock input from CPU.
	106	V_{DD}	—	—	Internal digital power supply.
	107	SENS	O	1, 0	SENS output to CPU.
	108	SCLK	I		SENS serial data readout clock input.
	109	ATSK	I/O	1, 0	Anti-shock input/output.
	110	WFCK	O	1, 0	WFCK output.
	111	XUGF	O	1, 0	XUGF output. Output MNT0, RFCK, SOUT by command switch.
	112	XPCK	O	1, 0	XPCK output. Output MNT1, SOCK by command switch.
	113	GFS	O	1, 0	GFS output. Output MNT2, XROF, XOLT by command switch.
	114	C2PO	O	1, 0	C2PO output. Output MNT3, GTOP by command switch.
	115	SCOR	O	1, 0	High output when the subcode sync, S0 or S1, is detected.
	116	V_{DD}	—	—	Internal digital power supply.
	117	C4M	O	1, 0	4.2336MHz output. 1/4 frequency-division output of the V16M in CAV-W mode and variable pitch mode.
	118	WDCK	O	1, 0	Word clock output. f = 2Fs. GRSCOR output by command switch.
	119	COUT	I/O	1, 0	Track number count signal input/output.
	120	NC	—	—	

Notes)

- PCMD is a MSB first, two's complement output.
- GTOP is used to monitor the frame sync protection status. (High: sync protection window released.)
- XUGF is the frame sync obtained from the EFM signal, and is negative pulse. It is the signal before sync protection.
- XPCK is the inverse of the EFM PLL clock. The PLL is designed so that the falling edge and the EFM signal transition point coincide.
- The GFS signal goes high when the frame sync and the insertion protection timing match.
- RFCK is derived from the crystal accuracy, and has a cycle of 136µs.
- C2PO represents the data error status.
- XROF is generated when the 32K RAM exceeds the ±28 frame jitter margin.
- C4M is a 4.2336MHz output that changes in CAV-W mode and variable pitch mode.
- FSTO is the 2/3 frequency-division output of the XTAI pin.
- SOUT is the serial data output inside the servo block.
- SOCK is the serial data readout clock output inside the servo block.
- XOLT is the serial data latch output inside the servo block.

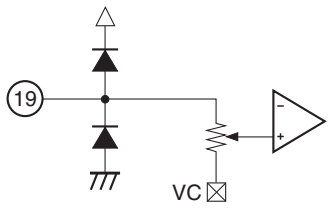
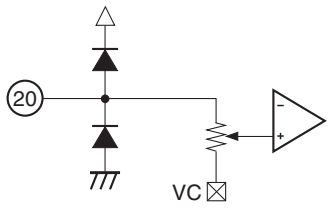
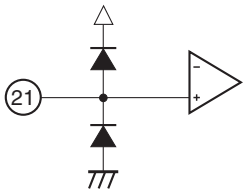
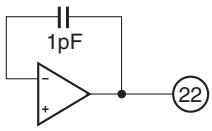
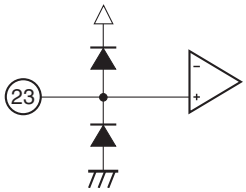
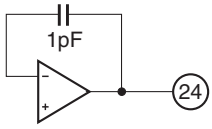
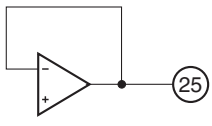
Monitor Pin Output Combinations

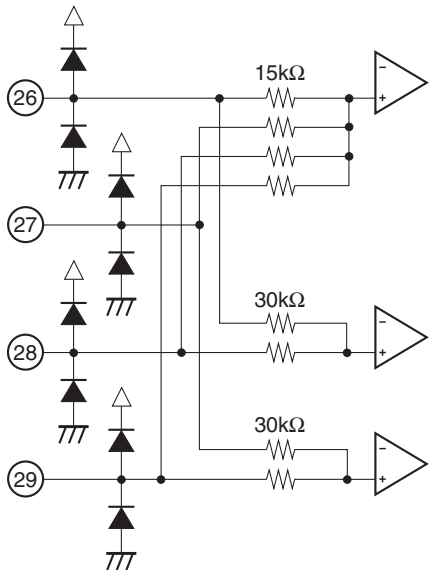
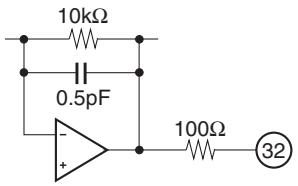
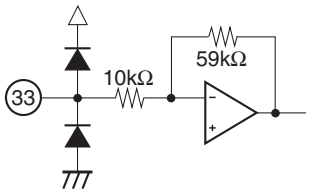
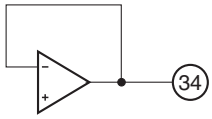
Command bit			Output data			
SRO1	MTSL1	MTSL0				
0	0	0	XUGF	XPCK	GFS	C2PO
0	0	1	MNT0	MNT1	MNT2	MNT3
0	1	0	RFCK	XPCK	XROF	GTOP
0	1	1	C4M	GSTO	GFS	C2PO
1	0	0	SOUT	SOCK	XOLT	C2PO

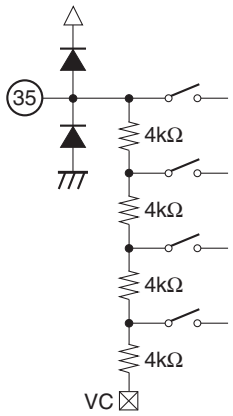
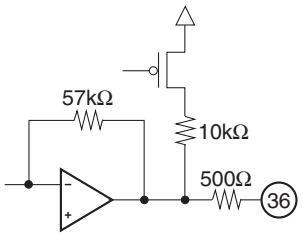
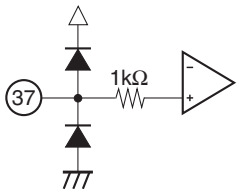
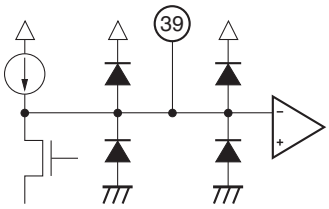
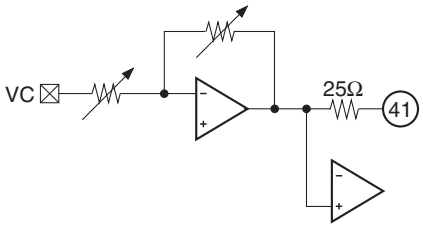
Reset Timing when Power on

Power on with XRST pin low.
Set XRST pin high after holding it low 100ns or more to cancel reset.

RF Block Pin Equivalent Circuit

Pin No.	Symbol	I/O	Equivalent circuit	Description
19	E	I		Tracking error amplifier input.
20	F	I		
21	TEI	I		Tracking error signal input to DSSP block.
22	TEO	O		Tracking error amplifier output.
23	FEI	I		Focus error signal input to DSSP block.
24	FEO	O		Focus error amplifier output.
25	VC	I/O		($AV_{DD}4$ – $AV_{SS}4$)/2 voltage output.

Pin No.	Symbol	I/O	Equivalent circuit	Description
26	A	I		RF summing amplifier and focus error amplifier input.
27	B	I		
28	C	I		
29	D	I		
30	NC	—	—	—
31	$AV_{DD}4$	—	—	Analog power supply.
32	RFDCO	I/O		RFDC amplifier output.
33	PDSENS	I		APC amplifier reference voltage (GND signal) input.
34	AC_SUM	O		RFAC summing amplifier output.

Pin No.	Symbol	I/O	Equivalent circuit	Description
35	EQ_IN	I		Equalizer circuit input.
36	LD	O		APC amplifier output.
37	PD	I		APC amplifier input.
38	NC	—	—	—
39	RFC	I		Equalizer cut-off frequency adjustment.
40	AVSS4	—	—	Analog GND.
41	RFACO	O		RFAC amplifier output.

Electrical Characteristics

1. DC Characteristics

(V_{DD} = XV_{DD} = 2.5 ± 0.2V, IOV_{DD}0 to 2 = AV_{DD}0 to 5 = 3.3 ± 0.3V, V_{SS} = XV_{SS} = IOV_{SS} = AV_{SS} = 0V, Topr = –40 to +85°C)

Item			Conditions	Min.	Typ.	Max.	Unit	Applicable pins
Input voltage (1)	High level input voltage	V_{IH} (1)		0.7V_{DD}			V	*1, *3, *9
	Low level input voltage	V_{IL} (1)				0.2V_{DD}		
Input voltage (2)	High level input voltage	V_{IH} (2)	Schmitt input	0.7V_{DD}			V	*2
	Low level input voltage	V_{IL} (2)				0.2V_{DD}		
	Hysteresis	Vt_+ – Vt_-			0.5			
Input voltage (3)	Input voltage	V_{IN} (3)	Analog input	V_{SS}		V_{DD}	V	*4, *12
Output voltage (1)	High level output voltage	V_{OH} (1)	I_{OH} = –2.4mA	V_{DD} – 0.4			V	*5, *8, *9
	Low level output voltage	V_{OL} (1)	I_{OL} = 4mA			0.4		
Output voltage (2)	High level output voltage	V_{OH} (2)	I_{OH} = –1.2mA	V_{DD} – 0.4			V	*6
	Low level output voltage	V_{OL} (2)	I_{OL} = 2mA			0.4		
Output voltage (3)	High level output voltage	V_{OH} (3)	I_{OH} = –2.4, –4.8, –7.2, –9.6mA	V_{DD} – 0.4			V	*7
	Low level output voltage	V_{OL} (3)	I_{OL} = 4, 8, 12, 16mA			0.4		
Output voltage (4)	High level output voltage	V_{OH} (4)	I_{OH} = –0.28mA	V_{DD} – 0.4			V	*11
	Low level output voltage	V_{OL} (4)	I_{OL} = 0.36mA			0.4		
Input leak current		I_I	V_{IN} = V_{SS} or V_{DD}	–10		10	µA	*1, *2, *9
Input leak current (with pull-down resistor)		I_{IH}	V_{IN} = V_{DD}	40	100	240	µA	*3
Tri-state output leak current (when high impedance)		I_{OZ}	V_{IN} = V_{SS} or V_{DD}	–10		10	µA	*8

Applicable pins

*1 PCMDI, EMPHI, TEST, TES1, XTSL, XTACN, SYSM, DATA

*2 BCKI, LRCKI, SQCK, EXCK, XRST, XLAT, CLOK, SCLK

*3 SSTP

*4 E, F, TEI, FEI, A, B, C, D, PDSENS, EQ_IN, PD, RFC, RFACI, BIAS, ASYI, VCTL, CLTV, FILI, DDVRSEN, DDCR

*5 SFDR, SRDR, TFDR, TRDR, FFDR, FRDR, LRCK, PCMD, BCK, EMPH, RMUT, LMUT, SQSO, SBSO, WFCK, XUGF, XPCK, GFS, C2PO, SCOR, C4M, WDCK

*6 ASYO

*7 DOUT

*8 MDP, VPCO, PCO, SENS

*9 MIRR, DFCT, FOK, LOCK, ATSK, COUT

*10 TEO, FEO, AC_SUM, LD, RFACO, DDVROUT, AOUT1, VREFL, VREFR, AOUT2

*11 FILO

*12 VC, RFDCO

2. AC Characteristics

(1) XTAI pin

(a) When using self-oscillation

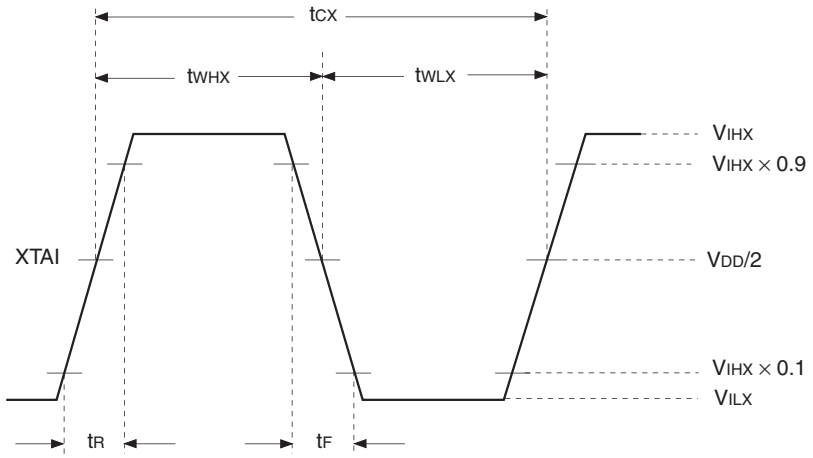
(V_{DD} = XV_{DD} = 2.5 ± 0.2V, IOV_{DD}0 to 2 = AV_{DD}0 to 5 = 3.3 ± 0.3V, V_{SS} = XV_{SS} = IOV_{SS} = AV_{SS} = 0V, Topr = –40 to +85°C)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Oscillation frequency	f_{MAX}	XTSL = L, $AEXX1 CKSL (1, 0) = 00	16.8	16.9344	17.1	MHz
		XTSL = H, $AEXX1 CKSL (1, 0) = 00	33.5	33.8688	34.2	
		XTSL = H, $AEXX1 CKSL (1, 0) = 01 or 10 or 11	67.1	67.7376	68.4	

(b) When inputting pulses to XTAI pin

(V_{DD} = XV_{DD} = 2.5 ± 0.2V, IOV_{DD}0 to 2 = AV_{DD}0 to 5 = 3.3 ± 0.3V, V_{SS} = XV_{SS} = IOV_{SS} = AV_{SS} = 0V, Topr = –40 to +85°C)

Item	Symbol	Min.	Typ.	Max.	Unit
High level pulse width	t_{WHX}	6.6		32.7	ns
Low level pulse width	t_{WLX}	6.6		32.7	ns
Pulse cycle	t_{CX}	14.6		59.5	ns
Input high level	V_{IHX}	1.7			V
Input low level	V_{ILX}			0.7	V
Rise time, fall time	t_R, t_F	0		10	ns



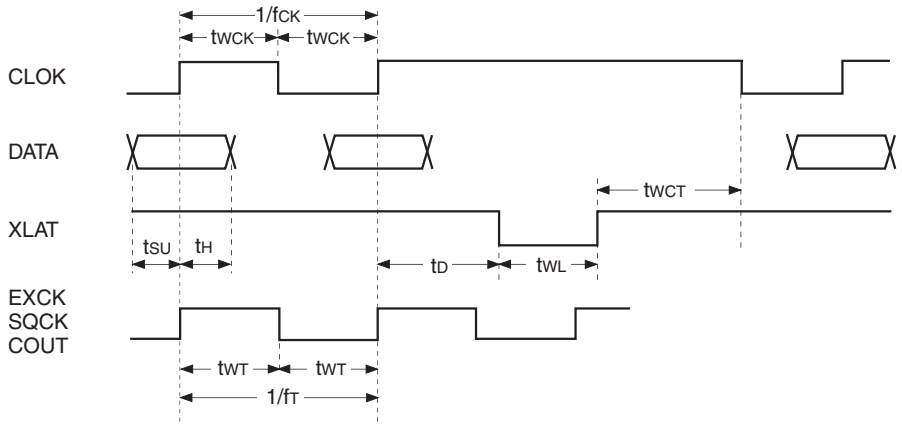
Note) When the pulse is input to the XTAI pin, be sure to input it via the capacitor.

(2) CLOK, DATA, XLAT, SQCK and EXCK pins

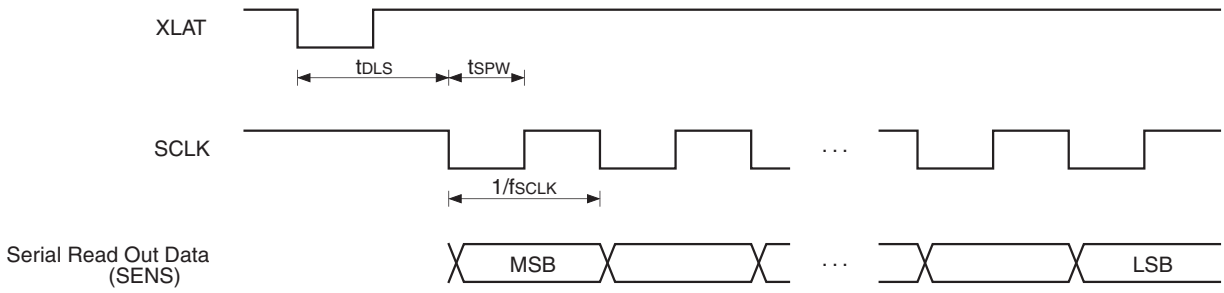
(V_{DD} = XV_{DD} = 2.5 ± 0.2V, $IOV_{DD}0$ to 2 = $AV_{DD}0$ to 5 = 3.3 ± 0.3V, V_{SS} = XV_{SS} = IOV_{SS} = AV_{SS} = 0V, Topr = –40 to +85°C)

Item	Symbol	Min.	Typ.	Max.	Unit
Clock frequency	f_{CK}			16	MHz
Clock pulse width	t_{WCK}	31.3		30000	ns
Setup time	t_{SU}	30			ns
Hold time	t_H	30			ns
Delay time	t_D	300		30000	ns
Latch pulse width	t_{WL}	750			ns
Command transfer interval	t_{WCT}	750			ns
EXCK frequency	f_T			0.65	MHz
EXCK pulse width	t_{WT}	750			ns
SQCK frequency	f_T			0.65	MHz
SQCK pulse width	t_{WT}	750		120000	ns
COUT frequency (during input)*	f_T			65	kHz
COUT pulse width (during input)*	f_{WT}	7.5			µs

* Only when $44 and $45 are executed.



(3) SCLK pin



(V_{DD} = XV_{DD} = 2.5 ± 0.2V, IOV_{DD}0 to 2 = AV_{DD}0 to 5 = 3.3 ± 0.3V, V_{SS} = XV_{SS} = IOV_{SS} = AV_{SS} = 0V, Topr = –40 to +85°C)

Item	Symbol	Min.	Typ.	Max.	Unit
SCLK frequency	f_{SCLK}			16	MHz
SCLK pulse width	t_{SPW}	31.3			ns
Delay time	t_{DLS}	15			µs

(4) COUT, MIRR and DFCT pins

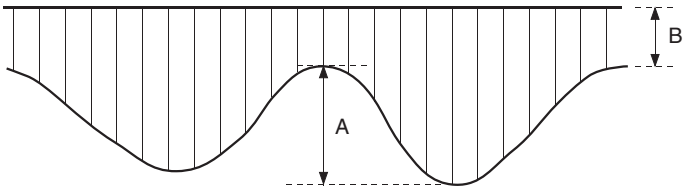
Operating frequency

(V_{DD} = XV_{DD} = 2.5 ± 0.2V, IOV_{DD}0 to 2 = AV_{DD}0 to 5 = 3.3 ± 0.3V, V_{SS} = XV_{SS} = IOV_{SS} = AV_{SS} = 0V, Topr = –40 to +85°C)

Item	Symbol	Min.	Typ.	Max.	Unit	Conditions
COUT maximum operation frequency	f_{COUT}	40			kHz	*1
MIRR maximum operation frequency	f_{MIRR}	40			kHz	*2
DFCT maximum operation frequency	f_{DFCTH}	5			kHz	*3

*1 When using a high-speed traverse TZC

*2



When the RF signal continuously satisfies the following conditions during the traverse.

- A = 0.11V_{DD} to 0.23V_{DD}
- $\frac{B}{A + B} \leq 25\%$

*3 During complete RF signal omission.
When settings related to DFCT signal generation are Typ.

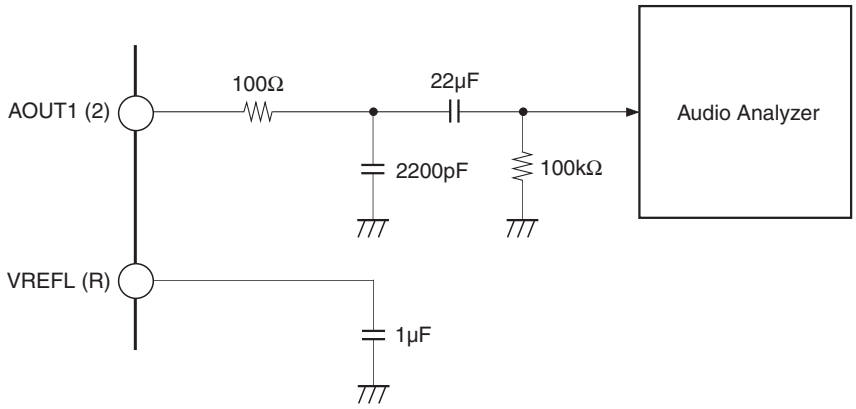
1-bit DAC and LPF Block Analog Characteristics

(V_{DD} = XV_{DD} = 2.5V, IOV_{DD}0 to 2 = AV_{DD}0 to 5 = 3.3V, V_{SS} = XV_{SS} = IOV_{SS} = AV_{SS} = 0V, Topr = +25°C)

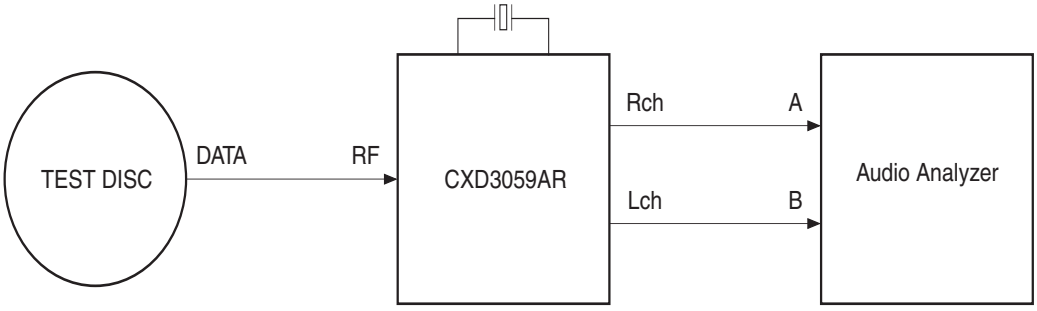
Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Total harmonic distortion	THD	1kHz sine wave, 0dB data, 20kHz LPF		0.006	0.014	%
Signal-to-noise ratio	S/N	1kHz sine wave, 0dB data, AMUT OFF (Using A-weighting filter 20kHz LPF)	90	95		dB

Fs = 44.1kHz in all cases.

The total harmonic distortion and signal-to-noise ratio measurement circuits are shown below.



LPF external circuit diagram



Block diagram of analog characteristics measurement

(V_{DD} = XV_{DD} = 2.5V, IOV_{DD}0 to 2 = AV_{DD}0 to 5 = 3.3V, V_{SS} = XV_{SS} = IOV_{SS} = AV_{SS} = 0V, Topr = +25°C)

Item	Symbol	Min.	Typ.	Max.	Unit	Applicable pins
Output voltage	V_{OUT}	920	928		mVrms	*1
Load resistance	R_L	10			kΩ	*1
VREF pin capacitance	C_{VREF}		1		µF	*2

* Measurement is conducted for the above circuit diagrams with the sine wave output of 1kHz and 0dB.

Applicable pins

*1 AOUT1, AOUT2

*2 VREFL, VREFR

RF Block Electrical Characteristics

(V_{DD} = XV_{DD} = 2.5V, IOV_{DD}0 to 2 = AV_{DD}0 to 5 = 3.3V, V_{SS} = XV_{SS} = IOV_{SS} = AV_{SS} = 0V, Topr = +25°C)

Measurement item		Symbol	SW conditions	Sending command	Bias conditions				V_{DD}	AV_{DD}	Measurement conditions	Measurement pins	Min.	Typ.	Max.	Unit
					AC input amplitude	AC input frequency	DC input voltage	DC input current								
Input impedance (A, B, C and D)		$R_{A,B,C,D}$	Connect to VC except measurement pins.						2.5V	3.3V	Pin current	A, B, C, D	10	15	20	kΩ
Input impedance (E and F)		$R_{E,F}$									Pin current	E, F	21	30	39	kΩ
Input impedance (PD)		R_{PD}									Pin current	PD	10			MΩ
RF block current consumption (on operation)		I_{AVD}		$3AF100					2.5V	3.3V	Pin current	AV_{DD}4		40	70	mA
RF block current consumption (on standby)		I_{STB}		$ADF7CC00							Pin current	AV_{DD}4			1	mA
VC	Output voltage	V_{VC}						±3mA	2.5V	3.3V	Pin voltage	VC	$0.5AV_{DD}$ – 0.1	$0.5AV_{DD}$	$0.5AV_{DD}$ + 0.1	V
APC	Input voltage	V_{PD}						0	2.5V	3.3V	PD input voltage which LD pin voltage is 1.41V	LD, PD	100	150	200	mV
	Output voltage (on standby)	V_{LD}stb		$AD000800				0			Pin voltage	LD	AV_{DD} – 0.2			V
	Input voltage range	V_{PDT}					V_{PD} + 12mV	0			Pin voltage	LD	1.89	2.14	2.39	V
		V_{PDB}					V_{PD} – 12mV	0			Pin voltage	LD	0.43	0.68	0.93	V
	Maximum output current	I_{LD}					0	1mA			Pin voltage	LD	0.34	0.64	0.94	V
	Output impedance	R_{LD}					V_{PD}	1mA			Pin voltage	LD	1.66	1.91	2.16	V

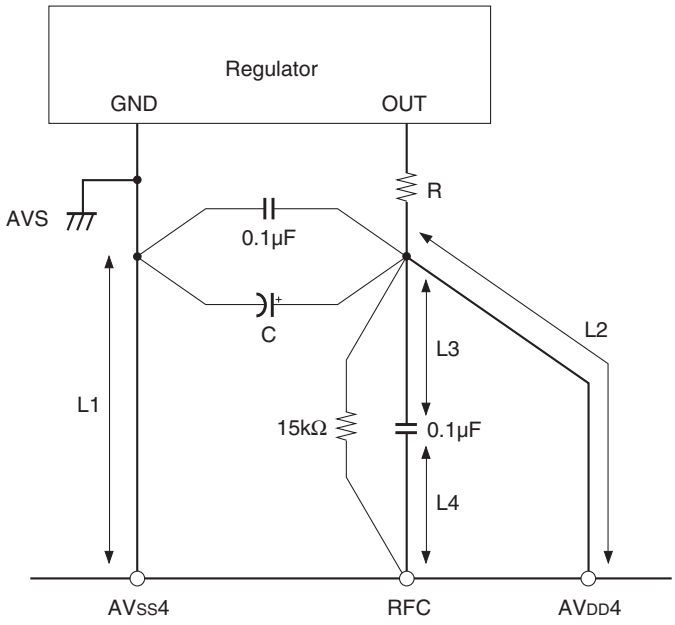
	Measurement item	Symbol	SW conditions	Sending command	Bias conditions				V_{DD}	AV_{DD}	Measurement conditions	Measurement pins	Min.	Typ.	Max.	Unit
					AC input amplitude	AC input frequency	DC input voltage	DC input current								
ACSUM	Input voltage range	$V_{IR\text{-}ACSUM}$							2.5V	3V	Pin voltage, A + B + C + D	RFDC	$0.5AV_{DD}$ – 0.1		$0.9AV_{DD}$ + 0.1	V
	Output voltage range	$V_{OR\text{-}ACSUM}$									Pin voltage	RFDC	$0.47AV_{DD}$		$0.65AV_{DD}$	V
	Input conversion DC offset voltage	$V_{OF\text{-}ACSUM}$		$3AA000							Pin voltage	RFDC	$0.5AV_{DD}$ – 0.23		$0.5AV_{DD}$ + 0.23	V
	Input conversion DC offset temperature drift	$V_{DF\text{-}ACSUM}$		$3AA01C										±6		µV/°C
	Offset voltage	V_{OFFSUM}									Pin voltage	RFDC	0.7	0.9	1.1	V
	Frequency characteristics 1	F_{SUM1}		$3AA004	61mVp-p	0.2/6MHz	VC + VAC1/2				20 log (V6M/V0.2M)	RFDC	–4	0	1	dB
	Frequency characteristics 2	F_{SUM2}		$3AA018	104mVp-p								–4	0	1	dB
	Distortion rate	D_{SUM}			600mVp-p	3MHz		VC + VAC1/2			(V6M/V3M) × 100	RFDC			3	%
RFDC	Input voltage range	$V_{IR\text{-}RFDC}$							2.5V	3V	Pin voltage, A + B + C + D	RFDC	$0.3AV_{DD}$ – 0.1		$0.7AV_{DD}$ + 0.1	V
	Output voltage range	$V_{OR\text{-}RFDC}$									Pin voltage	RFDC	$0.25AV_{DD}$		$0.75AV_{DD}$	V
	Input conversion DC offset voltage	$V_{OF\text{-}RFDC}$		$3AA000							Pin voltage	RFDC	$0.3AV_{DD}$ – 0.23		$0.3AV_{DD}$ + 0.23	V
	Input conversion DC offset temperature drift	$V_{DF\text{-}RFDC}$		$3AA01C										±6		µV/°C
	Frequency characteristics 1	F_{RFDC1}		$3AA004	61mVp-p	0.2/6MHz	VC + VAC1/2				20 log (V6M/V0.2M)	RFDC	–4	0	1	dB
	Frequency characteristics 2	F_{RFDC2}		$3AA018	104mVp-p								–4	0	1	dB
	Distortion rate	D_{RFDC}			1.5Vp-p	100kHz						RFDC		0.1		%

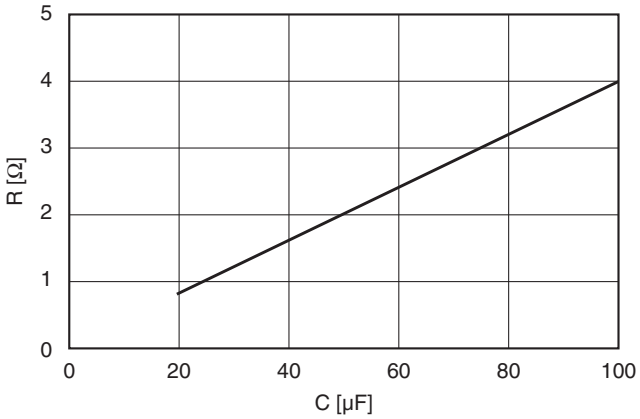
	Measurement item	Symbol	SW conditions	Sending command	Bias conditions				V_{DD}	AV_{DD}	Measurement conditions	Measurement pins	Min.	Typ.	Max.	Unit
					AC input amplitude	AC input frequency	DC input voltage	DC input current								
FE	Input voltage range	$V_{IR\text{-}FE}$							2.5V	3V	VC reference about (B + D) and (A + C)	FE	0.375 AV_{DD}		0.625 AV_{DD}	V
	Output voltage range	$V_{OR\text{-}FE}$									Pin voltage	FE	0.5		AV_{DD} – 0.5	V
	Input conversion DC offset voltage	$V_{OF\text{-}FE}$									Pin voltage	FE	0.5AV_{DD} – 0.03		0.5AV_{DD} + 0.03	V
	Input conversion DC offset temperature drift	$V_{DF\text{-}FE}$												±2.8		µV/°C
	Offset voltage	V_{OFFFE}									Pin voltage	FE	–0.06	0	0.06	V
	Frequency characteristics 1	F_{FE1}		$3AA104	30mVp-p	10/100kHz					20 log (V100k/V10k)	FE	–1	0	1	dB
	Frequency characteristics 2	F_{FE2}		$3AA118	52mVp-p								–1	0	1	dB
	Distortion rate	D_{FE}			600mVp-p	50kHz					(V50k/V100k) × 100	FE			3	%
TE	Input voltage range	$V_{IR\text{-}TE}$							2.5V	3V	VC reference about (B + D) and (A + C)	TE	0.4AV_{DD}		0.6AV_{DD}	V
	Output voltage range	$V_{OR\text{-}TE}$									Pin voltage	TE	0.5		AV_{DD} – 0.5	V
	Input conversion DC offset voltage	$V_{OF\text{-}TE}$									Pin voltage	TE	0.5AV_{DD} – 0.03		0.5AV_{DD} + 0.03	V
	Input conversion DC offset temperature drift	$V_{DF\text{-}TE}$												±2.5		µV/°C
	Offset voltage	V_{OFFTE}									Pin voltage	TE	–0.075	0	0.075	V
	Frequency characteristics 1	F_{TE1}		$3AA204	28mVp-p	10/100kHz					20 log (V100k/V10k)	TE	–1	0	1	dB
	Frequency characteristics 2	F_{TE2}		$3AA218	45mVp-p								–1	0	1	dB
	Distortion rate	D_{TE}		$3AA200	480mVp-p	50kHz					(V50k/V100k) × 100	TE			3	%

Measurement item		Symbol	SW conditions	Sending command	Bias conditions				V_{DD}	AV_{DD}	Measurement conditions	Measure-ment pins	Min.	Typ.	Max.	Unit
					AC input amplitude	AC input frequency	DC input voltage	DC input current								
EQ	Input voltage range	V_{IR-EQ}							2.5V	3V	Distortion rate 3% or less, no DC bias	RFACO			250	mVp-p
	Output voltage range	V_{OR-EQ}									Pin voltage	RFACO	0.5		AV_{DD} – 0.5	V
	Input conversion DC offset voltage	V_{OF-EQ}									Pin voltage	RFACO	–0.25		0.25	V
	Input conversion DC offset temperature drift	V_{DF-EQ}									Ta = –40 to +85°C			±0.1		V
	Offset voltage	V_{OFFEQ}									Pin voltage	RFACO	–0.5	0	0.5	V
	Frequency characteristics 1	F_{EQ1}		$3AA204	28mVp-p	10/ 100kHz					20 log (V100k/V10k)	RFACO	–1	0	1	dB
	Frequency characteristics 2	F_{EQ2}		$3AA218	45mVp-p								–1	0	1	dB
	Distortion rate	D_{EQ}		$3AA200	1.2Vp-p	360kHz					(V720k/V360k) × 100	RFACO			3	%

Notes on Operation for RFC Pin

- Set each impedance of the heavy line shown bellow 0.1Ω or less.
- Make each wiring length of L1 to L4, L1 ≤ 20mm, L2 ≤ 20mm and L3 + L4 ≤ 40mm.
- Use the bypass condenser C with capacitance led by resistance (regulator output impedance and wiring resistance to C) or more seeing the figure bellow.



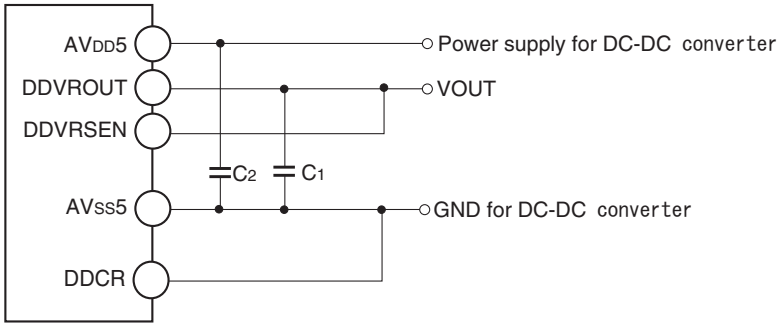


Impedance R tolerance for bypass condenser C

DC-DC Converter Characteristics

(V_{DD} = XV_{DD} = 2.5 ± 0.2V, IOV_{DD}0 to 2 = AV_{DD}0 to 5 = 3.3 ± 0.3V, V_{SS} = XV_{SS} = IOV_{SS} = AV_{SS} = 0V, Topr = –40 to +85°C)

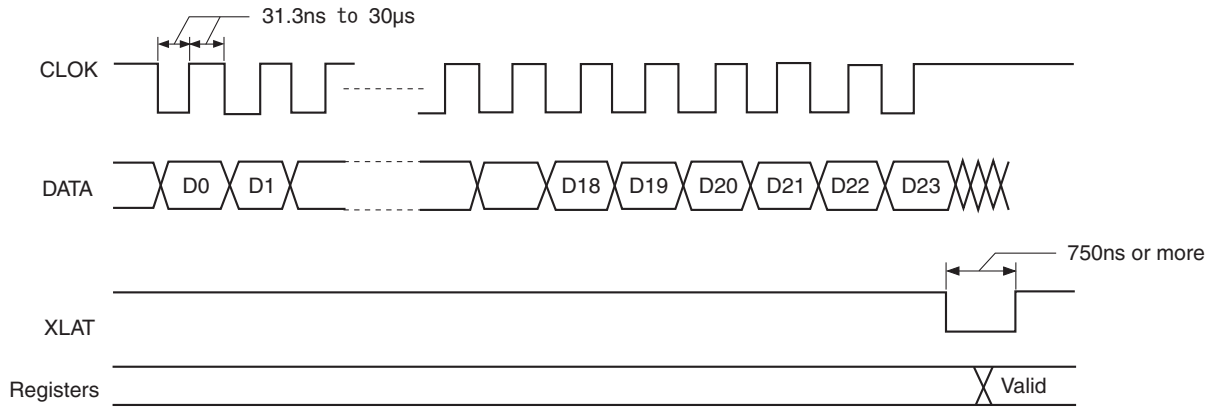
Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Output voltage	V_O	—	2.3	2.5	2.7	V
Output current	Iope	—	—	—	100	mA



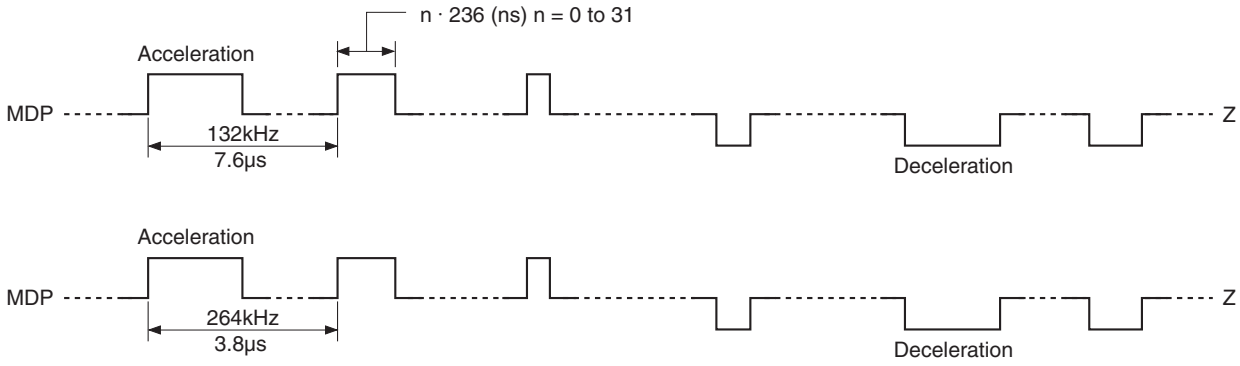
DC-DC converter application circuit sample

Refer to Application Notes on operation.

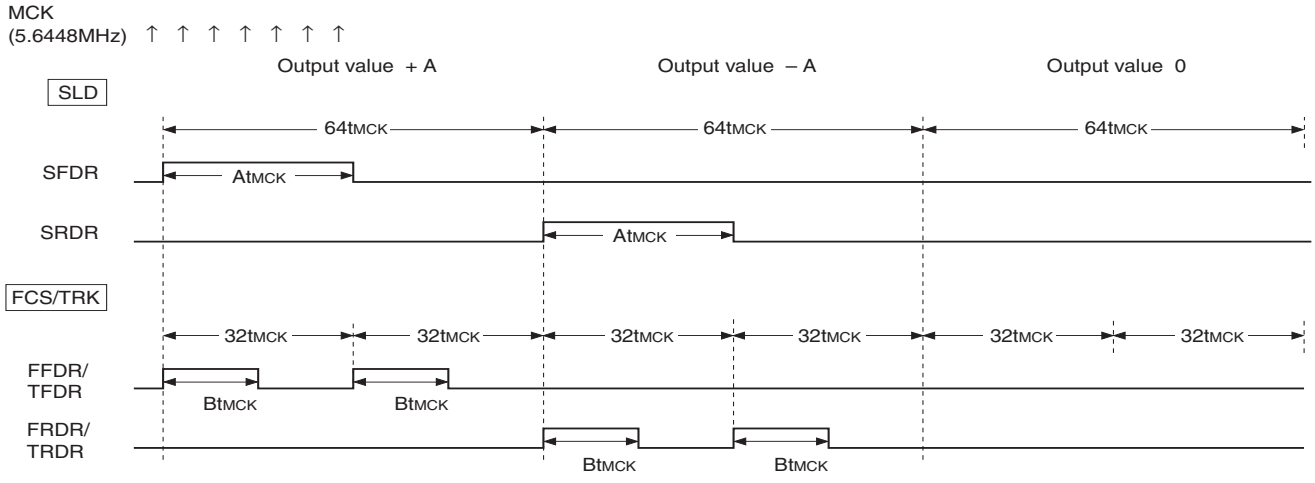
CPU Interface Timing



Spindle Output



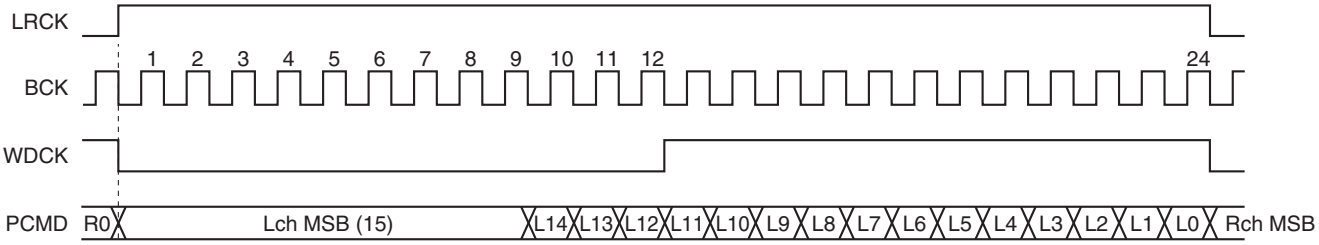
Servo Output



A: 0 to 63 integer number
B: 0 to 31 integer number

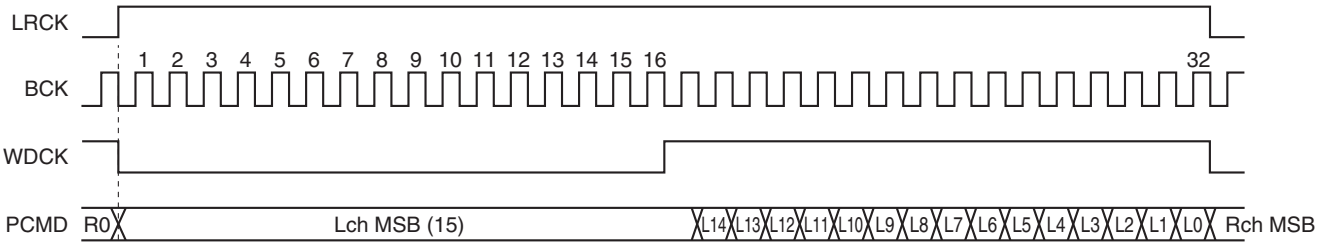
DA Interface

CDDSP output selected (1× speed playback LRCK = 44.1kHz, BCK = 2.1168MHz)

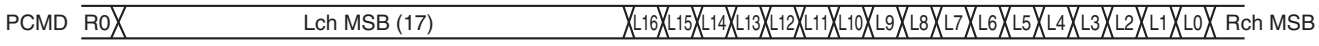


DAC output selected (1× speed playback LRCK = 44.1kHz, BCK = 2.8224MHz)

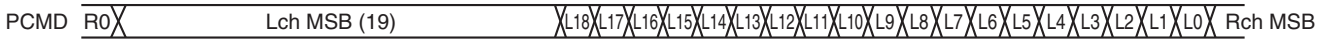
$A5EA OBIT1 = 1, OBIT0 = 1



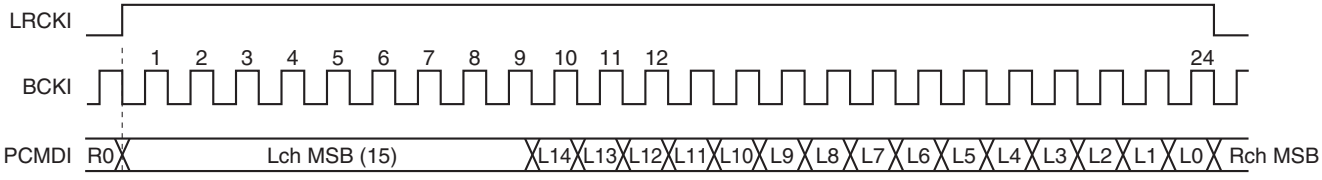
$A5EA OBIT1 = 1, OBIT0 = 0



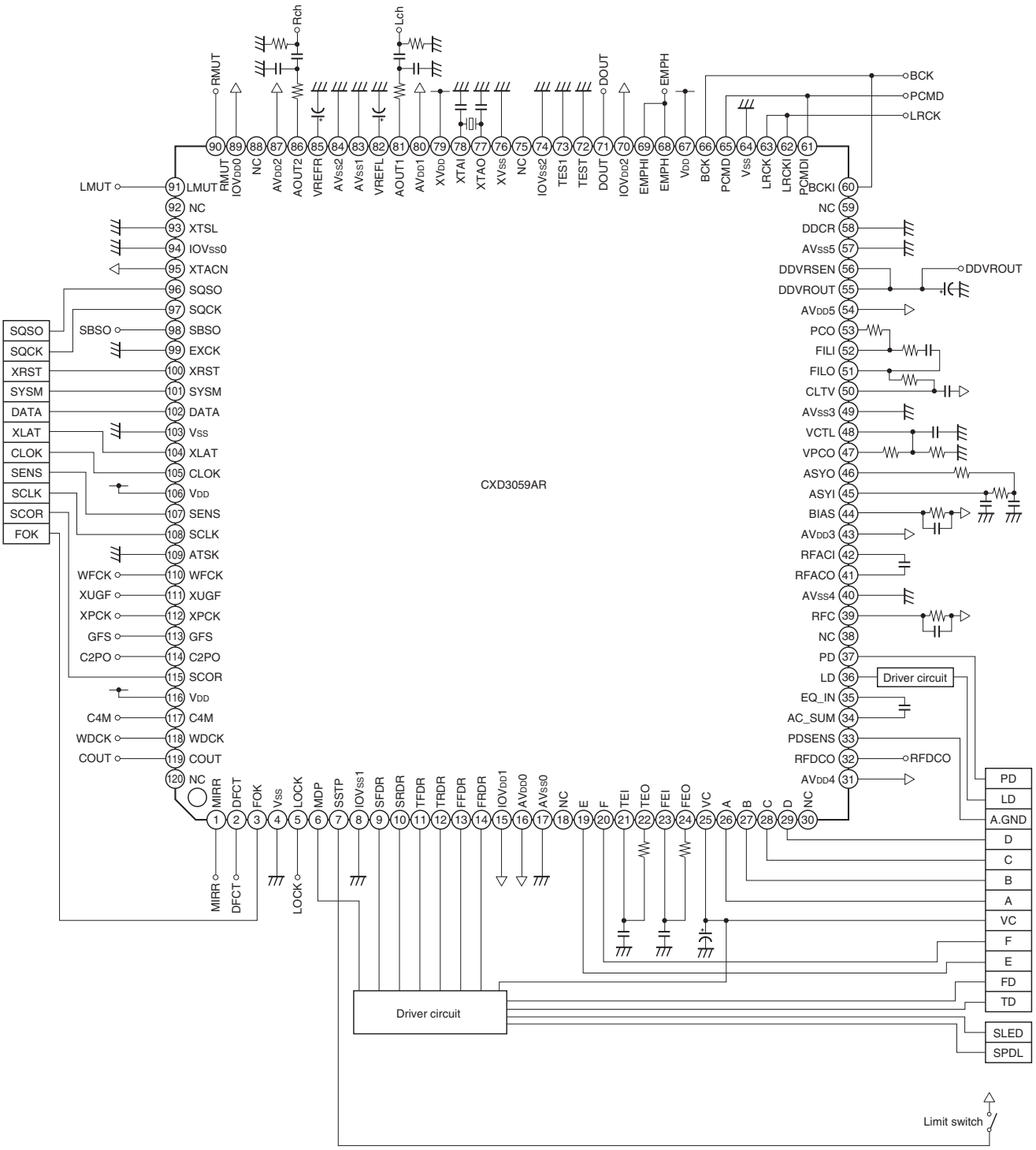
$A5EA OBIT1 = 0, OBIT0 = 0



DAC block input timing (LRCK = 44.1kHz, BCK = 2.1168MHz)



Application Circuit

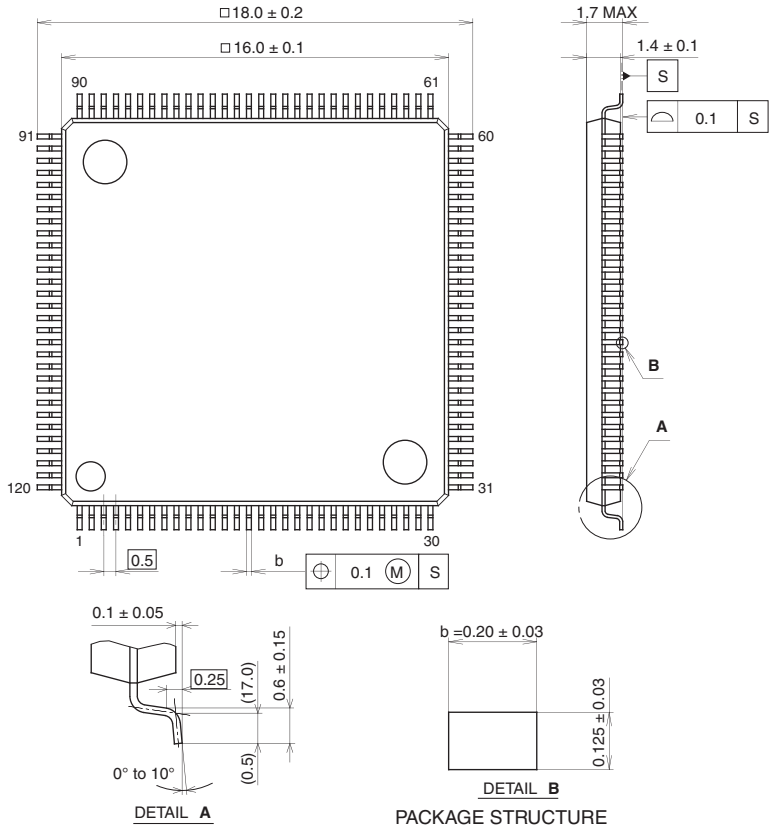


Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Package Outline Unit: mm

Ass'y Plant: Mitsui HT

120PIN LQFP (PLASTIC)



PACKAGE STRUCTURE

SONY CODE	LQFP-120P-L241
EIAJ CODE	P-LQFP120-16x16-0.5
JEDEC CODE	————

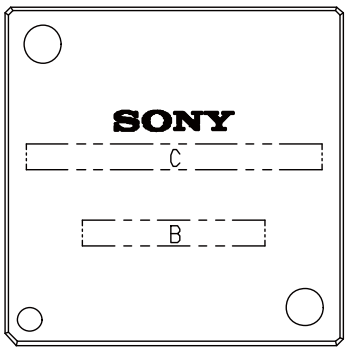
PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	PALLADIUM PLATING
LEAD MATERIAL	COPPER ALLOY
PACKAGE MASS	0.8g

AP-2000-120QX1S

04.02.14

CODE : LQ-120-WD

Marking



MARKING C: CXD3057R

注1) C部は製品名(Max14文字)を配置する. (14文字を越える場合は製品名省略標示規定に従う.)

2) B部はロット番号(Max7文字)を配置する.

< INSTRUCTIONS >

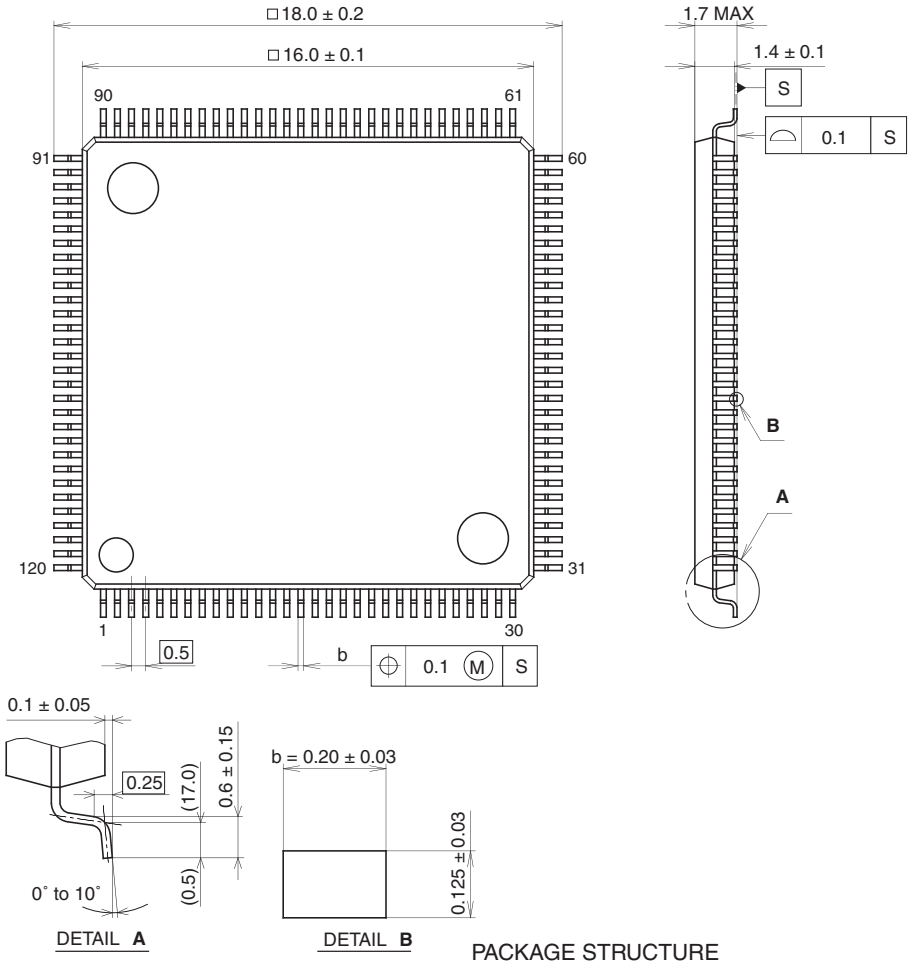
1) TYPE NO. (MAX 14 CHARACTERS) IN SECTION C.
(FOR MORE THAN 14 CHARACTERS FOLLOW RULES FOR ABBREVIATIONS.)

2) LOT NO. (MAX 7 CHARACTERS) IN SECTION B.

Package Outline Unit: mm

Ass'y Plant: SDT

120PIN LQFP (PLASTIC)

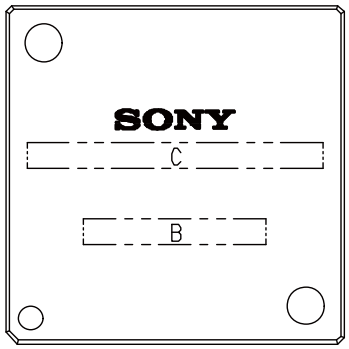


SONY CODE	LQFP-120P-L01
EIAJ CODE	LQFP120-P-1616
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	PALLADIUM PLATING
LEAD MATERIAL	COPPER ALLOY
PACKAGE MASS	0.8g

Marking



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