SONY

Audio DAC + Driver for TV

CXA3803R

Description

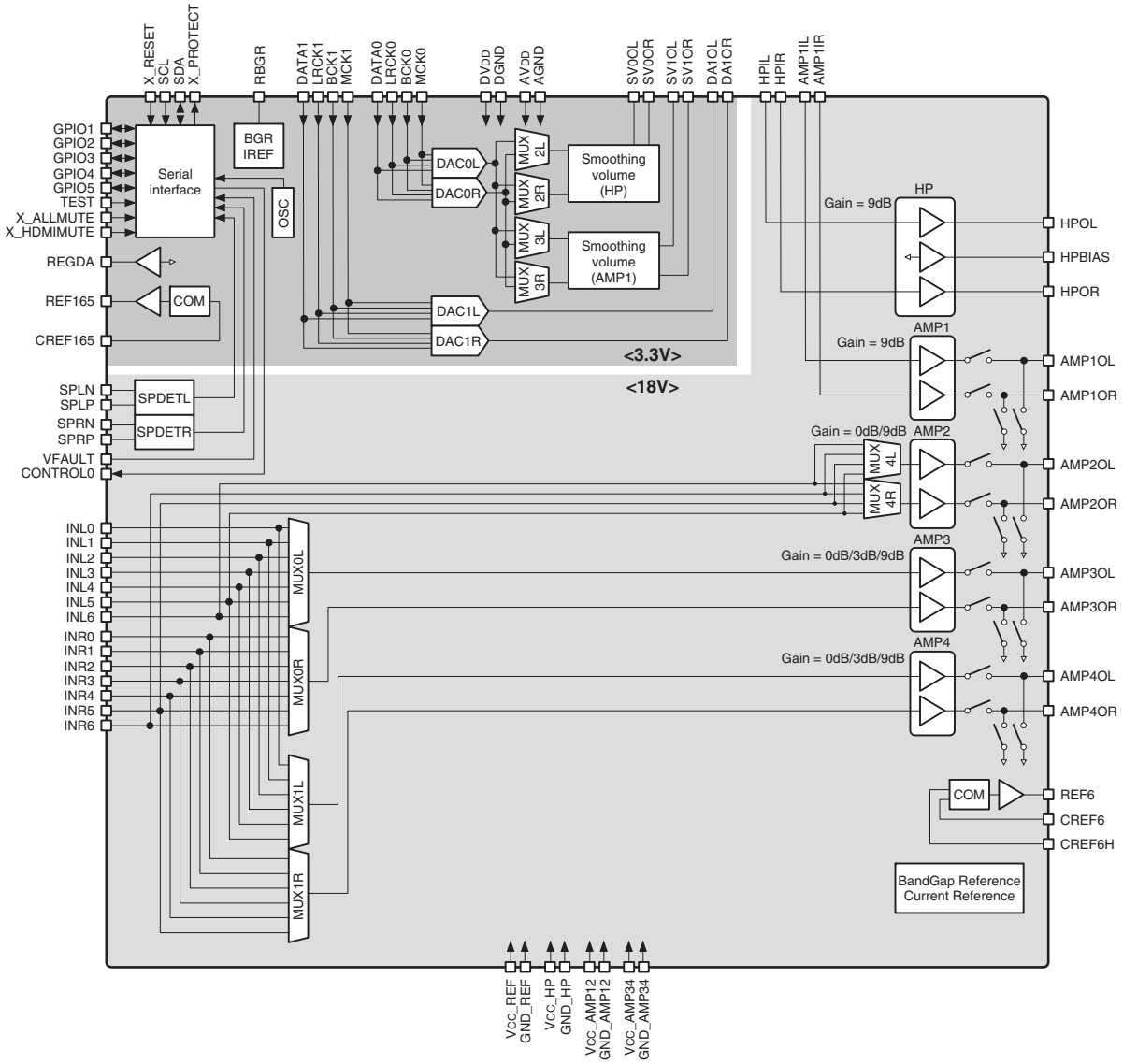
The CXA3803R is a single-chip, 24-bit, 2 stereo, audio digital-to-analog converter (DAC) with headphone amplifier, 4 stereo line amplifiers, clickless stereo volume and speaker short detector.
The 2 stereo DAC supports several common audio sampling rates between 32kHz and 48kHz and 16-/24-/32-bit width digital audio input word on the audio interface. The audio interface of the CXA3803R supports the I²S compatible and left justified MSB first.
The headphone amplifier features cap-less (bias center), a mute control and 2.8Vrms output.
The 4 stereo line amplifiers features pop-noise free power-on/off, a mute control and 2.8Vrms output.
The CXA3803R is provided in a LQFP-80 package with a size of 14mm × 14mm.

Features

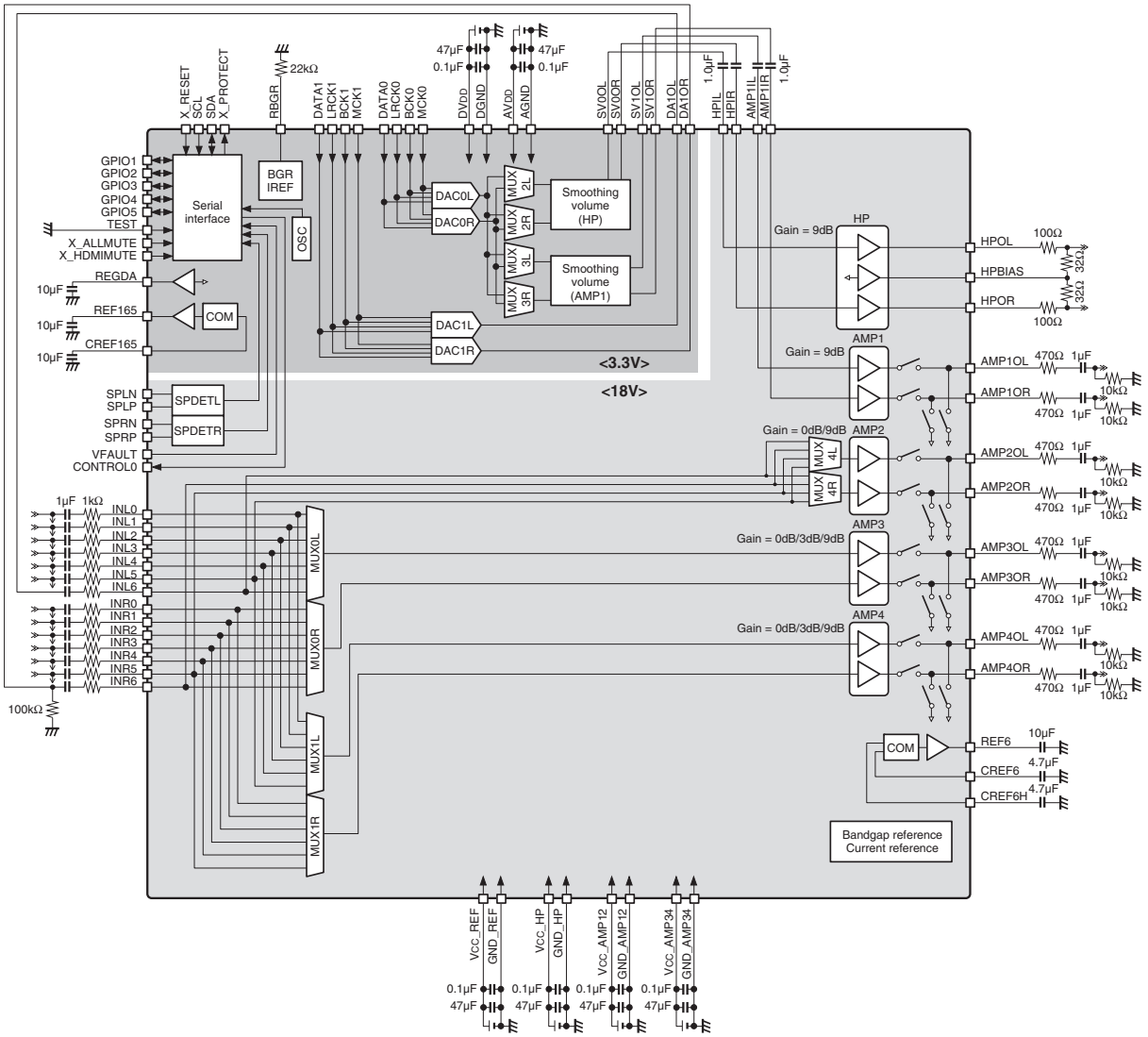
- 24-bit stereo ΔΣDAC
- Sampling rate: 32kHz to 48kHz
- Audio I/F format:
  - I²S compatible, 24-bit MSB first left justified
- Master clock:
  - 256fs/512fs
- Analog smoothing volume control:
  - Headphone: 0dB to –90dB, 0.5dB step
  - Lineout: 0dB to –90dB, 0.5dB step
- 7 stereo input
- I²C high-speed control
- DAC performance:
  - (Lineout) THD+N: 0.02%, output level: 2Vrms
  - (Headphone) THD+N: 0.1%, output level: 2Vrms
- Buffers performance:
  - THD+N: 0.01%, output level: 2Vrms
- Power supply:
  - DAC, digital I/F: 3 to 3.6V
  - Output buffers: 11 to 14V
- Ta: –25 to +85°C
- Package: 80-pin LQFP

E09807A1Z

Block Diagram

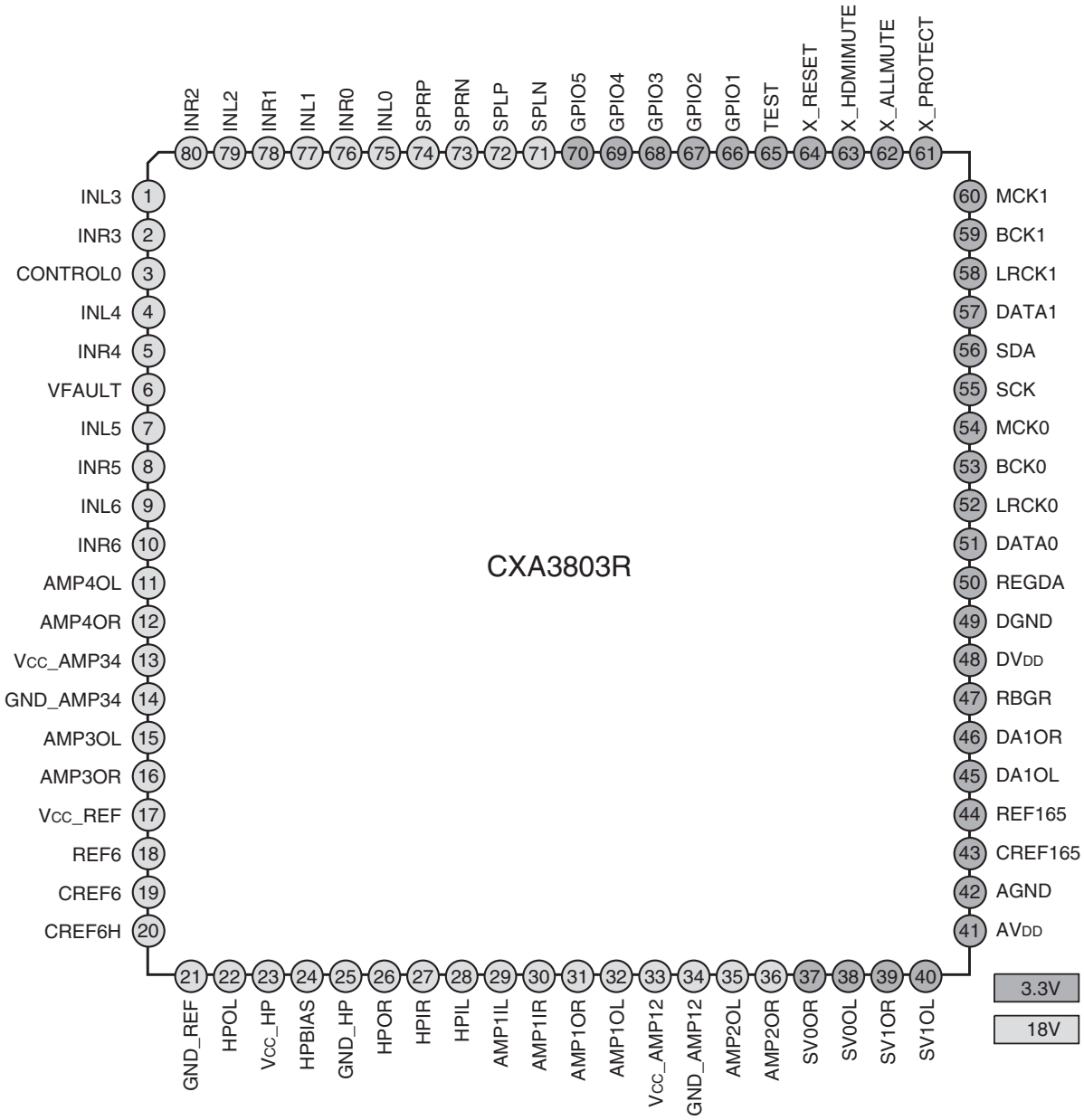


Application Circuit



Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Pin Assignment

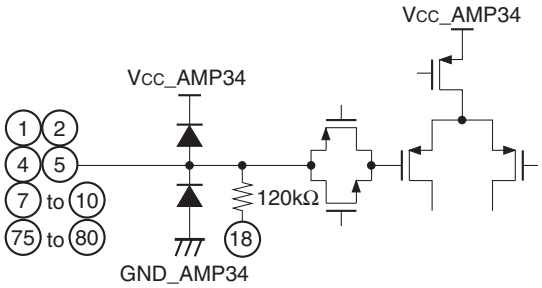
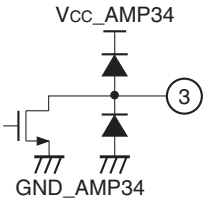
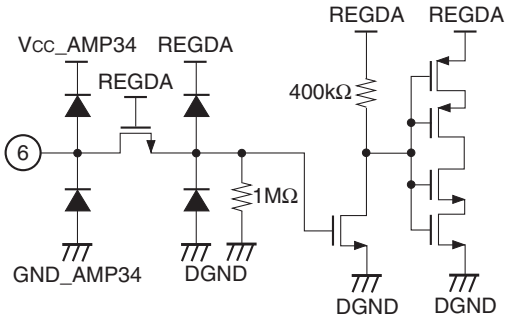
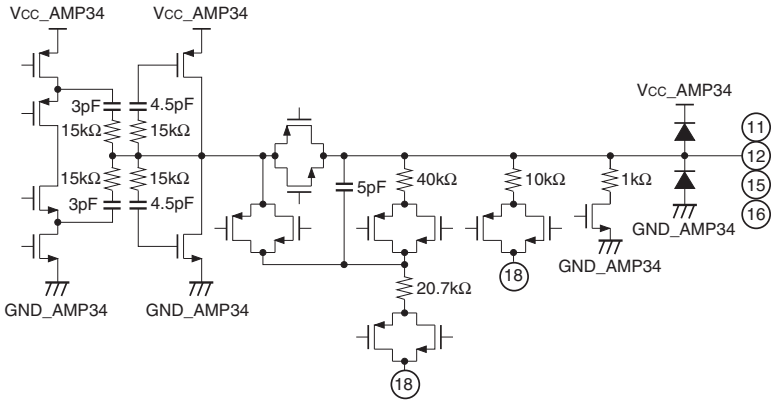


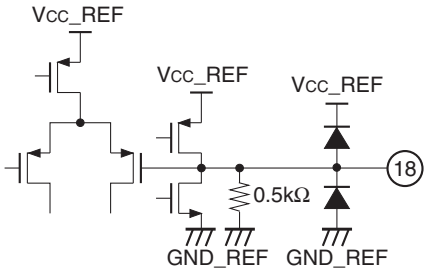
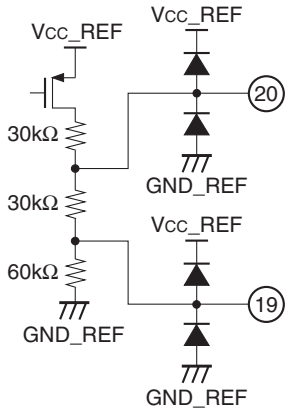
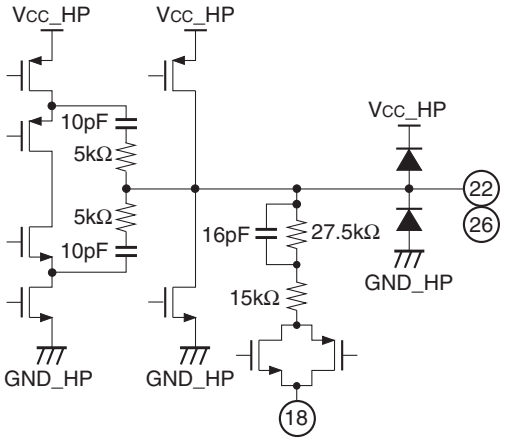
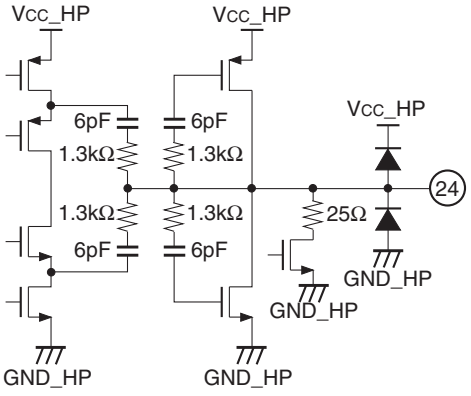
Pin Description

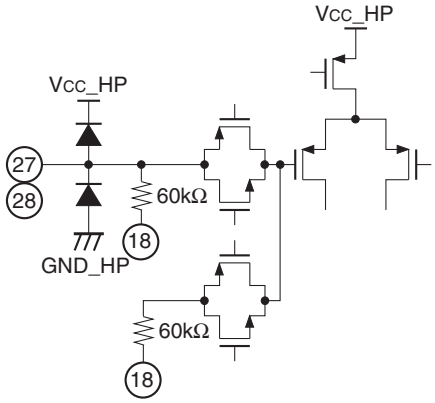
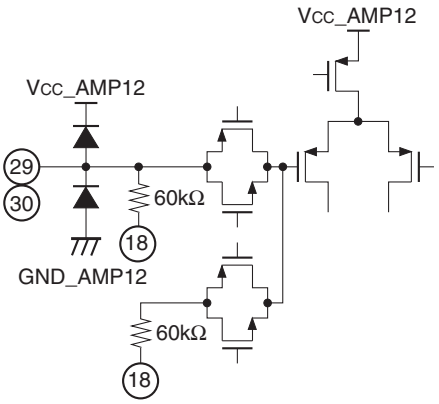
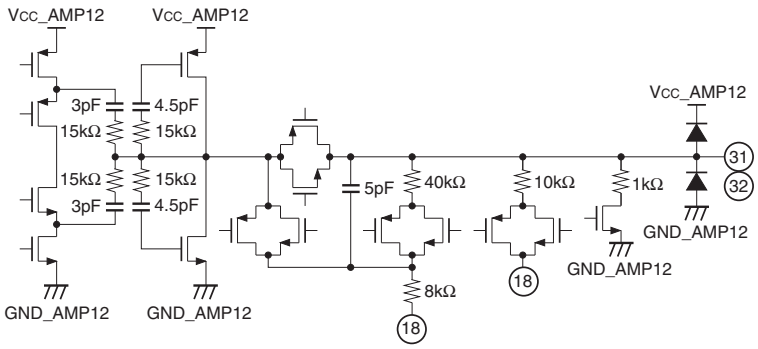
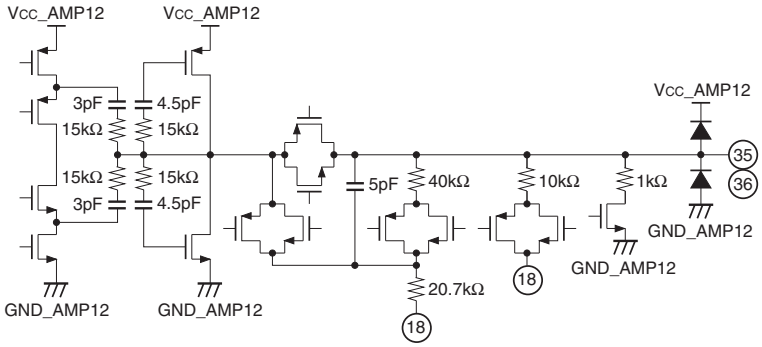
Pin No.	Symbol	I/O	Description
1	INL3	I	MUX0, 1 Lch input 3
2	INR3	I	MUX0, 1 Rch input 3
3	CONTROL0	O	Nch open drain output
4	INL4	I	MUX0, 1 Lch input 4
5	INR4	I	MUX0, 1 Rch input 4
6	VFAULT	I	Fault signal input
7	INL5	I	MUX0, 1 Lch input 5
8	INR5	I	MUX0, 1 Rch input 5
9	INL6	I	MUX0 Lch input 6
10	INR6	I	MUX0 Rch input 6
11	AMP4OL	O	AMP4 Lch output
12	AMP4OR	O	AMP4 Rch output
13	Vcc_AMP34	—	AMP3, 4 power
14	GND_AMP34	—	AMP3, 4 ground
15	AMP3OL	O	AMP3 Lch output
16	AMP3OR	O	AMP3 Rch output
17	Vcc_REF	—	Reference power
18	REF6	O	AMP1-4 and HPAMP reference
19	CREF6	O	Reference capacitor (6V)
20	CREF6H	O	“H” reference capacitor (6V)
21	GND_REF	—	Reference ground
22	HPOL	O	Headphone amp Lch output
23	Vcc_HP	—	Headphone amp power
24	HPBIAS	O	Headphone amp bias output
25	GND_HP	—	Headphone amp ground
26	HPOR	O	Headphone amp Rch output
27	HPIR	I	Headphone amp Rch input
28	HPIL	I	Headphone amp Lch input
29	AMP1IL	I	AMP1 Lch input
30	AMP1IR	I	AMP1 Rch input
31	AMP1OR	O	AMP1 Rch output
32	AMP1OL	O	AMP1 Lch output
33	Vcc_AMP12	—	AMP1, 2 power
34	GND_AMP12	—	AMP1, 2 ground
35	AMP2OL	O	AMP2 Lch output
36	AMP2OR	O	AMP2 Rch output
37	SV0OR	O	Smoothing volume0 Rch output
38	SV0OL	O	Smoothing volume0 Lch output
39	SV1OL	O	Smoothing volume1 Lch output

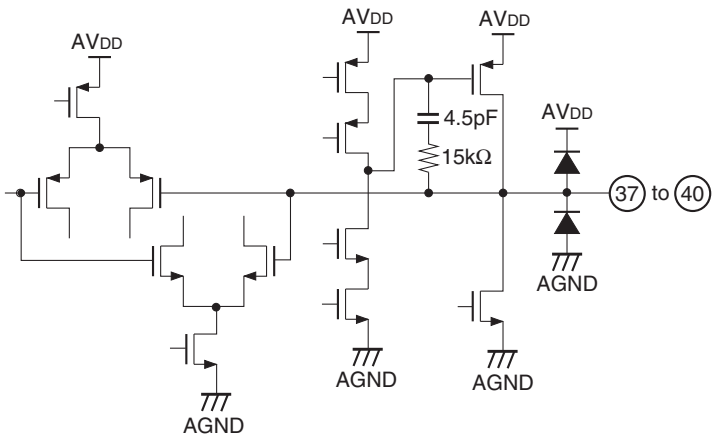
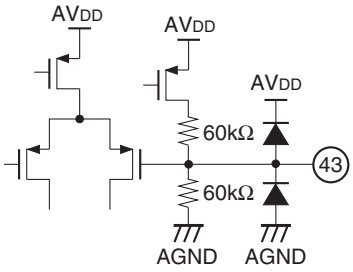
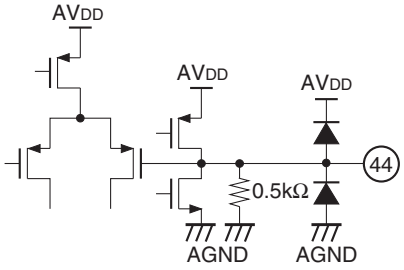
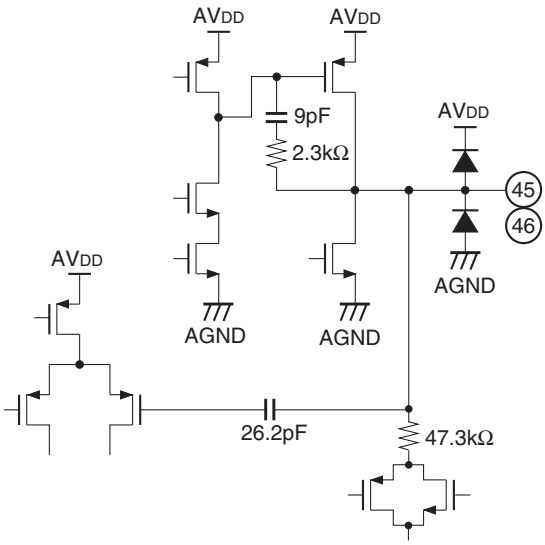
Pin No.	Symbol	I/O	Description
40	SV1OR	O	Smoothing volume1 Lch output
41	AV_{DD}	—	Smoothing volume and DAC power
42	AGND	—	Smoothing volume and DAC ground
43	CREF165	O	Reference capacitor (1.65V)
44	REF165	O	Smoothing volume and DAC reference
45	DA1OL	O	DAC1 Lch output
46	DA1OR	O	DAC1 Rch output
47	RBGR	O	Constan current buffer output
48	DV_{DD}	—	Logic power
49	DGND	—	Logic ground
50	REGDA	O	Regulator output for logic core power
51	DATA0	I	Audio serial data input 0
52	LRCK0	I	L/R clock input 0
53	BCK0	I	Serial bit clock input 0
54	MCK0	I	Master clock input 0
55	SCK	I	I^2C clock
56	SDA	I/O	I^2C data
57	DATA1	I	Audio serial data input 1
58	LRCK1	I	L/R clock input 1
59	BCK1	I	Serial bit clock input 1
60	MCK1	I	Master clock input 1
61	X_PROTECT	O	Protect signal output
62	X_ALLMUTE	I	Mute control input 1
63	X_HDMIMUTE	I	Mute control input 2
64	X_RESET	I	Reset input
65	TEST	I	TEST input
66	GPIO1	I/O	General purpose input/output 1
67	GPIO2	I/O	General purpose input/output 2
68	GPIO3	I/O	General purpose input/output 3
69	GPIO4	I/O	General purpose input/output 4
70	GPIO5	I/O	General purpose input/output 5
71	SPLN	I	Speaker Lch negative input
72	SPLP	I	Speaker Lch positive input
73	SPRN	I	Speaker Rch negative input
74	SPRP	I	Speaker Rch positive input
75	INL0	I	MUX0, 1 Lch input 0
76	INR0	I	MUX0, 1 Rch input 0
77	INL1	I	MUX0, 1 Lch input 1
78	INR1	I	MUX0, 1 Rch input 1
79	INL2	I	MUX0, 1 Lch input 2
80	INR2	I	MUX0, 1 Rch input 2

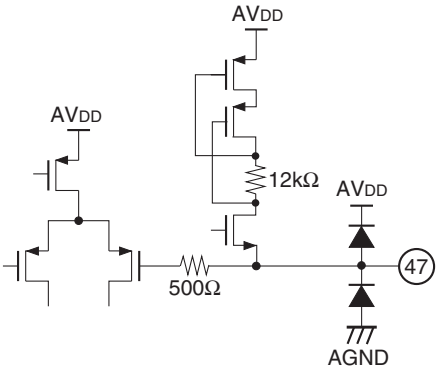
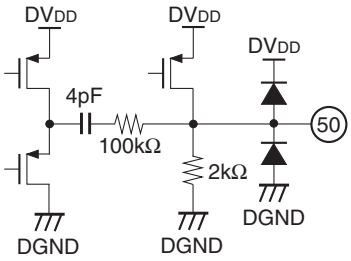
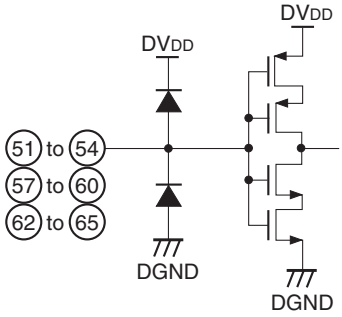
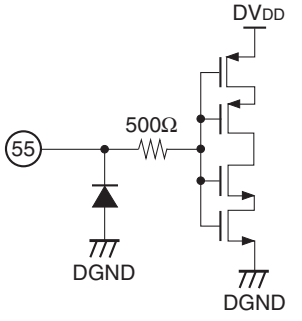
Pin Circuits

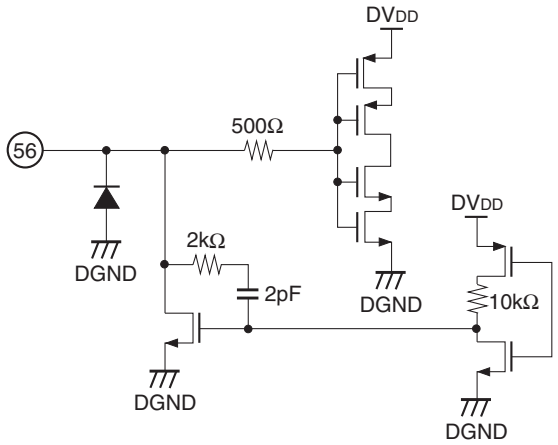
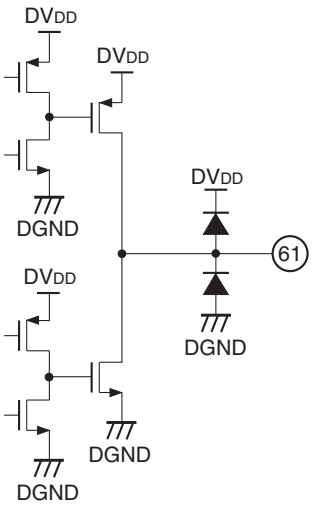
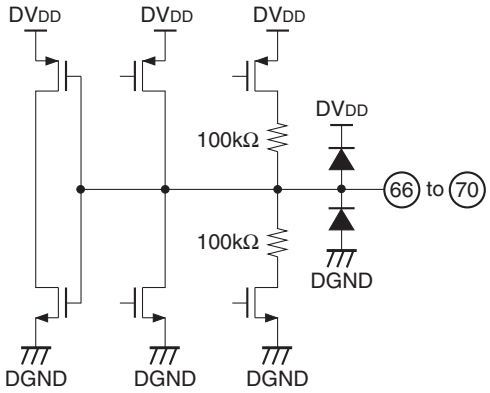
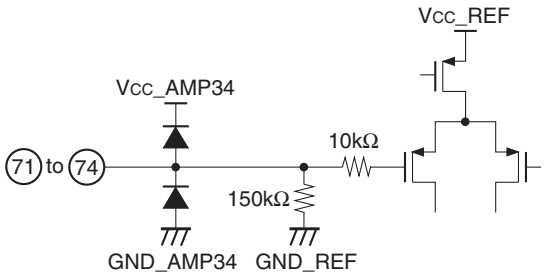
Pin	Symbol	Equivalent circuit
1 2 4 5 7 8 9 10 75 76 77 78 79 80	INL3 INR3 INL4 INR4 INL5 INR5 INL6 INR6 INL0 INR0 INL1 INR1 INL2 INR2	
3	CONTROL0	
6	VFAULT	
11 12 15 16	AMP4OL AMP4OR AMP3OL AMP3OR	

Pin	Symbol	Equivalent circuit
18	REF6	
19 20	CREF6 CREF6H	
22 26	HPOL HPOR	
24	HPBIASOUT	

Pin	Symbol	Equivalent circuit
27 28	HPIR HPIL	
29 30	AMP1IL AMP1IR	
31 32	AMP1OR AMP1OL	
35 36	AMP2OL AMP2OR	

Pin	Symbol	Equivalent circuit
37 38 39 40	SV0OR SV0OL SV1OR SV1OL	
43	CREF165	
44	REF165	
45 46	DA1OL DA1OR	

Pin	Symbol	Equivalent circuit
47	RBGR	
50	REGDA	
51 52 53 54 57 58 59 60 62 63 64 65	DATA0 LRCK0 BCK0 MCK0 DATA1 LRCK1 BCK1 MCK1 X_ALLMUTE X_HDMIMUTE X_RESET TEST	
55	SCK	

Pin	Symbol	Equivalent circuit
56	SDA	
61	X_PROTECT	
66 67 68 69 70	GPIO1 GPIO2 GPIO3 GPIO4 GPIO5	
71 72 73 74	SPLN SPLP SPRN SPRP	

Electrical Characteristics

◆ Absolute Maximum Ratings

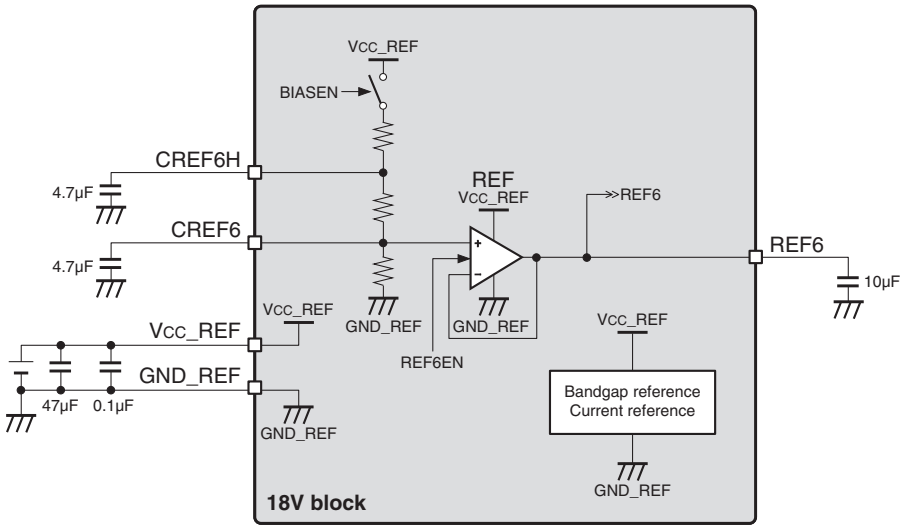
Item	Symbol	Rating	Condition	Unit
Supply voltage	V_{CC}	24.0		V
	AV_{DD}	4.5		V
	DV_{DD}	4.5		V
Operating temperature range	T_A	–25 to +85		℃
Storage temperature range	T_{stg}	–55 to +125		℃
Junction temperature	$T_{J(max)}$	+125		℃
Power dissipation	P_d	$(T_{J(max)} - T_A)/\theta_{JA}$ *1		—
Thermal impedance	θ_{JA_2lay}	64.1	Two-layer board	℃/W
	θ_{JA_4lay}	42.5	Four-layer board	℃/W
	θ_{JC_2lay}	0.4	Two-layer board	℃/W
	θ_{JC_4lay}	0.3	Four-layer board	℃/W

*1 Glass fabric base epoxy two-layer and four-layer board, 76mm × 114mm, t = 1.6mm

◆ Recommended Operating Conditions

Item	Symbol	Min.	Typ.	Max.	Condition	Unit
Supply voltage	V_{CC}	11.0	12.0	14.0	Minimum V_{CC} supply voltage = 8.0V	V
	AV_{DD}	3.0	3.3	3.6		V
	DV_{DD}	3.0	3.3	3.6		V
Operating ambient temperature	T_{opt}	–25	—	+85		℃

Reference Block



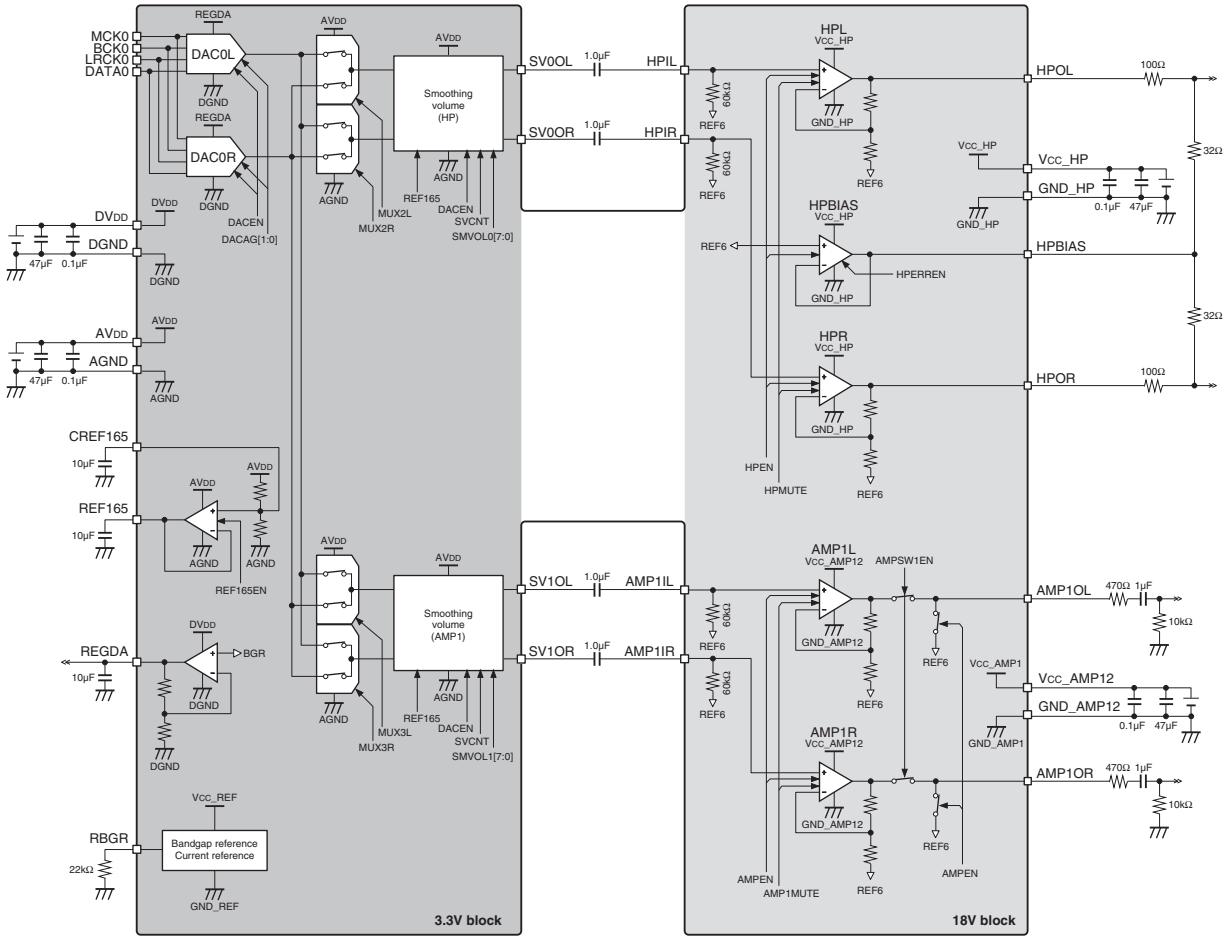
Electrical Characteristics

◆ Electrical Characteristics (Regulator, Reference)

(unless otherwise specified; Ta = 25°C, V_{CC} = 12.0V, AV_{DD} = 3.3V, DV_{DD} = 3.3V, fsignal = 1kHz, Measurement band width = 20 to 20kHz)

Item	Symbol	Min.	Typ.	Max.	Condition	Unit
REGDA output voltage	V_{DA}	2.3	2.5	2.7	For only internal logic core power	V
CREF165 output voltage	$V_{CREF165}$	$(AV_{DD}/2) \times 0.9$	$AV_{DD}/2$	$(AV_{DD}/2) \times 1.1$		V
REF165 output voltage	V_{REF165}	$(AV_{CC}/2) \times 0.9$	$AV_{CC}/2$	$(AV_{CC}/2) \times 1.1$		V
CREF6 output voltage	V_{CREF6}	$(V_{CC}/2) \times 0.9$	$V_{CC}/2$	$(V_{CC}/2) \times 1.1$		V
CREF6H output voltage	V_{CREF6H}	$(3 \times V_{CC}/4) \times 0.9$	$3 \times V_{CC}/4$	$(3 \times V_{CC}/4) \times 1.1$		V
REF6 output voltage	V_{REF6}	$(V_{CC}/2) \times 0.9$	$V_{CC}/2$	$(V_{CC}/2) \times 1.1$		V

DAC0, HP, AMP1 Block



Electrical Characteristics

◆ Electrical Characteristics (DAC0 → SMVOL0 → HP Block)

(unless otherwise specified; Ta = 25℃, V_{CC} = 12.0V, AV_{DD} = 3.3V, DV_{DD} = 3.3V, fsignal = 1kHz, Measurement band width = 20 to 20kHz)

Item	Symbol	Min.	Typ.	Max.	Condition	Unit
HPAMP input impedance	RIN_{HP}	48.0	60.0	72.0		kΩ
Output DC voltage (HPAMP, HPBIAS)	$VOUT_{HP}$	(V_{CC}/2) × 0.9	V_{CC}/2	(V_{CC}/2) × 1.1	AC coupled input	V
HPAMP gain	$GAIN_{HP1}$	8.0	9.0	10.0	fsig = 1kHz	dB
Volume adjustment range	$GAINH_{P2}$	–90.0	—	0.0	fsig = 1kHz	dB
Volume adjustment step	STP_{HP}	0	0.5	1.0		dB
Output level	VOM_{HP}	2.4	2.8	—	SMVOL0 = 0dB, R_L = 100Ω + 32Ω, DAC0 = 0dBFS, V_{CC} = 12.0V	Vrms
	VO_{HP1}	1.78	2.0	2.24	SMVOL0 = 0dB, R_L = 100Ω + 32Ω, DAC0 = –3dBFS, V_{CC} = 12.0V	Vrms
THD+N	THD_{HP1}	—	1.0	10.0	SMVOL0 = 0dB, R_L = 100Ω + 32Ω, DAC0 = 0dBFS, V_{CC} = 12.0V	%
	THD_{HP2}	—	0.10	0.20	SMVOL0 = 0dB, R_L = 100Ω + 32Ω, DAC0 = –3dBFS, V_{CC} = 12.0V	%
Output noise level	VN_{HP1}	—	–90.0	–80.0	SMVOL0 = 0dB, R_L = 100Ω + 32Ω, DAC0 = No signal, Measured at R_L of 32Ω	dBm
	VN_{HP2}	—	—	–90.0	SMVOL0 = –90dB, R_L = 100Ω + 32Ω, DAC0 = No signal, Measured at R_L of 32Ω	dBm
	VN_{HP3}	—	—	–96.0	SMVOL0 = Mute, R_L = 100Ω + 32Ω, DAC0 = No signal, Measured at R_L of 32Ω	dBm
Gain error	GE_{HP}	–0.5	0	0.5	SMVOL0 = 0dB, R_L = 10kΩ, DAC0 = –3dBFS, V_{CC} = 12.0V	dB
Channel separation	CS_{HP}	70.0	80.0	—	DAC0 = 0dBFS/No signal, 1kHz BPF, Rg = 1kΩ	dB

Item	Symbol	Min.	Typ.	Max.	Condition	Unit
Cross talk	CT_{HP}	70.0	80.0	—	DAC0 = No signal, DAC1 = 0dBFS, AMP2, 3, 4 gain = 9dB, INLx/Rx = 1.0Vrms, 1kHz BPF, Rg = 1kΩ	dB
PSRR	$PSRR_{HP}$	30.0	40.0	—	DAC0 = No signal, fsig = 1kHz	dB

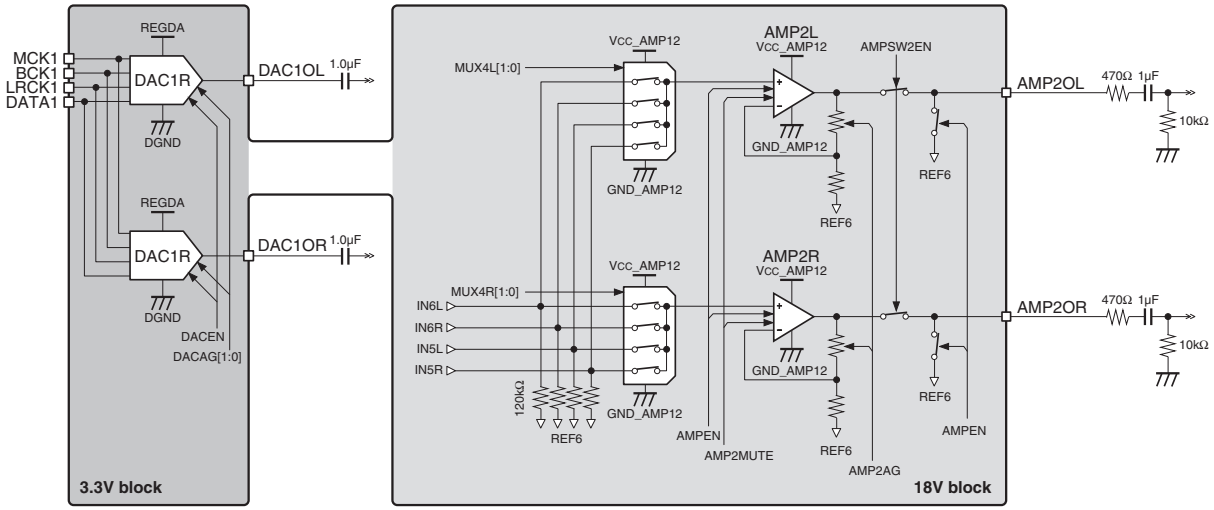
◆ **Electrical Characteristics (DAC0 → SMVOL1 → AMP1 Block)**

(unless otherwise specified; Ta = 25℃, V_{CC} = 12.0V, AV_{DD} = 3.3V, DV_{DD} = 3.3V, fsignal = 1kHz, Measurement band width = 20 to 20kHz)

Item	Symbol	Min.	Typ.	Max.	Condition	Unit
AMP1 input impedance	RIN_{AMP1}	48.0	60.0	72.0		kΩ
Output DC voltage	$VOUT_{AMP1}$	(V_{CC}/2) × 0.9	V_{CC}/2	(V_{CC}/2) × 1.1	AC coupled input	V
AMP1 gain	$GAIN_{AMP1\_1}$	8.0	9.0	10.0	fsig = 1kHz	dB
Volume adjustment range	$GAIN_{AMP1\_2}$	–90.0	—	0.0	fsig = 1kHz	dB
Volume adjustment step	STP_{AMP1}	0	0.5	1.0		dB
Output level	VOM_{AMP1_1}	2.4	2.8	—	SMVOL1 = 0dB, R_L = 10kΩ, DAC0 = 0dBFS, V_{CC} = 12.0V	Vrms
	VO_{AMP1_2}	1.78	2.0	2.24	SMVOL1 = 0dB, R_L = 10kΩ, DAC0 = –3dBFS, V_{CC} = 12.0V	Vrms
THD+N	$THDA_{MP1\_1}$	—	1.0	10.0	SMVOL1 = 0dB, R_L = 10kΩ, DAC0 = 0dBFS, V_{CC} = 12.0V	%
	THD_{AMP1_2}	—	0.02	0.10	SMVOL1 = 0dB, R_L = 10kΩ, DAC0 = –3dBFS, V_{CC} = 12.0V	%
Output noise level	VN_{AMP1_1}	—	–80.0	–74.0	SMVOL1 = 0dB, R_L = 10kΩ, DAC0 = No signal	dBm
	VN_{AMP1_2}	—	—	–84.0	SMVOL1 = –90dB, R_L = 10kΩ, DAC0 = No signal	dBm
	VN_{AMP1_3}	—	—	–88.0	SMVOL1 = Mute, R_L = 10kΩ, DAC0 = No signal	dBm
Gain error	GE_{AMP1}	–0.5	0	0.5	SMVOL0 = 0dB, R_L = 10kΩ, DAC0 = –3dBFS, V_{CC} = 12.0V	dB

Item	Symbol	Min.	Typ.	Max.	Condition	Unit
Channel separation	CS_{AMP1}	70.0	80.0	—	DAC0 = 0dBFS/No signal, 1kHz BPF, Rg = 1kΩ	dB
Cross talk	CT_{AMP1}	70.0	80.0	—	DAC0 = No signal, DAC1 = 0dBFS, AMP2, 3, 4 gain = 9dB, INLx/Rx = 1.0Vrms, 1kHz BPF, Rg = 1kΩ	dB
PSRR	$PSRR_{AMP1}$	30.0	40.0	—	DAC0 = No signal, fsig = 1kHz	dB

DAC1, AMP2 Block



Electrical Characteristics

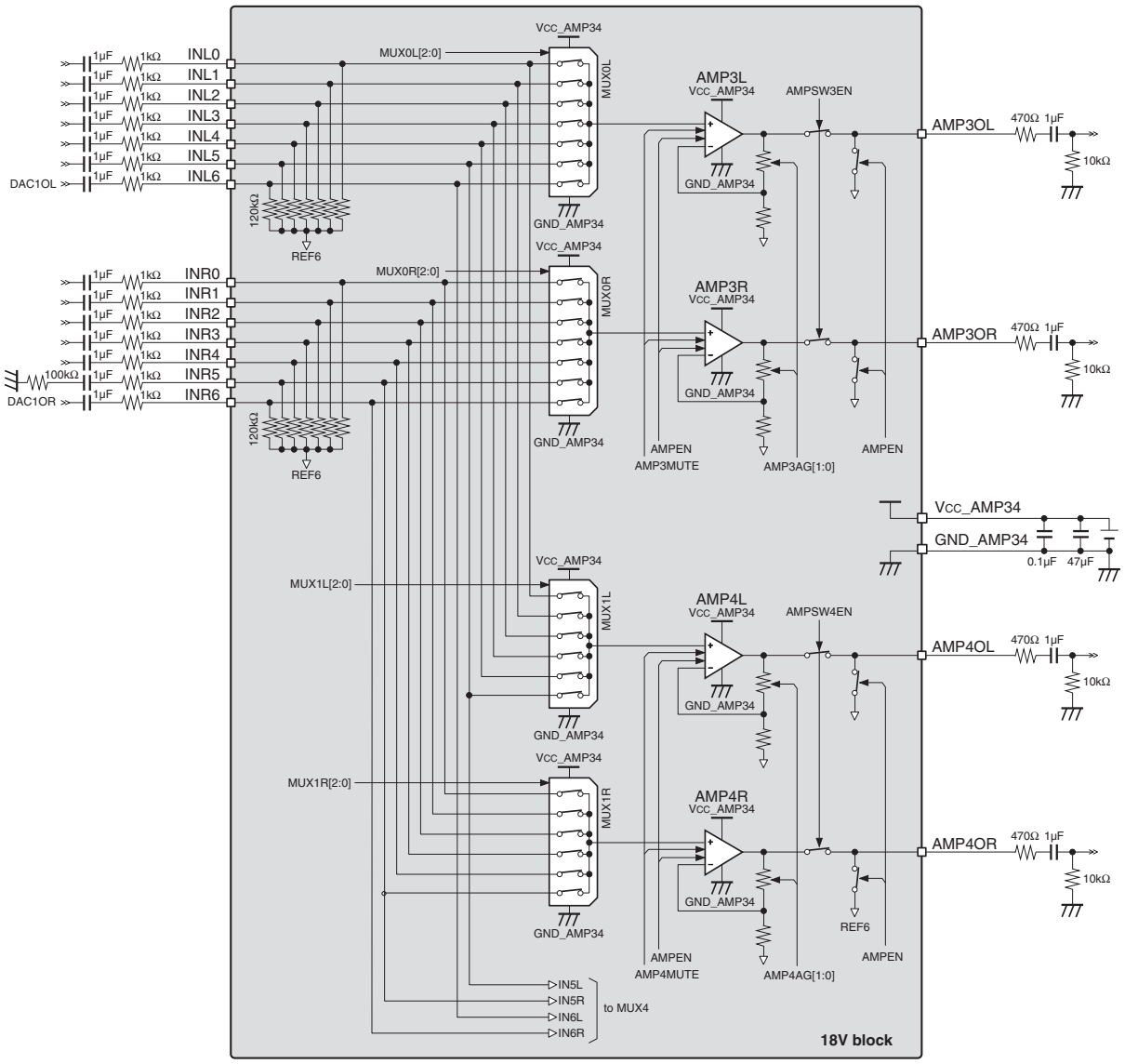
◆ Electrical Characteristics ([1] DAC1 → AMP2 / [2] INL,R5 → AMP2 Block)

(unless otherwise specified; Ta = 25℃, V_{CC} = 12.0V, AV_{DD} = 3.3V, DV_{DD} = 3.3V, fsignal = 1kHz, Measurement band width = 20 to 20kHz)

Item	Symbol	Min.	Typ.	Max.	Condition	Unit
<[1] DAC1 → AMP2>						
AMP2 input impedance	RIN_{AMP2}	96.0	120.0	144.0		kΩ
Output DC voltage	$VOUT_{AMP2}$	(V_{CC}/2) × 0.9	V_{CC}/2	(V_{CC}/2) × 1.1	AC coupled input	V
AMP2 gain	$GAIN_{AMP2\_1}$	–1.0	0.0	1.0	fsig = 1kHz	dB
	$GAIN_{AMP1\_2}$	8.0	9.0	10.0	fsig = 1kHz	dB
Output level	VOM_{AMP2_1}	2.4	2.8	—	R_L = 10kΩ, AMP2 gain = 9dB, DAC1 = 0dBFS, V_{CC} = 12.0V	Vrms
	VO_{AMP2_2}	1.78	2.0	2.24	R_L = 10kΩ, AMP2 gain = 9dB, DAC1 = –3dBFS, V_{CC} = 12.0V	Vrms
THD+N	THD_{AMP2_1}	—	1.0	10.0	R_L = 10kΩ, AMP2 gain = 9dB, DAC1 = 0dBFS, V_{CC} = 12.0V	%
	THD_{AMP2_2}	—	0.02	0.10	R_L = 10kΩ, AMP2 gain = 9dB, DAC1 = –3dBFS, V_{CC} = 12.0V	%
Output noise level	VN_{AMP2_1}	—	–80.0	–74.0	R_L = 10kΩ, AMP2 gain = 9dB, DAC1 = No signal	dBm
Gain error	GE_{AMP2_1}	–0.5	0	0.5	R_L = 10kΩ, AMP2 gain = 9dB, DAC1 = –3dBFS, V_{CC} = 12.0V	dB
Channel separation	CS_{AMP2_1}	70.0	80.0	—	DAC1 = 0dBFS/No signal, AMP2 gain = 9dB, 1kHz BPF, Rg = 1kΩ	dB
Cross talk	CT_{AMP2_1}	70.0	80.0	—	DAC1 = No signal, DAC0 = 0dBFS, AMP2, 3, 4 gain = 9dB, INLx/Rx = 1.0Vrms, 1kHz BPF, Rg = 1kΩ	dB
PSRR	$PSRR_{AMP2\_1}$	30.0	40.0	—	DAC1 = No signal, fsig = 1kHz, AMP2 gain = 9dB	dB

Item	Symbol	Min.	Typ.	Max.	Condition	Unit
<[2] INL,R5 → AMP2>						
Output level	VOM_{AMP2_3}	2.4	2.8	—	R_L = 10kΩ, AMP2 gain = 9dB, INL,R5 = 1.0Vrms, V_{CC} = 12.0V	Vrms
	VO_{AMP2_4}	1.78	2.0	2.24	R_L = 10kΩ, AMP2 gain = 9dB, INL,R5 = 0.7Vrms, V_{CC} = 12.0V	Vrms
THD+N	THD_{AMP2_3}	—	1.0	10.0	R_L = 10kΩ, AMP2 gain = 9dB, INL,R5 = 1.0Vrms, V_{CC} = 12.0V	%
	THD_{AMP2_4}	—	0.01	0.05	R_L = 10kΩ, AMP2 gain = 9dB, INL,R5 = 0.7Vrms, V_{CC} = 12.0V	%
Output noise level	VN_{AMP2_2}	—	–90.0	–84.0	R_L = 10kΩ, AMP2 gain = 9dB, INL,R5 = No signal	dBm
Gain error	GE_{AMP2_2}	–0.5	0	0.5	R_L = 10kΩ, AMP2 gain = 9dB, INL,R5 = 1.0Vrms, V_{CC} = 12.0V	dB
Channel separation	CS_{AMP2_2}	70.0	80.0	—	INL,R5 = 1.0Vrms/No signal, AMP2 gain = 9dB, 1kHz BPF, Rg = 1kΩ	dB
Cross talk	CT_{AMP2_2}	70.0	80.0	—	INL,R5 = No signal, DAC0 = 0dBFS, AMP2, 3, 4 gain = 9dB, INLx/Rx = 1.0Vrms, 1kHz BPF, Rg = 1kΩ	dB
PSRR	$PSRR_{AMP2\_2}$	30.0	40.0	—	INL,R5 = No signal, fsig = 1kHz, AMP2 gain = 9dB	dB

AMP3, 4 Block


INL0
INL1
INL2
INL3
INL4
INL5
INL6
DAC1OL
INR0
INR1
INR2
INR3
INR4
INR5
INR6
DAC1OR
1µF
1kΩ
100kΩ
120kΩ
REF6
MUX0L[2:0]
MUX0R[2:0]
MUX1L[2:0]
MUX1R[2:0]
MUX0L
MUX0R
MUX1L
MUX1R
Vcc_AMP34
GND_AMP34
AMP3L
AMP3R
AMP4L
AMP4R
AMPSW3EN
AMPSW4EN
AMPEN
AMP3MUTE
AMP4MUTE
AMP3AG[1:0]
AMP4AG[1:0]
AMP3OL
AMP3OR
AMP4OL
AMP4OR
470Ω
10kΩ
0.1µF
47µF
IN5L
IN5R
IN6L
IN6R
to MUX4
18V block

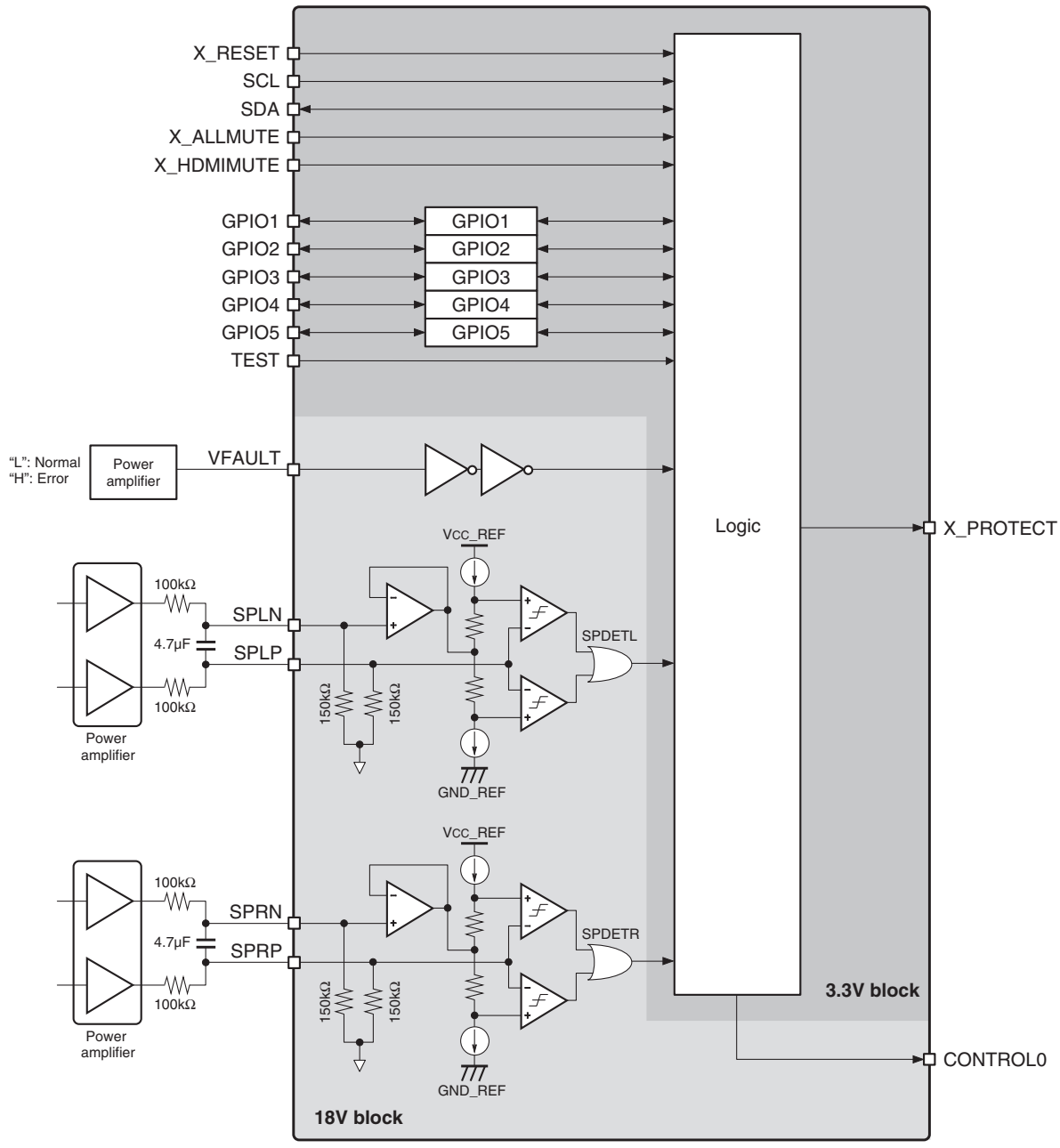
Electrical Characteristics

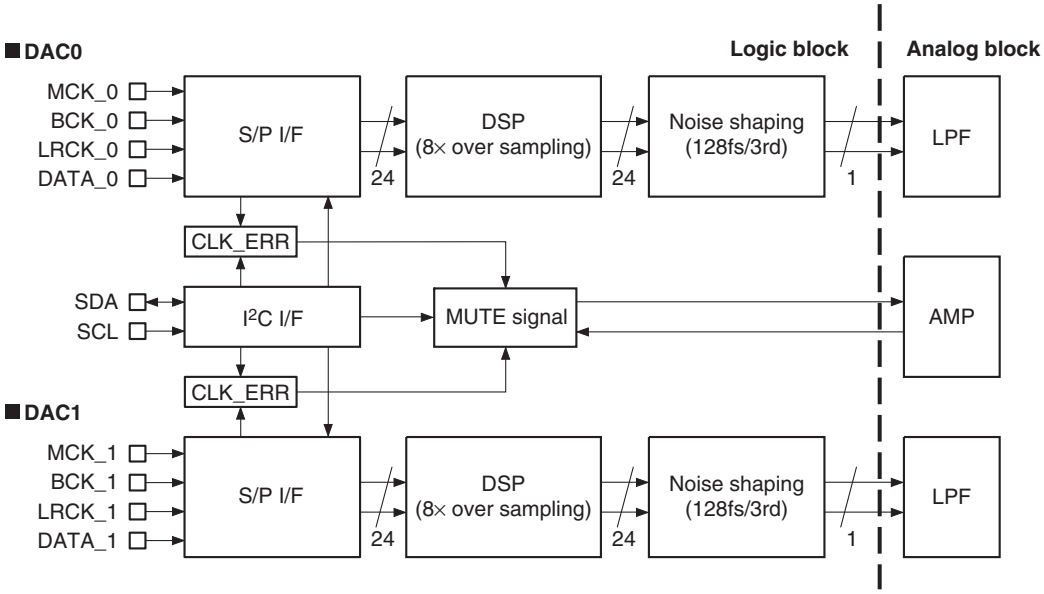
◆ Electrical Characteristics (INL,Rx → AMP3 / INL,Rx → AMP4 Block)

(unless otherwise specified; Ta = 25℃, V_{CC} = 12.0V, AV_{DD} = 3.3V, DV_{DD} = 3.3V, fsignal = 1kHz, Measurement band width = 20 to 20kHz)

Item	Symbol	Min.	Typ.	Max.	Condition	Unit
INL,Rx input impedance	RIN_{INLRx}	96.0	120.0	144.0		kΩ
Output DC voltage	$VOUT_{AMP34}$	(V_{CC}/2) × 0.9	V_{CC}/2	(V_{CC}/2) × 1.1	AC coupled input	V
AMP3, 4 gain	$GAIN_{AMP34\_1}$	–1.0	0.0	1.0	fsig = 1kHz	dB
	$GAIN_{AMP34\_2}$	2.0	3.0	4.0	fsig = 1kHz	dB
	$GAIN_{AMP34\_3}$	8.0	9.0	10.0	fsig = 1kHz	dB
Output level	VOM_{AMP34_1}	2.4	2.8	—	THD = 10.0%, R_L = 10kΩ, AMP3, 4 gain = 9dB, INL,R5 = 1.0Vrms, V_{CC} = 12.0V	Vrms
	VO_{AMP34_2}	1.78	2.0	2.24	R_L = 10kΩ, AMP3, 4 gain = 9dB, INL,R5 = 0.7Vrms, V_{CC} = 12.0V	Vrms
THD+N	THD_{AMP34_1}	—	1.0	10.0	R_L = 10kΩ, AMP3, 4 gain = 9dB, INL,R5 = 1.0Vrms, V_{CC} = 12.0V	%
	THD_{AMP34_2}	—	0.01	0.05	R_L = 10kΩ, AMP3, 4 gain = 9dB, INL,R5 = 0.7Vrms, V_{CC} = 12.0V	%
Output noise level	VN_{AMP34}	—	–90.0	–84.0	R_L = 10kΩ, AMP3, 4 gain = 9dB, INL,R5 = No signal	dBm
Gain error	GE_{AMP34}	–0.5	0	0.5	R_L = 10kΩ, AMP3, 4 gain = 9dB, INL,R5 = 0.7Vrms, V_{CC} = 12.0V	dB
Channel separation	CS_{AMP34}	70.0	80.0	—	INL,Rx = 1.0Vrms/No signal, AMP3, 4 gain = 9dB, 1kHz BPF, Rg = 1kΩ	dB
Cross talk	CT_{AMP34}	70.0	80.0	—	INL,Rx = No signal, DAC0, 1 = 0dBFS, AMP3, 4 gain = 9dB, 1kHz BPF, Rg = 1kΩ	dB
PSRR	$PSRR_{AMP34}$	30.0	40.0	—	INL,Rx = No signal, fsig = 1kHz, AMP3, 4 gain = 9dB	dB

Logic Block


X_RESET
SCL
SDA
X_ALLMUTE
X_HDMIMUTE
GPIO1
GPIO2
GPIO3
GPIO4
GPIO5
TEST
GPIO1
GPIO2
GPIO3
GPIO4
GPIO5
"L": Normal
"H": Error
Power amplifier
VFAULT
Logic
X_PROTECT
VCC_REF
100kΩ
SPLN
4.7μF
SPLP
100kΩ
Power amplifier
150kΩ
150kΩ
SPDETL
GND_REF
VCC_REF
100kΩ
SPRN
4.7μF
SPRP
100kΩ
Power amplifier
150kΩ
150kΩ
SPDETR
GND_REF
3.3V block
CONTROL0
18V block


■DAC0
Logic block
Analog block
MCK_0
BCK_0
LRCK_0
DATA_0
S/P I/F
24
DSP
(8× over sampling)
24
Noise shaping
(128fs/3rd)
1
LPF
CLK_ERR
SDA
SCL
I²C I/F
MUTE signal
AMP
CLK_ERR
■DAC1
MCK_1
BCK_1
LRCK_1
DATA_1
S/P I/F
24
DSP
(8× over sampling)
24
Noise shaping
(128fs/3rd)
1
LPF

Electrical Characteristics

◆ Electrical Characteristics (Filter Block)

(unless otherwise specified; Ta = 25℃, V_{CC} = 12.0V, AV_{DD} = 3.3V, DV_{DD} = 3.3V)

Item	Symbol	Min.	Typ.	Max.	Condition	Unit
DAC Spec.						
Resolution			24			Bits
Audio data interface format			I^2S, left justified MSB first			
Audio data bit length			16 bits, 24 bits, 32 bits selectable			
Audio data format			Binary 2's complement			
Sampling frequency	fs	10		50		kHz
System clock frequency			256, 512fs			
Digital Filter Performance						
Pass band				0.456fs	±0.031dB	
Pass band				0.489fs	–3dB	
Stop band		0.546fs				
Pass-band ripple				±0.031		dB
Stop-band attenuation		–55				dB
Analog Filter Performance						
Frequency response			–0.02		f = 20kHz, fs = 48kHz	dB
			–0.37		f = 48kHz, fs = 48kHz	

◆ Electrical Characteristics (Serial Audio Interface Block; DC)

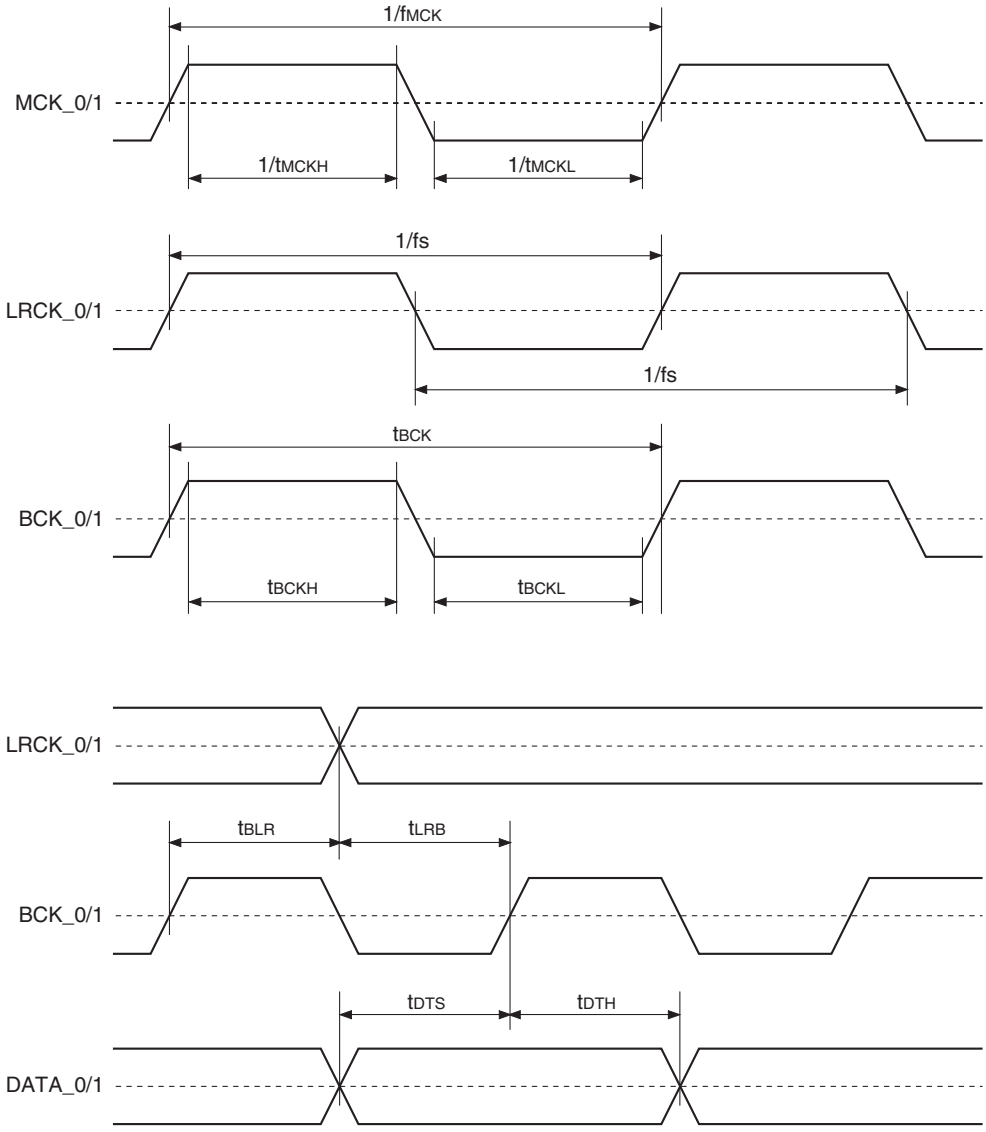
(unless otherwise specified; Ta = 25℃, V_{CC} = 12.0V, AV_{DD} = 3.3V, DV_{DD} = 3.3V)

Item	Symbol	Min.	Typ.	Max.	Condition	Unit
Digital Input						
Logic family			CMOS compatible			
Input Logic Level						
High-level input voltage	V_{IH}	0.7 × DV_{DD}		DV_{DD}		Vdc
Low-level input voltage	V_{IL}	0		0.5		Vdc
Input Logic Current						
Input leakage current			±1			μA

◆ **Electrical Characteristics (Serial Audio Interface Block; AC)**

(unless otherwise specified; Ta = 25℃, V_{CC} = 12.0V, AV_{DD} = 3.3V, DV_{DD} = 3.3V)

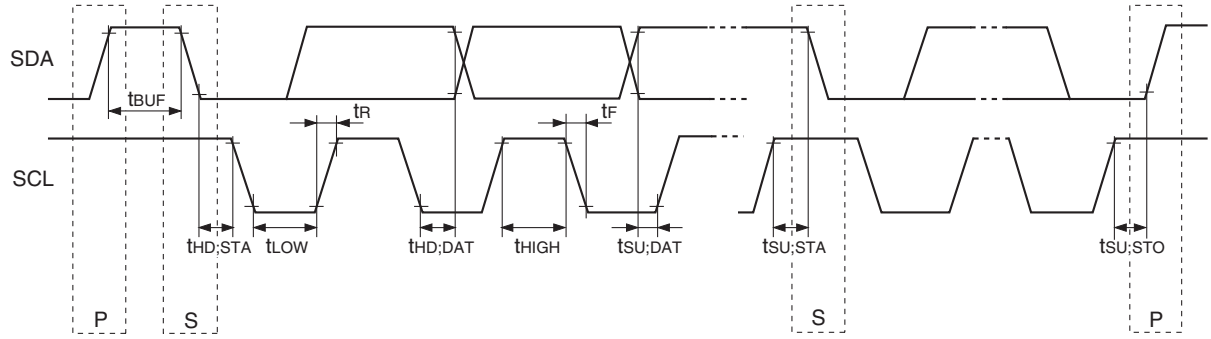
Item	Symbol	Min.	Typ.	Max.	Condition	Unit
Clock Frequency						
MCK frequency	f_{MLK}	5.12		25.6	MCK_SEL = 512Fs	MHz
Duty cycle	d_{MLK}	40		60	$t_{MCKH} \times f_{MCK}$, $t_{MCKL} \times f_{MCK}$	%
LRCK frequency	fs	10		50		kHz
Serial Audio Interface						
BCK cycle time	t_{BCK}	1/32fs, or 1/48fs, or 1/64fs				s
BCK High level time	t_{BCKH}	100				ns
BCK Low level time	t_{BCKL}	100				ns
BCK rising edge to LRCK edge	t_{BLR}	20				ns
LRCK edge to BCK rising edge	t_{LRB}	20				ns
DATA setup time	t_{DTS}	20				ns
DATA hold time	t_{DTH}	20				ns


1/fMCK
MCK_0/1
1/tMCKH
1/tMCKL
1/fs
LRCK_0/1
1/fs
tBCK
BCK_0/1
tBCKH
tBCKL
LRCK_0/1
tBLR
tLRB
BCK_0/1
tDTS
tDTH
DATA_0/1

◆ Electrical Characteristics (I²C BUS Block)

(unless otherwise specified; Ta = 25°C, V_{CC} = 12.0V, AV_{DD} = 3.3V, DV_{DD} = 3.3V, fsignal = 1kHz, Measurement band width = 20 to 20kHz)

Item	Symbol	Min.	Typ.	Max.	Condition	Unit
High level input voltage	V_{IH}	0.7 × DV_{DD}	—	DV_{DD}		V
Low level input voltage	V_{IL}	0	—	0.5		V
High level input current	I_{IH}	—	—	10.0		μA
Low level input current	I_{IL}	—	—	10.0		μA
Low level output voltage	V_{OL}	0	—	0.4	SDA and SCL 3mA current supplied	V
Clock frequency	f_{SCL}	—	—	400		kHz
Data change minimum waiting time	t_{BUF}	1.3	—	—		μs
Data transfer start waiting time	$t_{HD;STA}$	0.6	—	—		μs
Low level clock pulse width	t_{LOW}	1.3	—	—		μs
High level clock pulse width	t_{HIGH}	0.6	—	—		μs
Start setup waiting time	$t_{SU;STA}$	0.6	—	—		μs
Data hold time	$t_{HD;DAT}$	0	—	—		μs
Data setup time	$t_{SU;DAT}$	100	—	—		ns
Rise time	t_R	—	—	300		ns
Fall time	t_F	—	—	300		ns
Stop setup waiting time	$t_{SU;STO}$	0.6	—	—		μs



◆ Electrical Characteristics (GPIO Block)

(unless otherwise specified; Ta = 25°C, V_{CC} = 12.0V, AV_{DD} = 3.3V, DV_{DD} = 3.3V, fsignal = 1kHz, Measurement band width = 20 to 20kHz)

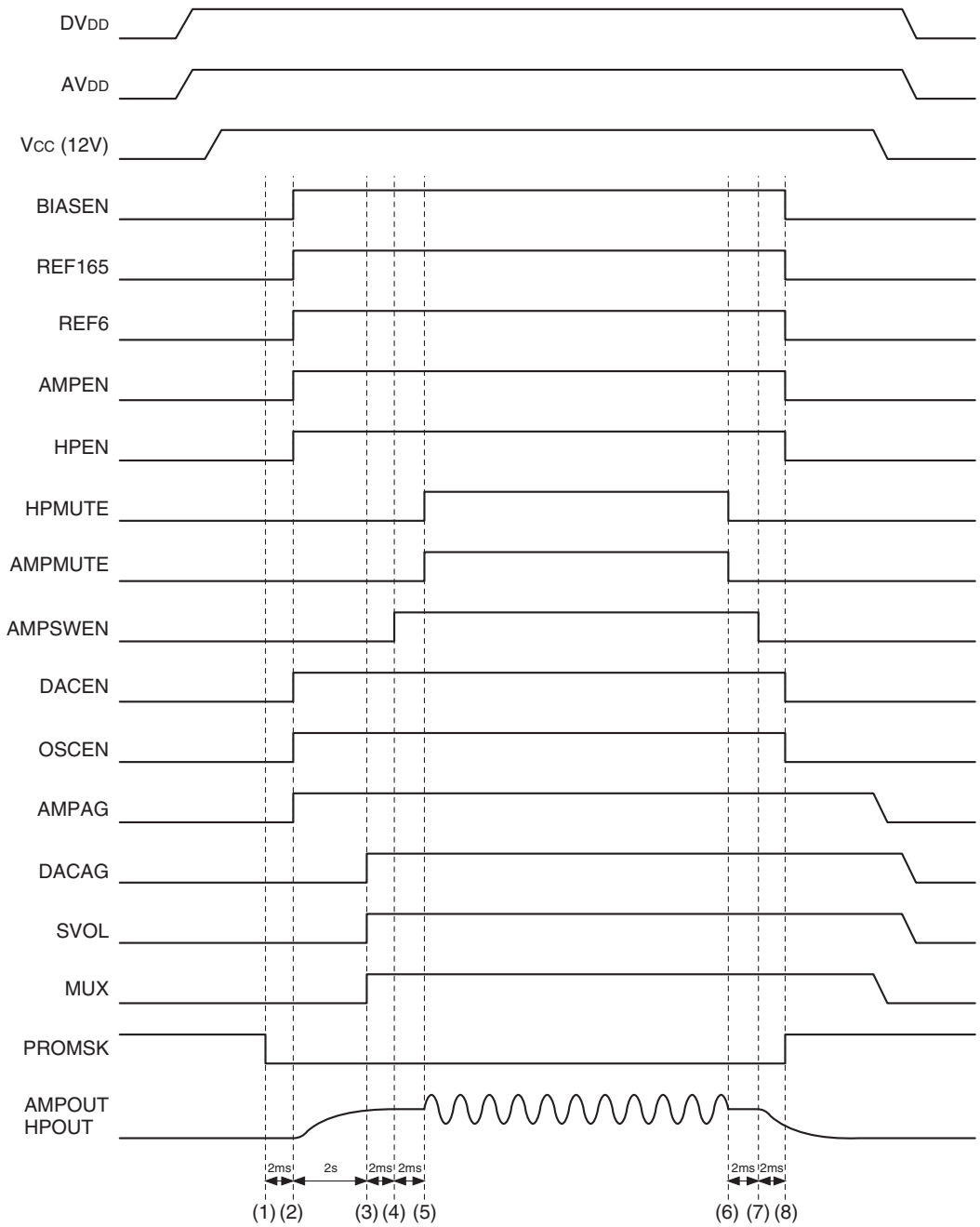
Item	Symbol	Min.	Typ.	Max.	Condition	Unit
Input Low voltage	V_{IL}	0	—	0.5		V
Input High voltage	V_{IH}	0.7 × DV_{DD}	—	DV_{DD}		V
Output Low voltage	V_{OL}	0	—	0.5	I_{SINK} = 1mA	V
Output High voltage	V_{OH}	2.5	—	DV_{DD}	I_{SOURCE} = 1mA	V
Pull-up resistor	R_{PU}	50	100	200		kΩ
Pull-down resistor	R_{PD}	50	100	200		kΩ

◆ Electrical Characteristics (Detector Block)

(unless otherwise specified; Ta = 25℃, V_{CC} = 12.0V, AV_{DD} = 3.3V, DV_{DD} = 3.3V, fsignal = 1kHz, Measurement band width = 20 to 20kHz)

Item	Symbol	Min.	Typ.	Max.	Condition	Unit
VFAULT High level input voltage	V_{FAULTH}	2.0	—	12.0	Input: High level, V_{CC} = 12V	V
VFAULT Low level input voltage	V_{FAULTL}	0	—	0.5	Input: Low level	V
X_PROTECTOUT High level output voltage	VO_{PROH}	2.7	—	DV_{DD}	Output: High level, R_L = 1MΩ	V
X_PROTECTOUT Low level output voltage	VO_{PROL}	0	—	0.5	Output: Low level, R_L = 1MΩ	V
X_ALLMUTE, X_HDMIMUTE High level input voltage	VI_{MT_CNT}	0.7 × DV_{DD}	—	DV_{DD}	Input: High level	V
X_ALLMUTE, X_HDMIMUTE Low level input voltage	VI_{MT_CNT}	0	—	0.5	Input: Low level	V
Minimum input voltage (SPK_SPxP/N)	$V_{IN\_SPK\_SPP/N}$	0	—	—	Speaker output minimum input voltage, Rin = 100kΩ + 150kΩ	V
Detection voltage 1	V_{DET1}	1.10	1.45	1.80	Speaker out (|SPK_SPxP – SPK_SPxN|) voltage detection, Rin = 100kΩ + 150kΩ	V
SPDET hysteresis	V_{HYS1}	0.04	0.10	0.15		V
Detection voltage 2	V_{DET2}	1.0	1.8	3.5	HPBIAS voltage detection, HPERREN = “1”	V

Power-On/Off Sequence



Power-On Sequence

(1) PROMSK register should be set to "L" after the power is supplied.

(2) Amplifier and BIAS enable registers (BIASEN, REF165, REF6, AMPEN, HPEN, DACEN, OSCEN and AMPAG) should be set to "H" at least 2ms after (2).

(3) DAC Gain, Smoothing Volume and Multiplex select registers be set.

(4) Amplifier output switch register (AMPSWEN) should be set to "H" at least 2s after (3).

(5) Amplifier mute registers (HPMUTE and AMPMUTE) should be set to "H" at least 2ms after (4).

Power-Off Sequence

(6) Amplifier mute registers (HPMUTE and AMPMUTE) should be set to "L".

(7) Amplifier output switch register (AMPSWEN) should be set to "L" at least 2s after (6).

(8) Amplifier and BIAS enable registers (BIASEN, REF165, REF6, AMPEN, HPEN, DACEN and OSCEN) should be set to "L" and PROMSK register should be set to "H" at least 2ms after (7).

Register 1 (Analog Block)

Address	Register name	D7	D6	D5	D4	D3	D2	D1	D0
00	AMP ENABLE REF ENABLE		HPERREN	HPMUTE	HPEN	AMPEN	REF6EN	REF165EN	BIASEN
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	1	0	1	1	1	1	1

Address	Register name	D7	D6	D5	D4	D3	D2	D1	D0
01	AMP SW ENABLE AMP MUTE ENABLE	AMPSW1EN	AMPSW2EN	AMPSW3EN	AMPSW4EN	AMP1MUTE	AMP2MUTE	AMP3MUTE	AMP4MUTE
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

Address	Register name	D7	D6	D5	D4	D3	D2	D1	D0
02	OSC ENABLE DAC ENABLE AMP GAIN CONTROL	OSCEN	DACEN		AMP2AG	AMP3AG[1:0]		AMP4AG[1:0]	
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		1	1	0	0	0	0	0	0

Address	Register name	D7	D6	D5	D4	D3	D2	D1	D0
03	MUTE TIME CONTROL DAC GAIN CONTROL	SMVOL_FREQ[1:0]					SVCNT	DACAG[1:0]	
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		1	0	0	0	0	0	0	1

Address	Register name	D7	D6	D5	D4	D3	D2	D1	D0
04	SMOOTHING VOLUME0	SMVOL0[7:0]							
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		1	1	1	1	1	1	1	1

Address	Register name	D7	D6	D5	D4	D3	D2	D1	D0
05	SMOOTHING VOLUME1	SMVOL1[7:0]							
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		1	1	1	1	1	1	1	1

Address	Register name	D7	D6	D5	D4	D3	D2	D1	D0
06	MUX0			MUX0L[2:0]			MUX0R[2:0]		
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

Address	Register name	D7	D6	D5	D4	D3	D2	D1	D0
07	MUX1			MUX1L[2:0]			MUX1R[2:0]		
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

Address	Register name	D7	D6	D5	D4	D3	D2	D1	D0
08	MUX2, MUX3, MUX4	MUX2L	MUX2R	MUX3L	MUX3R	MUX4L[1:0]		MUX4R[1:0]	
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	1	0	1	0	0	1	0

Address	Register name	D7	D6	D5	D4	D3	D2	D1	D0
09		GP1PD	GP1PU	GP1DATA	GP1EN	GP2PD	GP2PU	GP2DATA	GP2EN
R/W	GPIO1, 2	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		1	0	0	0	1	0	0	0

Address	Register name	D7	D6	D5	D4	D3	D2	D1	D0
0A		GP3PD	GP3PU	GP3DATA	GP3EN	GP4PD	GP4PU	GP4DATA	GP4EN
R/W	GPIO3, 4	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		1	0	0	0	1	0	0	0

Address	Register name	D7	D6	D5	D4	D3	D2	D1	D0
0B	GPIO5	TEST1	TEST2	PROMSK	CNTR0	GP5PD	GP5PU	GP5DATA	GP5EN
R/W	CONTROL0	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	PROTECT MASK	0	0	1	1	1	0	0	0

Address	Register name	D7	D6	D5	D4	D3	D2	D1	D0
0C		TEST3	TEST4	TEST5	GPIO1	GPIO2	GPIO3	GPIO4	GPIO5
R/W	GPIO READ DATA	R/W	R/W	R/W	R	R	R	R	R
Default		0	0	0	0	0	0	0	0

Address	Register name	D7	D6	D5	D4	D3	D2	D1	D0
0D		P_HDMM	X_MCE	P_FAULT	M_CNRL0	X_MAL	X_MHD	M_GP4	M_GP5
R/W	GPIO MODE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

Register (ADD: 00)

Address	Register name	D7	D6	D5	D4	D3	D2	D1	D0
00	AMP ENABLE REF ENABLE		HPERREN	HPMUTE	HPEN	AMPEN	REF6EN	REF165EN	BIASEN
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	1	0	1	1	1	1	1

D6: HPERREN

HP bias short error to VFAULT enable

"0" OFF
"1" ON (default)

D5: HPMUTE

HPAMP mute control

"0" Mute (default)
"1" Un-Mute

D4: HPEN

HPAMP enable

"0" OFF
"1" ON (default)

D3: AMPEN

AMP1 to AMP4 enable

"0" OFF
"1" ON (default)

D2: REF6EN

REF6 amp enable

"0" OFF
"1" ON (default)

D1: REF165EN

REF165 amp enable

"0" OFF
"1" ON (default)

D0: BIASEN

Amp bias enable

"0" OFF
"1" ON (default)

Register (ADD: 01)

Address	Register name	D7	D6	D5	D4	D3	D2	D1	D0
01	AMP SW ENABLE AMP MUTE ENABLE	AMPSW1EN	AMPSW2EN	AMPSW3EN	AMPSW4EN	AMP1MUTE	AMP2MUTE	AMP3MUTE	AMP4MUTE
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

D7: AMPSW1EN

AMP1 output switch enable

"0" OFF (default)
"1" ON

D6: AMPSW2EN

AMP2 output switch enable

"0" OFF (default)
"1" ON

D5: AMPSW3EN

AMP3 output switch enable

"0" OFF (default)
"1" ON

D4: AMPSW4EN

AMP4 output switch enable

"0" OFF (default)
"1" ON

D3: AMP1MUTE

AMP1 mute control

"0" Mute (default)
"1" Un-mute

D2: AMP2MUTE

AMP2 mute control

"0" Mute (default)
"1" Un-mute

D1: AMP3MUTE

AMP3 mute control

"0" Mute (default)
"1" Un-mute

D0: AMP4MUTE

AMP4 mute control

"0" Mute (default)
"1" Un-mute

Register (ADD: 02)

Address	Register name	D7	D6	D5	D4	D3	D2	D1	D0
02	OSC ENABLE DAC ENABLE AMP GAIN CONTROL	OSCEN	DACEN		AMP2AG	AMP3AG[1:0]		AMP4AG[1:0]	
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		1	1	0	0	0	0	0	0

D7: OSCEN

Oscillator for smoothing volume enable

"0" OFF
"1" ON (default)

D6: DACEN

DAC analog and smoothing volume enable

"0" OFF
"1" ON (default)

D4: AMP2AG

AMP2 gain control

"0" 0dB (default)
"1" 9dB

D3-2: AMP3AG[1:0]

AMP3 mute control

"00" 0dB (default)
"01" 3dB
"10" 9dB

D1-0: AMP4AG[1:0]

AMP4 mute control

"00" 0dB (default)
"01" 3dB
"10" 9dB

Register (ADD: 03)

Address	Register name	D7	D6	D5	D4	D3	D2	D1	D0
03	MUTE TIME CONTROL DAC GAIN CONTROL	SMVOL_FREQ[1:0]					SVCNT	DACAG[1:0]	
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		1	0	0	0	0	0	0	1

D7-6: SMVOL_FREQ[1:0]

Smoothing volume transition time control

"00" 7.2ms
"01" 14.4ms
"10" 28.8ms (default)
"11" 57.6ms

D2: SVCNT

Smoothing volume register inverted

"0" Not Inverted (default)
"1" Inverted

D1-0: DACAG[1:0]

DAC LPF gain control

"00" 0.90 times
"01" 0.85 times (default)
"10" 0.80 times
"11" 0.75 times

Register (ADD: 04)

Address	Register name	D7	D6	D5	D4	D3	D2	D1	D0
04	SMOOTHING VOLUME0	SMVOL0[7:0]							
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		1	1	1	1	1	1	1	1

D7-0: SMVOL0[7:0]

Smoothing Volume0 gain control

<Case: SVCNT = "0">

"11111111" 0dB (default)
"11111110" –0.5dB
"11111101" –1.0dB
"11111100" –1.5dB
"11111011" –2.0dB
:
"10100111" –44.0dB
"10100110" –44.5dB
"10100101" –45.0dB
"10100100" –45.5dB
"10100011" –46.0dB
:
"01001110" –88.5dB
"01001101" –89.0dB
"01001100" –89.5dB
"01001011" –90.0dB
"01001010" Mute

<Case: SVCNT = "1">

"00000000" 0dB (default)
"00000001" –0.5dB
"00000010" –1.0dB
"00000011" –1.5dB
"00000100" –2.0dB
:
"01011000" –44.0dB
"01011001" –44.5dB
"01011010" –45.0dB
"01011011" –45.5dB
"01011100" –46.0dB
:
"10110001" –88.5dB
"10110010" –89.0dB
"10110011" –89.5dB
"10110100" –90.0dB
"10110101" Mute

Register (ADD: 05)

Address	Register name	D7	D6	D5	D4	D3	D2	D1	D0
05	SMOOTHING VOLUME1	SMVOL1[7:0]							
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		1	1	1	1	1	1	1	1

D7-0: SMVOL1[7:0]

Smoothing Volume1 gain control

<Case: SVCNT = "0">

"11111111" 0dB (default)
"11111110" –0.5dB
"11111101" –1.0dB
"11111100" –1.5dB
"11111011" –2.0dB
:
"10100111" –44.0dB
"10100110" –44.5dB
"10100101" –45.0dB
"10100100" –45.5dB
"10100011" –46.0dB
:
"01001110" –88.5dB
"01001101" –89.0dB
"01001100" –89.5dB
"01001011" –90.0dB
"01001010" Mute

<Case: SVCNT = "1">

"00000000" 0dB (default)
"00000001" –0.5dB
"00000010" –1.0dB
"00000011" –1.5dB
"00000100" –2.0dB
:
"01011000" –44.0dB
"01011001" –44.5dB
"01011010" –45.0dB
"01011011" –45.5dB
"01011100" –46.0dB
:
"10110001" –88.5dB
"10110010" –89.0dB
"10110011" –89.5dB
"10110100" –90.0dB
"10110101" Mute

Register (ADD: 06)

Address	Register name	D7	D6	D5	D4	D3	D2	D1	D0
06	MUX0			MUX0L[2:0]			MUX0R[2:0]		
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

D5-3: MUX0L[2:0]

MUX0L selector control

"000" INL0 (default)
"001" INL1
"010" INL2
"011" INL3
"100" INL4
"101" INL5
"110" INL6

D2-0: MUX0R[2:0]

MUX0R selector control

"000" INR0 (default)
"001" INR1
"010" INR2
"011" INR3
"100" INR4
"101" INR5
"110" INR6

Register (ADD: 07)

Address	Register name	D7	D6	D5	D4	D3	D2	D1	D0
07	MUX1			MUX1L[2:0]			MUX1R[2:0]		
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

D5-3: MUX1L[2:0]

MUX1L selector control

"000" INL0 (default)
"001" INL1
"010" INL2
"011" INL3
"100" INL4
"101" INL5

D2-0: MUX1R[2:0]

MUX1R selector control

"000" INR0 (default)
"001" INR1
"010" INR2
"011" INR3
"100" INR4
"101" INR5

Register (ADD: 08)

Address	Register name	D7	D6	D5	D4	D3	D2	D1	D0
08	MUX2, MUX3, MUX4	MUX2L	MUX2R	MUX3L	MUX3R	MUX4L[1:0]		MUX4R[1:0]	
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	1	0	1	0	0	1	0

D7: MUX2L

MUX2L selector control

"0" DACL0 (default)
"1" DACR0

D6: MUX2R

MUX2R selector control

"0" DACL0
"1" DACR0 (default)

D5: MUX3L

MUX3L selector control

"0" DACL0 (default)
"1" DACR0

D4: MUX3R

MUX3R selector control

"0" DACL0 (default)
"1" DACR0

D3-2: MUX4L[1:0]

MUX4L selector control

"00" INL5 (default)
"01" INL6
"10" INR5
"11" INR6

D1-0: MUX4R[1:0]

MUX4R selector control

"00" INL5
"01" INL6
"10" INR5 (default)
"11" INR6

Register (ADD: 09)

Address	Register name	D7	D6	D5	D4	D3	D2	D1	D0
09	GPIO1, 2	GP1PD	GP1PU	GP1DATA	GP1EN	GP2PD	GP2PU	GP2DATA	GP2EN
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		1	0	0	0	1	0	0	0

D7: GP1PD

GPIO1 input pull-down resister enable

"0" Pull-down disable
"1" Pull-down enable (default)

D6: GP1PU

GPIO1 input pull-up resister enable

"0" Pull-up disable (default)
"1" Pull-up enable

D5: GP1DATA

GPIO1 output data control

"0" Output is "L" (default)
"1" Output is "H"

D4: GP1EN

GPIO1 input-output enable

"0" Input mode (default)
"1" Output mode

D3: GP2PD

GPIO2 input pull-down resister enable

"0" Pull-down disable
"1" Pull-down enable (default)

D2: GP2PU

GPIO2 input pull-up resister enable

"0" Pull-up disable (default)
"1" Pull-up enable

D1: GP2DATA

GPIO2 output data control

"0" Output is "L" (default)
"1" Output is "H"

D0: GP2EN

GPIO2 input-output enable

"0" Input mode (default)
"1" Output mode

Register (ADD: 0A)

Address	Register name	D7	D6	D5	D4	D3	D2	D1	D0
0A	GPIO3, 4	GP3PD	GP3PU	GP3DATA	GP3EN	GP4PD	GP4PU	GP4DATA	GP4EN
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		1	0	0	0	1	0	0	0

D7: GP3PD

GPIO3 input pull-down resister enable

"0" Pull-down disable
"1" Pull-down enable (default)

D6: GP3PU

GPIO3 input pull-up resister enable

"0" Pull-up disable (default)
"1" Pull-up enable

D5: GP3DATA

GPIO3 output data control

"0" Output is "L" (default)
"1" Output is "H"

D4: GP3EN

GPIO3 input-output enable

"0" Input mode (default)
"1" Output mode

D3: GP4PD

GPIO4 input pull-down resister enable

"0" Pull-down disable
"1" Pull-down enable (default)

D2: GP4PU

GPIO4 input pull-up resister enable

"0" Pull-up disable (default)
"1" Pull-up enable

D1: GP4DATA

GPIO4 output data control

"0" Output is "L" (default)
"1" Output is "H"

D0: GP4EN

GPIO4 input-output enable

"0" Input mode (default)
"1" Output mode

Register (ADD: 0B)

Address	Register name	D7	D6	D5	D4	D3	D2	D1	D0
0B	GPIO5 CONTROL0 PROTECT MASK	TEST1	TEST2	PROMSK	CNTR0	GP5PD	GP5PU	GP5DATA	GP5EN
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	1	1	1	0	0	0

D5: PROMSK

X_PROTECTOUT mask control

"0" Mask OFF
"1" Mask ON (default)
(X_PROTECTOUT function OFF)

D4: CNTR0

CONTROL0 output control

"0" Output is Hi-Z
"1" Output is "L" (default)

D3: GP5PD

GPIO5 input pull-down resister enable

"0" Pull-down disable
"1" Pull-down enable (default)

D2: GP5PU

GPIO5 input pull-up resister enable

"0" Pull-up disable (default)
"1" Pull-up enable

D1: GP5DATA

GPIO5 output data control

"0" Output is "L" (default)
"1" Output is "H"

D0: GP5EN

GPIO5 input-output enable

"0" Input mode (default)
"1" Output mode

Register (ADD: 0C)

Address	Register name	D7	D6	D5	D4	D3	D2	D1	D0
0C	GPIO READ DATA	TEST3	TEST4	TEST5	GPIO1	GPIO2	GPIO3	GPIO4	GPIO5
R/W		R/W	R/W	R/W	R	R	R	R	R
Default		0	0	0	—	—	—	—	—

D4: GPIO1

GPIO1 input data

D3: GPIO2

GPIO2 input data

D2: GPIO3

GPIO3 input data

D1: GPIO4

GPIO4 input data

D0: GPIO5

GPIO5 input data

Register (ADD: 0D)

Address	Register name	D7	D6	D5	D4	D3	D2	D1	D0
0D	GPIO MODE	P_HDMM	X_MCE	P_FAULT	M_CNRL0	X_MAL	X_MHD	M_GP4	M_GP5
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

D7: P_HDMM

X_HDMIMUTE polarity

"0" Low active (default)
"1" High active

D6: X_MCE

Clock error mask

"0" Mask (default)
"1" Don't mask

D5: P_FAULT

VFAULT polarity

"0" High active (default)
"1" Low active

D4: M_CNTR0

X_CONTROL0 mask

"0" CONTROL0 mode (default)
"1" MUTE mode

D3: X_MAL

X_ALLMUTE mask

"0" Mask (default)
"1" Don't mask

D2: X_MHD

X_HDMIMUTE mask

"0" Mask (default)
"1" Don't mask

D1: M_GP4

GPIO4 usage mode

"0" GPIO mode (default)
"1" MUTE mode

D0: M_GP5

GPIO5 usage mode

"0" GPIO mode (default)
"1" CLOCK ERROR mode

Register 2 (Digital Block)

◆ DAC_0 Register

Address	Register name	D7	D6	D5	D4	D3	D2	D1	D0
10	DAC Format CONTROL_0	LENGTH_SEL_0[1:0]		BCK_SEL_0[1:0]		D_FORMAT _SEL_0	TEST		MCK_SEL_0
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	1	0	0	1

Address	Register name	D7	D6	D5	D4	D3	D2	D1	D0
11	DAB CONTROL_0	TEST		DABON_0	FORCE_ MASK_0	SYNC_0	TEST		S_RESET_0
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	W
Default		0	0	0	0	0	0	0	0

Address	Register name	D7	D6	D5	D4	D3	D2	D1	D0
12	TEST_00	TEST							
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

Address	Register name	D7	D6	D5	D4	D3	D2	D1	D0
13	TEST_01	TEST							
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	1	0

Address	Register name	D7	D6	D5	D4	D3	D2	D1	D0
14	TEST_02	TEST							
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		1	0	1	1	0	0	0	0

Address	Register name	D7	D6	D5	D4	D3	D2	D1	D0
15	TEST_03	TEST							
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

Address	Register name	D7	D6	D5	D4	D3	D2	D1	D0
16	CLOCK_ERROR_0	MCK_ERR _MSK_0	TEST	BCK_ERR _MSK_0	TEST			LRCK_ERR _MSK_0	TEST
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		1	0	1	1	0	0	1	0

Address	Register name	D7	D6	D5	D4	D3	D2	D1	D0
17	TEST_05	TEST							
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

◆ DAC_1 Register

Address	Register name	D7	D6	D5	D4	D3	D2	D1	D0
18	DAC Format CONTROL_1	LENGTH_SEL_1[1:0]		BCK_SEL_1[1:0]		D_FORMAT _SEL_1	TEST		MCK_SEL_1
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	1	0	0	1

Address	Register name	D7	D6	D5	D4	D3	D2	D1	D0
19	DAB CONTROL_1	TEST		DABON_1	FORCE_ MASK_1	SYNC_1	TEST		S_RESET_1
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	W
Default		0	0	0	0	0	0	0	0

Address	Register name	D7	D6	D5	D4	D3	D2	D1	D0
1A	TEST_10	TEST							
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

Address	Register name	D7	D6	D5	D4	D3	D2	D1	D0
1B	TEST_11	TEST							
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	1	0

Address	Register name	D7	D6	D5	D4	D3	D2	D1	D0
1C	TEST_12	TEST							
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		1	0	1	1	0	0	0	0

Address	Register name	D7	D6	D5	D4	D3	D2	D1	D0
1D	TEST_13	TEST							
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

Address	Register name	D7	D6	D5	D4	D3	D2	D1	D0
1E	CLOCK_ERROR_1	MCK_ERR _MSK_1	TEST	BCK_ERR _MSK_1	TEST			LRCK_ERR _MSK_1	TEST
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		1	0	1	1	0	0	1	0

Register (ADD: 10)

Address	Register name	D7	D6	D5	D4	D3	D2	D1	D0
10	DAC Format CONTROL_0	LENGTH_SEL_0[1:0]		BCK_SEL_0[1:0]		D_FORMAT _SEL_0	TEST		MCK_SEL_0
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	1	0	0	1

D7-6: LENGTH_SEL_0[1:0]

Word bit length

"00" 32 bits (default)
"01" 24 bits
"10" 16 bits
"11" —

D5-4: BCK_SEL_0[1:0]

BCK frequency

"00" 64Fs (default)
"01" 48Fs
"10" 32Fs
"11" —

D3: D_FORMAT_SEL_0

Data format

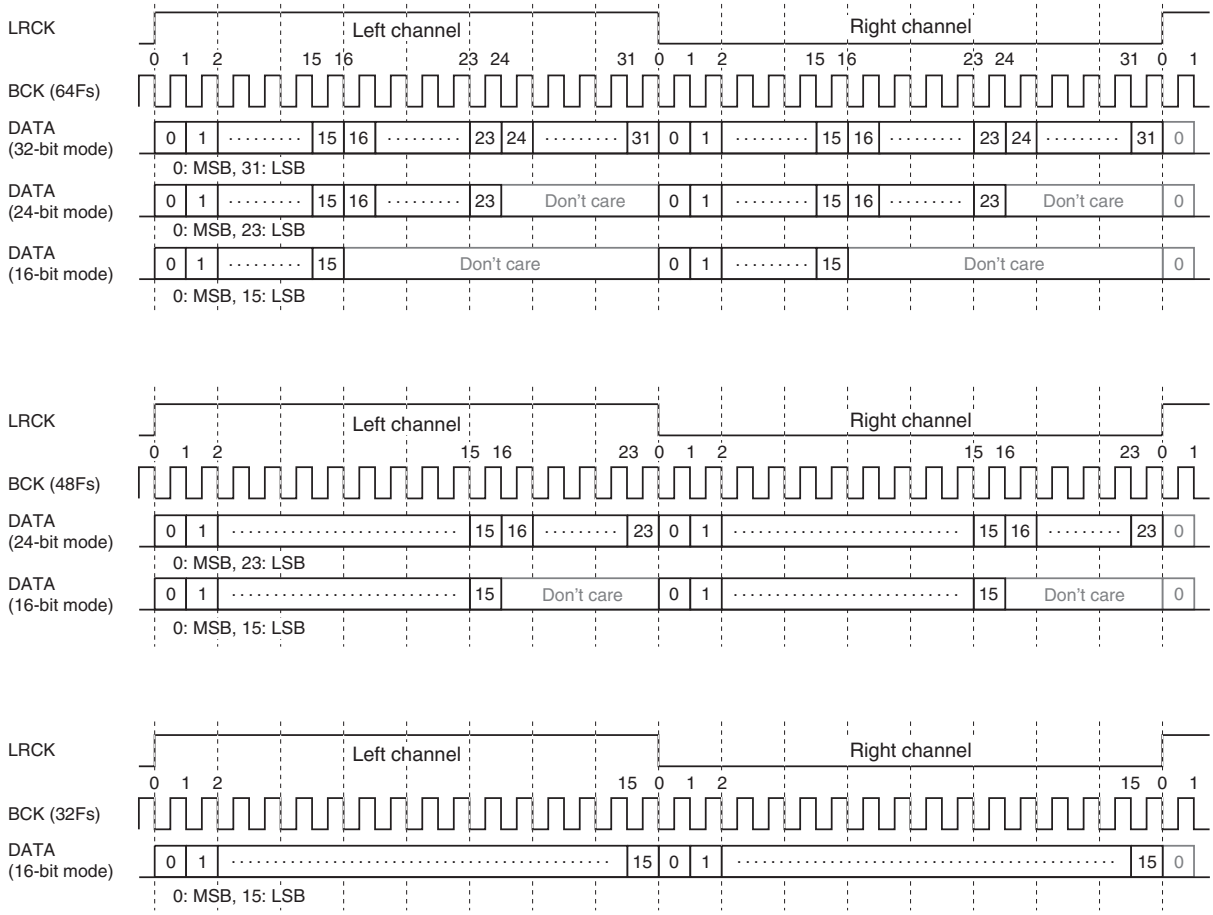
"0" Left justified, MSB first
"1" I^2S compatible (default)

D0: MCK_SEL_0

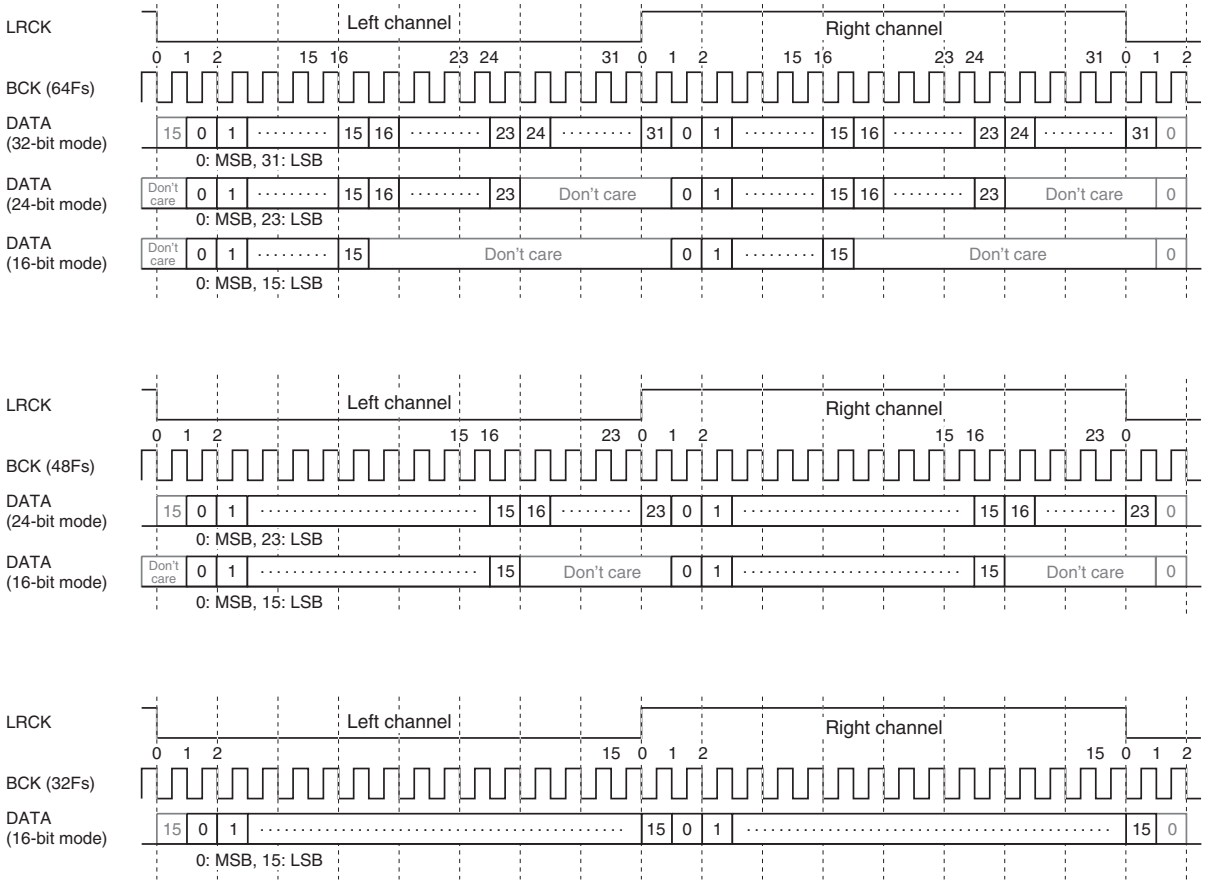
MCK frequency

"0" 512Fs
"1" 256Fs (default)

Left Justified MSB First Mode



I²S Compatible Mode



Register (ADD: 11)

Address	Register name	D7	D6	D5	D4	D3	D2	D1	D0
11	DAB CONTROL_0	TEST		DABON_0	FORCE_ MASK_0	SYNC_0	TEST		S_RESET_0
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	W
Default		0	0	0	0	0	0	0	0

D5: DABON_0

DSP operation

"0" Stop (default)
"1" Start

D4: FORCE_MASK_0

Valid if SYNC_0 = 0

"0" Resynchronization will be made if LRCK edge does not come with the internal window. (default)
"1" Resynchronization will not be made if LRCK edge does not come with the internal window.

D3: SYNC_0

Synchronization mode

"0" Automatic (default)
First LRCK after reset will be used to make synchronization.
Resynchronization will be made when LRCK edge does not come with the internal window.
(±4 MCK)

"1" Forced to the edge of LRCK

D0: S_RESET_0

Soft reset

"0" Normal operation (default)
"1" Reset
This bit will be cleared automatically after a certain time (about 100μs).

Register (ADD: 16)

Address	Register name	D7	D6	D5	D4	D3	D2	D1	D0
16	CLOCK_ERROR	MCK_ERR_MSK_0	TEST	BCK_ERR_MSK_0	TEST			LRCK_ERR_MSK_0	TEST
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		1	0	1	1	0	0	1	0

D7: MCK_ERR_MSK_0

Mask MCK_ERROR

"0" X_ERR_STATE will be on (Low) when MCK_ERROR occurs.
"1" Mask (default)

D5: BCK_ERR_MSK_0

Mask BCK_ERROR

"0" X_ERR_STATE will be on (Low) when BCK_ERROR occurs.
"1" Mask (default)

D1: LRCK_ERR_MSK_0

Mask LRCK_ERROR

"0" X_ERR_STATE will be on (Low) when LRCK_ERROR occurs.
"1" Mask (default)

Register (ADD: 0x12 to 0x15, 0x17)

Address	Register name	D7	D6	D5	D4	D3	D2	D1	D0
12-13	TEST_00 | TEST_01	TEST							
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		*	*	*	*	*	*	*	*

Address	Register name	D7	D6	D5	D4	D3	D2	D1	D0
14	TEST_02	TEST							
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		1	0	1	1	0	0	0	0

Address	Register name	D7	D6	D5	D4	D3	D2	D1	D0
15	TEST_03	TEST							
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

Address	Register name	D7	D6	D5	D4	D3	D2	D1	D0
17	TEST_05	TEST							
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

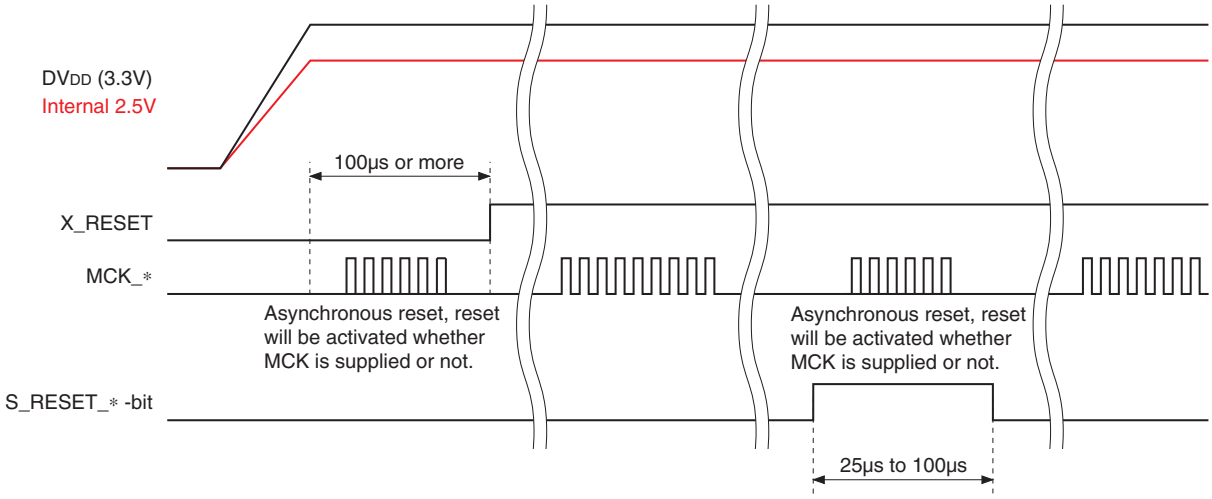
D7-0: TEST

For test. Please use them as default.

Registers (ADD: 0x18 to 0x1E)

Registers (Address: 0x18 to 0x1E) are for DAC_1.
Details will be the same as Address: 0x10 to 0x16 for DAC_0 respectively.

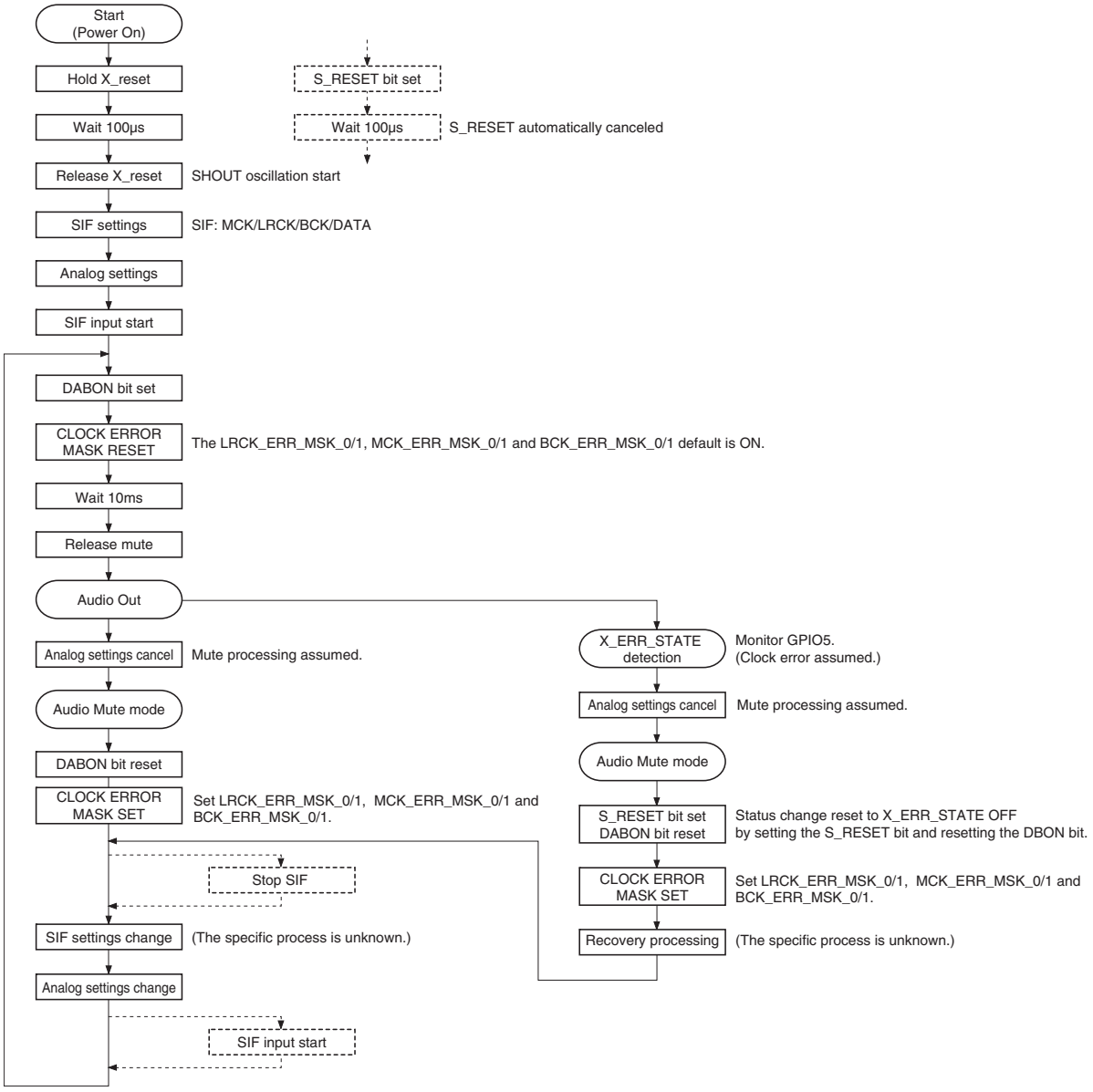
Logic Block Reset Sequence



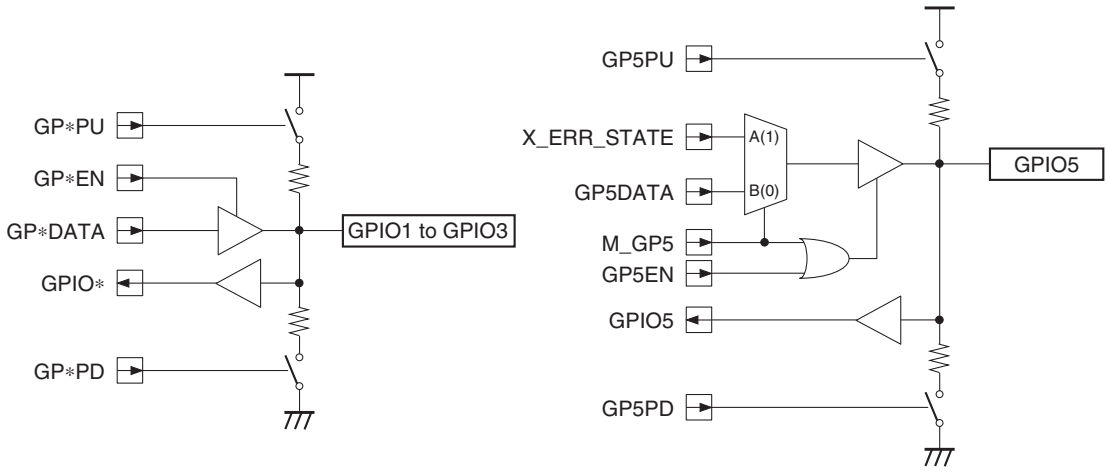
■ Reset signal valid range in the logic block

	I²C block (including registers)	DAC0	DAC1
X_RESET	Valid	Valid	Valid
S_RESET_0	Invalid	Valid	Invalid
S_RESET_1	Invalid	Invalid	Valid

DABON Sequence



GPIO1 to GPIO3, GPIO5



GPIO1 to GPIO3 **GPIO5**

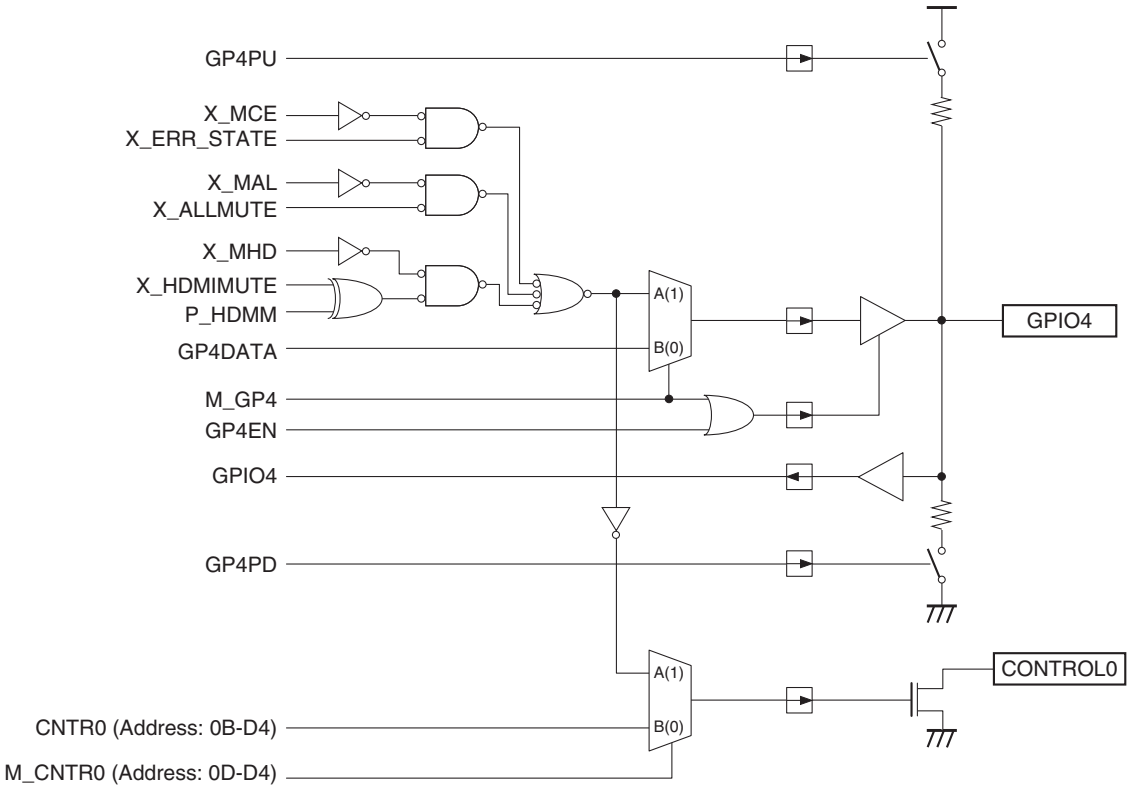
◆ The DAC0 and DAC1 clock error detection signals are output on the single pin GPIO5.

◆ This pin is shared as follows.

(1) M_GP5 = 0: Used as a normal GPIO.

(2) M_GP5 = 1: Used as the clock error detection pin.
(Select the clock error detection signal instead of GP5DATA, and set GP5EN to “1”.)

CONTROL0, GPIO4



CONTROL0, GPIO4

◆ **GPIO4 pin**

Use as a GPIO or as a dedicated mute pin (CONTROL1) can be selected by M_GP4.
(The mute signal ON (Low) factors for CONTROL1 are the X_ALLMUTE, X_HDMIMUTE and X_ERR_STATE signals. However, note that a mask bit should be added to each signals.)
Invert the X_HDMIMUTE input signal polarity by the P_HDMM signal (Address: 0x0D-D7).

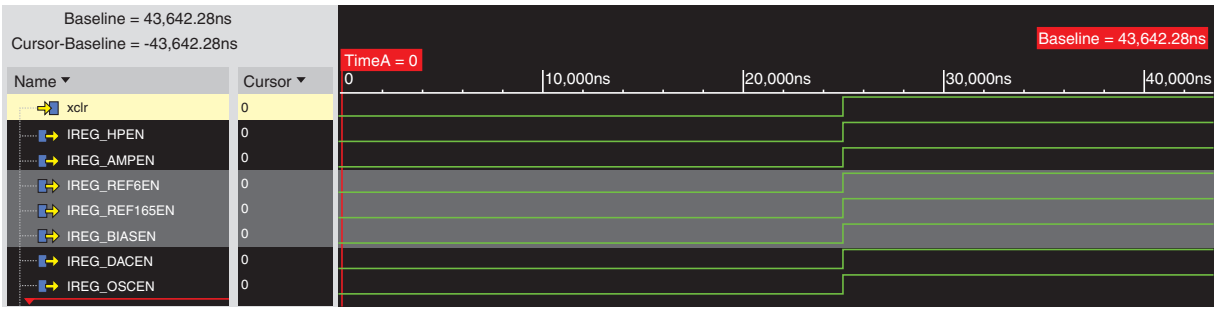
◆ **CONTROL0 pin**

CNTR0 signal (Address: 0x0B-D4) output or mute signal output can be selected by M_CNTR0 (Address: 0x0D-D4).
(The mute signal ON (Low) factors for CONTROL0 are the X_ALLMUTE, X_HDMIMUTE and X_ERR_STATE signals. However, note that a mask bit should be added to each signals.)
Invert the X_HDMIMUTE input signal polarity by the P_HDMM signal (Address: 0x0D-D7).

Address: 0x00-D4 to D0, : 0x02-D7, D6

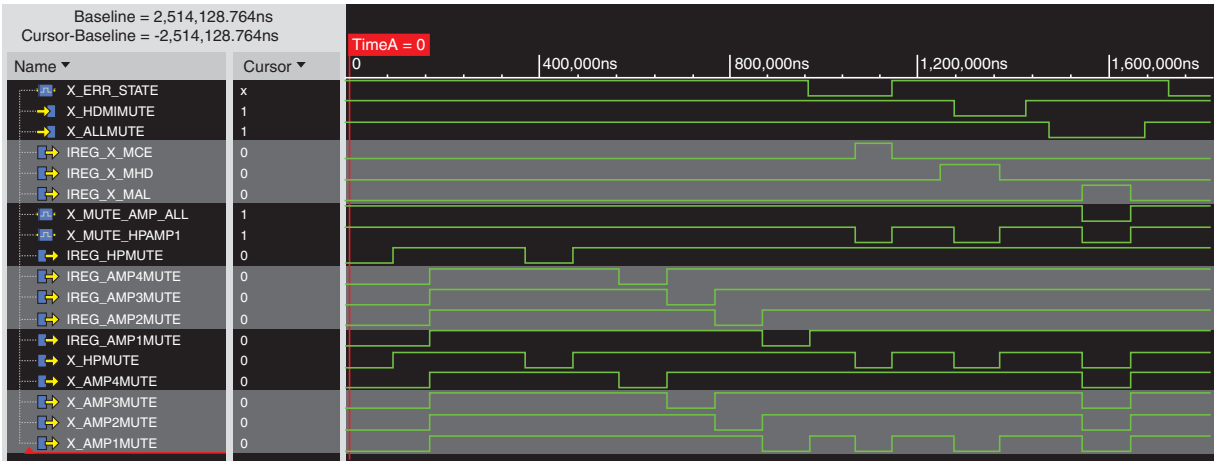
- ◆ BIASEN (0x00-D0)
- ◆ REF165EN (0x00-D1)
- ◆ REF6EN (0x00-D2)
- ◆ AMPEN (0x00-D3)
- ◆ HPEN (0x00-D4)
- ◆ DACEN (0x02-D6)
- ◆ OSCEN (0x02-D7)

Circuits corresponding to the above registers are reset at the X_RESET = Low falling edge, and Low is output. The circuit reset is released at the X_RESET = High rising edge, and at the same time the default values are output.



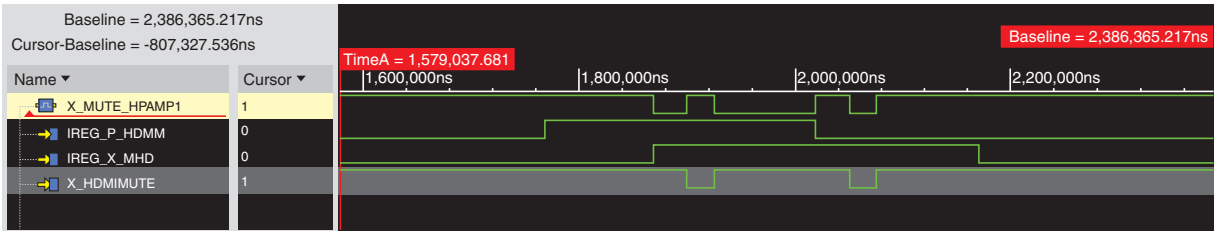
“R/W” and “W” registers other than noted above are as follows.
The circuits are reset at the X_RESET = Low falling edge, but the default values are output. The circuit reset is released at the X_RESET = High rising edge, but the default values continue to be output.

MUTE

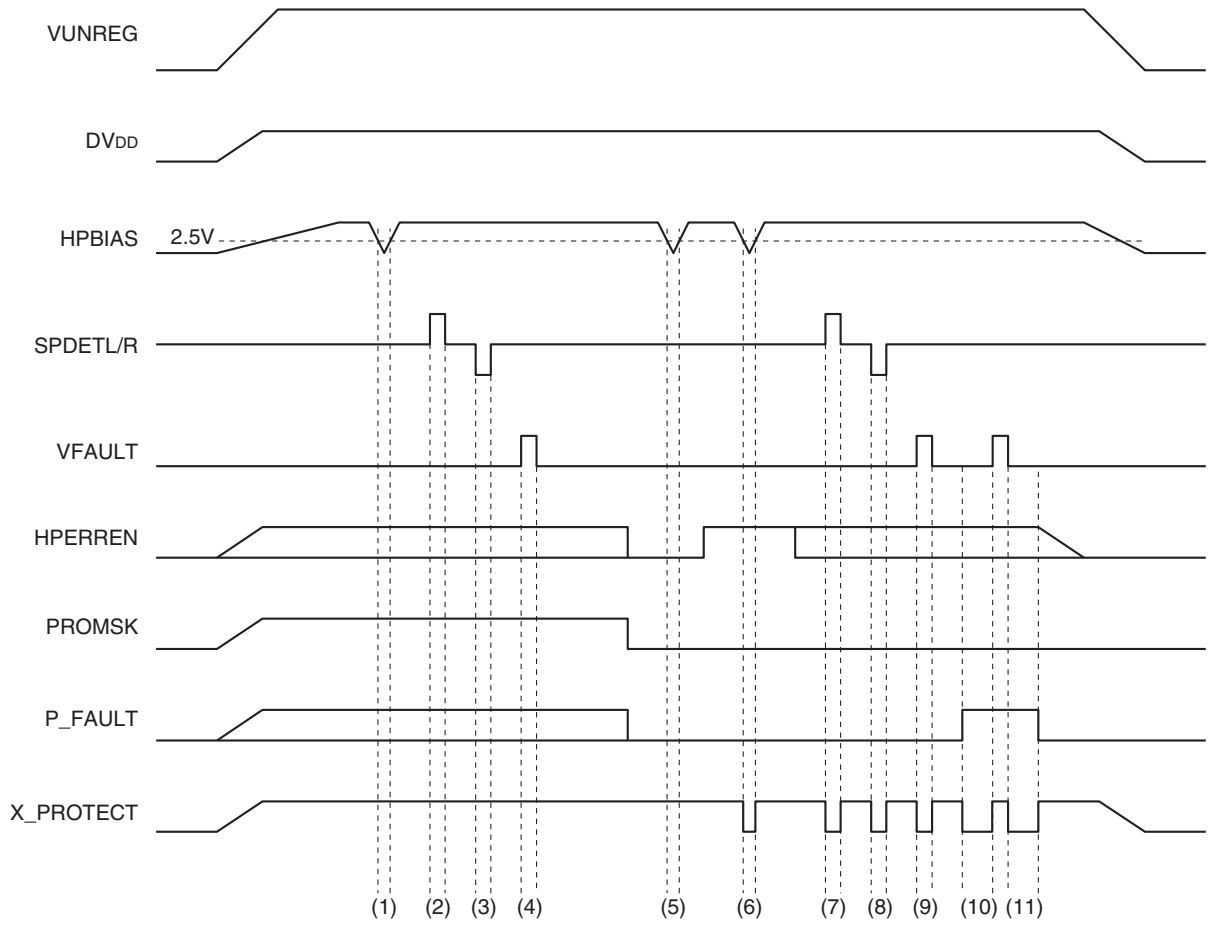


	HPMUTE	AMP4MUTE	AMP3MUTE	AMP2MUTE	AMP1MUTE	X_ERR_STATE or ~X_MCE	X_HDMIMUTE or ~X_MHD	X_ALLMUTE or ~X_MAL
X_HPAMP	yes					yes	yes	yes
X_AMP4MUTE		yes						yes
X_AMP3MUTE			yes					yes
X_AMP2MUTE				yes				yes
X_AMP1MUTE					yes	yes	yes	yes

Although not shown in the above figure, there are specifications that invert the X_HDMIMUTE input signal polarity using the P_HDMM signal (Address: 0x0D-D7).



Detector



(1) to (4): When PROMASK is (in the state of) High, all of the detecting function is disabled.

(5), (6): When PROMASK is (in the state of) Low, detecting function of HPERROR is enabled.
But when HPERREN is (in the state of) High, the function is disabled.

(7), (8): When PROMASK is (in the state of) Low, detecting function of SPDET is enabled.

(9), (10): When PROMASK is (in the state of) Low, VFAULT detection is enabled.
The state of P_FAULT controls the polarity of detecting function of VFAULT.

Restrictions During I²C Register Access

1. During Soft-Reset (Within 100μs after S_RESET_0/1 are set), write to other registers and read from them are prohibited.
2. Reset DABON_0/1 before setting S_RESET_0/1.
   Setting S_RESET_0/1 and resetting DABON_0/1 can be performed at the same time.
3. After setting DABON_0/1, reset LRCK_ERR_MSK_0/1 and MCK_ERR_MSK_0/1 and BCK_ERR_MSK_0/1.
4. Once the SMVOL0/1 registers (Address: 0x04, 0x05) have been written, continuous write (of different values) to the same registers is prohibited.

Clock Error Detection

DAC_0

Address	Register name	D7	D6	D5	D4	D3	D2	D1	D0
16	CLOCK_ERROR	MCK_ERR_MSK_0	TEST	BCK_ERR_MSK_0	TEST			LRCK_ERR_MSK_0	TEST
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		1	0	1	1	0	0	1	0

DAC_1

Address	Register name	D7	D6	D5	D4	D3	D2	D1	D0
1E	CLOCK_ERROR	MCK_ERR_MSK_1	TEST	BCK_ERR_MSK_1	TEST			LRCK_ERR_MSK_1	TEST
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		1	0	1	1	0	0	1	0

◆ When DABON_* is “1”, clock error detection is performed.
(When DABON_* is “0”, the input signal may not be reliable, so clock error detection is not performed.)

◆ When LRCK_ERR_MSK_*, BCK_ERR_MSK_* and MCK_ERR_MSK_* are set (to “1”), clock error detection is not performed for each clock. (The judgment results are masked.)

◆ The clock error detection status is reset when the S_RESET_* bit is set, or when DABON_* changes from “1” to “0”. (However, note that MCK_* must be input when DABON_* changes from “1” to “0”.)

Note) “_*”means “_0/1”.

◆ LRCK error detection

LRCK_* is monitored at the MCK (256Fs) timing, and when an unexpected frequency is detected, a LRCK error is judged and the X_ERR_STATE signal is set to ON (Low).

(1) When LRCK is not generated within the window, a LRCK error is judged and the X_ERR_STATE signal is set to ON (Low).

(2) To exit this state, stop DSP (DAB) operation.
(The error state is reset when DABON_* changes from “1” to “0”.)

(3) Setting SYNC to auto synchronization (“0”) is recommended to enable the above window processing.

(4) When a LRCK error occurs during auto synchronization, the DAB is resynchronized to LRCK, but the resynchronize operation is masked with FORCEMASK.
(When the unsynchronized state continues, input audio signal acquisition may fail, or noise may be generated in the audio output.)

(5) When the LRCK_* - stop - state (MCK_* (256Fs) must be input as a prerequisite) is detected and LRCK is determined to be stopped, a LRCK error is judged and the X_ERR_STATE signal is set to ON (Low). A watch dog counter that employs MCK (256fs) as a clock and LRCK_* falling edge as a reset, is used for judgment. The judgment reference is that this counter reaches “511”.

(6) When LRCK_ERR_MSK_* is “1”, LRCK error detection is not performed.
(The judgment results are masked.)

(7) The LRCK_ERROR_* detection default is OFF.

◆ **BCK error detection**

BCK_*/3 is monitored at the MCK (256Fs) timing, and when BCK is stopped, a BCK error is judged and the X_ERR_STATE signal is set to ON (Low).

(1) When the BCK _* - stop - state (MCK_* (256Fs) must be input as a prerequisite) is detected and BCK is determined to be stopped, a BCK error is judged and the X_ERR_STATE signal is set to ON (Low). A watch dog counter that employs MCK (256fs) as a clock and BCK_*/3 signal falling edge as a reset, is used for judgment. The judgment reference is that this counter reaches “47”.

(2) To exit this state, stop DAB operation. (The error state is reset when DABON_* changes from “1” to “0”.)

(3) When BCK_ERR_MSK_* is “1”, BCK error detection is not performed.

(4) The BCK_ERROR_* detection default is OFF.

◆ **MCK error detection**

MCK_* (256Fs) is monitored at the SHOUT timing, and when MCK_* (256Fs) does not toggle, a MCK error is judged and the X_ERR_STATE signal is set to ON (Low).

(1) When the MCK_* - stop - state is detected and MCK is determined to be stopped, a MCK error is judged and the X_ERR_STATE signal is set to ON (Low).

(2) To exit this state, stop DAB operation.
(The error state is reset when DABON_* changes from “1” to “0”.)

(3) When MCK_ERR_MSK_* is “1”, MCK error detection is not performed.

(4) The MCK_ERROR_* detection default is OFF.

(5) MCK is stopped, so the DAB must be reset to return to the operating state. Reset the DAB using S_RESET.

◆ **X_ERR_STATE: Clock error detection signal**

X_ERR_STATE = (~LRCK_ERR_0 or LRCK_ERR_MSK_0)
and (~LRCK_ERR_1 or LRCK_ERR_MSK_1)
and (~BCK_ERR_0 or BCK_ERR_MSK_0)
and (~BCK_ERR_1 or BCK_ERR_MSK_1)
and (~MCK_ERR_0 or MCK_ERR_MSK_0)
and (~MCK_ERR_1 or MCK_ERR_MSK_1)

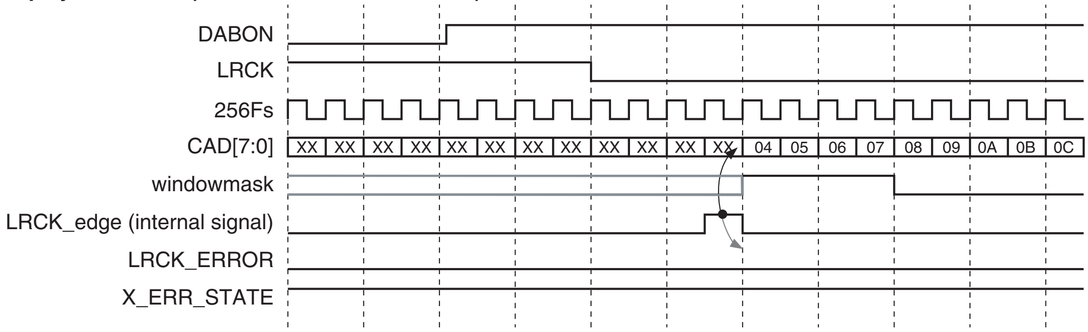
LRCK Error Detection

◆ LRCK error detection (1/6)

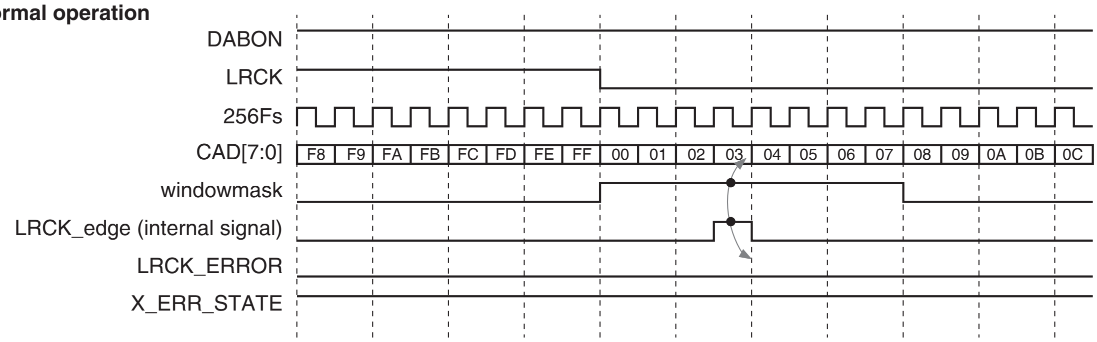
(1) When the DABON bit is set ("0" → "1"), the DAB starts to synchronize with LRCK. The DAB is synchronized with the first LRCK generated after DABON goes to "1", and runs freely thereafter.

(2) The free running state continues as long as LRCK (LRCK_edge) is generated within the window.

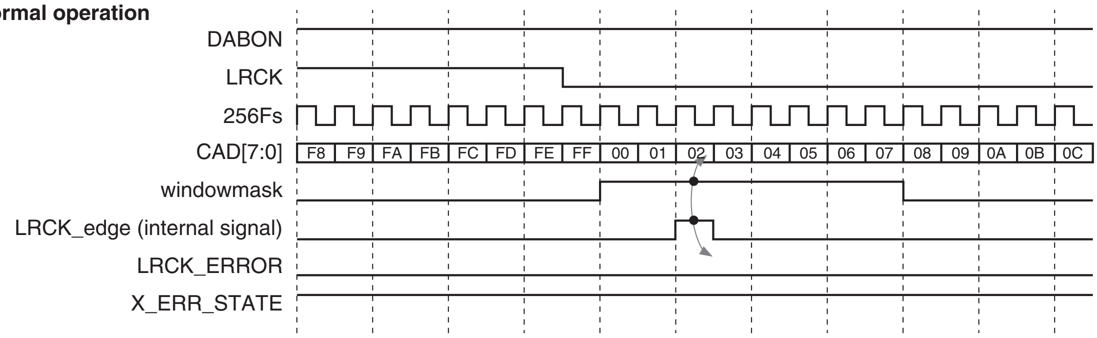
When playback starts (first LRCK after DABON = 1)



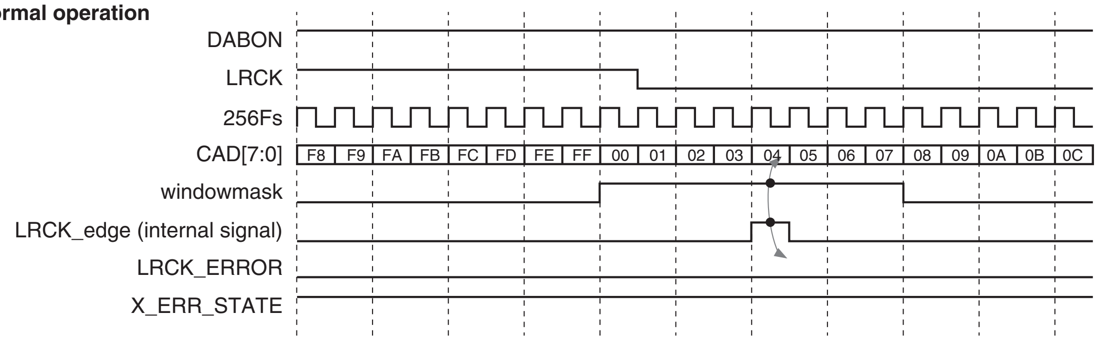
Normal operation



Normal operation



Normal operation

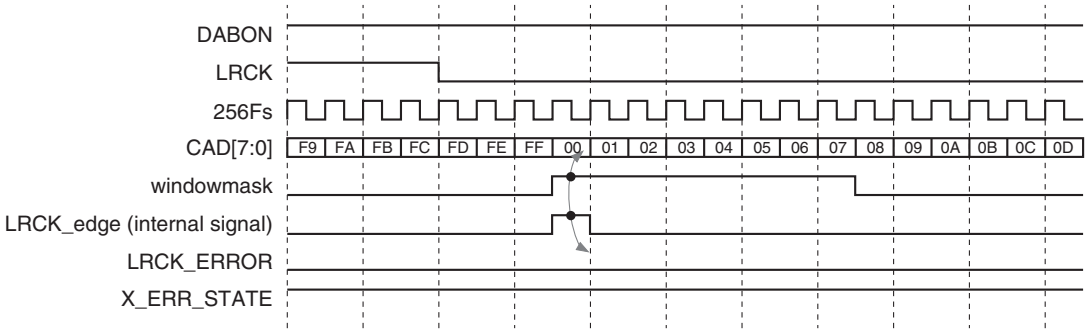


◆ **LRCK error detection (2/6)**

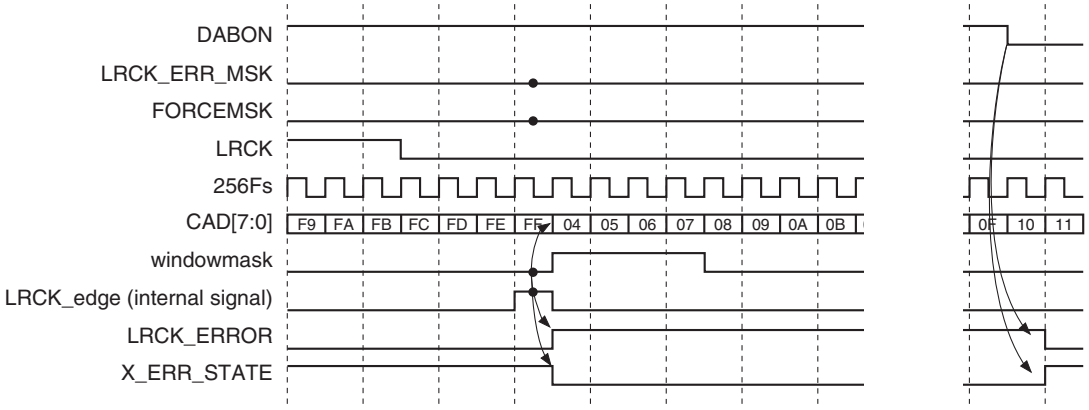
(1) When LRCK advances relative to the window for some reason and LRCK (LRCK_edge) is generated at a timing outside the window, a LRCK error is judged.

(2) When LRCK_ERR_MSK is “1”, LRCK error detection is masked, but noise may be generated in the audio output.

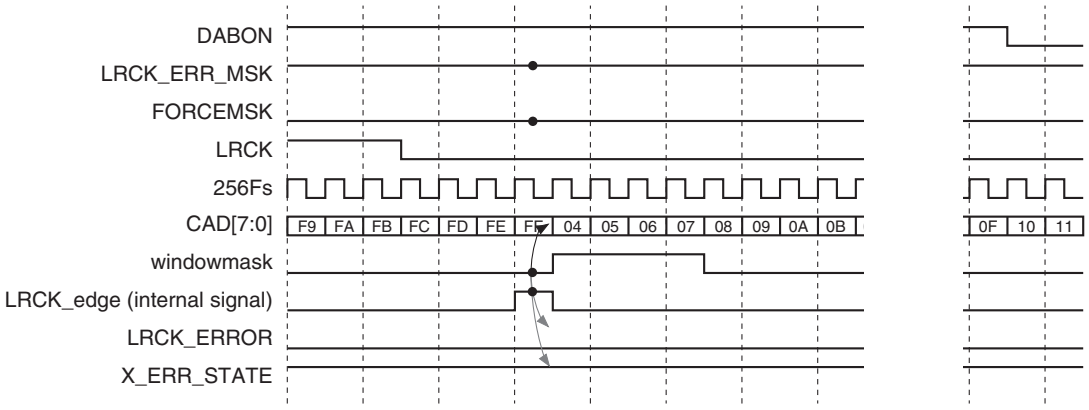
Normal operation (LRCK advances relative to the window for some reason)



LRCK_ERROR generated (LRCK_ERR_MSK = 0, FORCEMASK = 0) → Noise generated



LRCK_ERROR generated (LRCK_ERR_MSK = 1, FORCEMASK = 0) → Noise generated



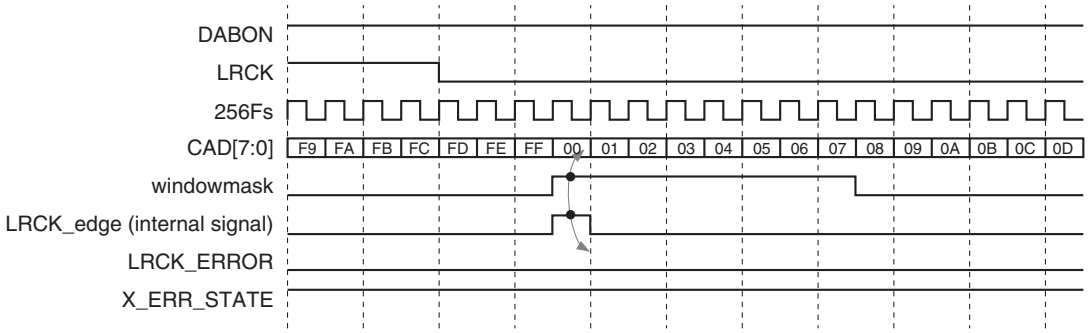
◆ **LRCK error detection (3/6)**

(1) When LRCK advances relative to the window for some reason and LRCK (LRCK_edge) is generated at a timing outside the window, a LRCK error is judged.

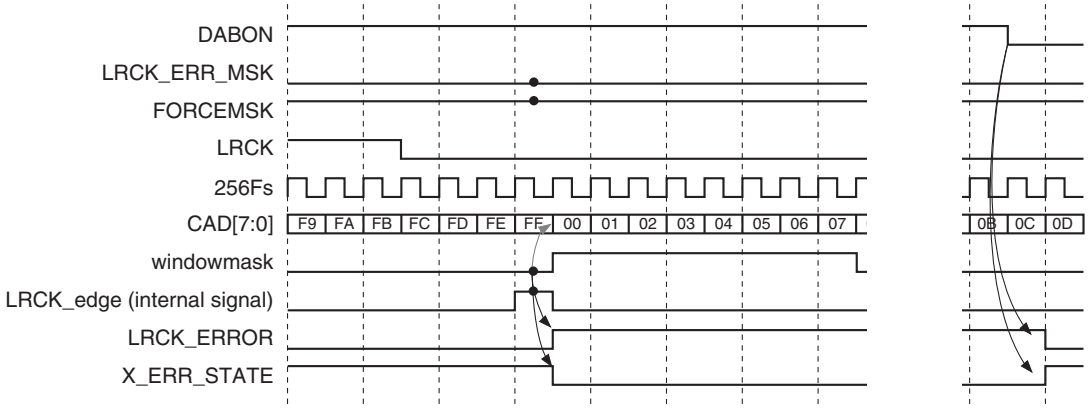
(2) When LRCK_ERR_MSK is “1”, LRCK error detection is masked.

(3) When FORCEMASK is “1”, DAB and LRCK synchronization is lost. When this unsynchronized state continues, input audio signal loading may fail, or noise may be generated in the audio output.

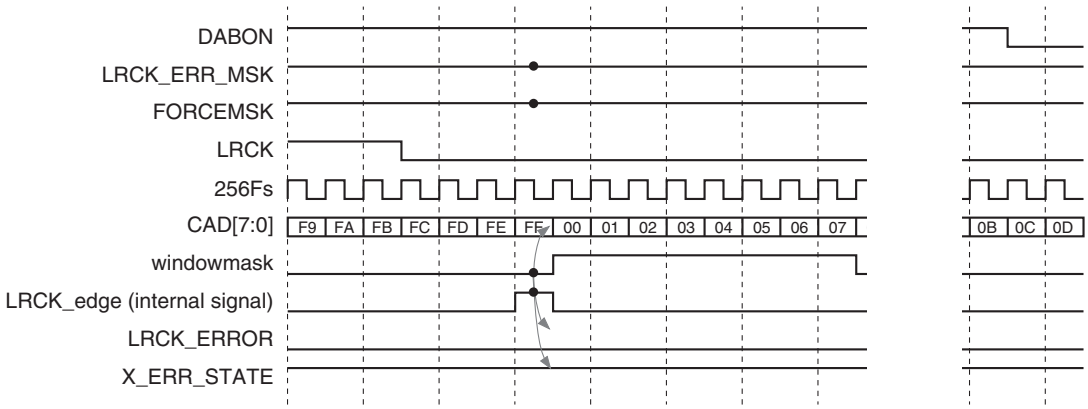
Normal operation (LRCK advances relative to the window for some reason)



LRCK_ERROR generated (LRCK_ERR_MSK = 0, FORCEMASK = 1) → DSP and LRCK synchronization lost



LRCK_ERROR generated (LRCK_ERR_MSK = 1, FORCEMASK = 1) → DSP and LRCK synchronization lost

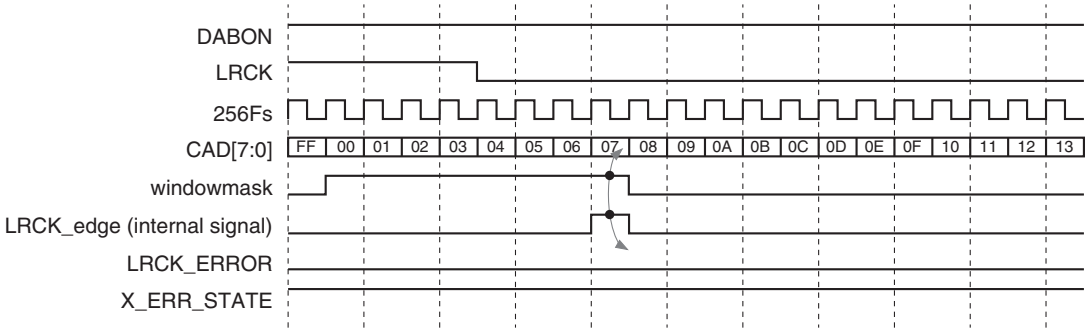


◆ **LRCK error detection (4/6)**

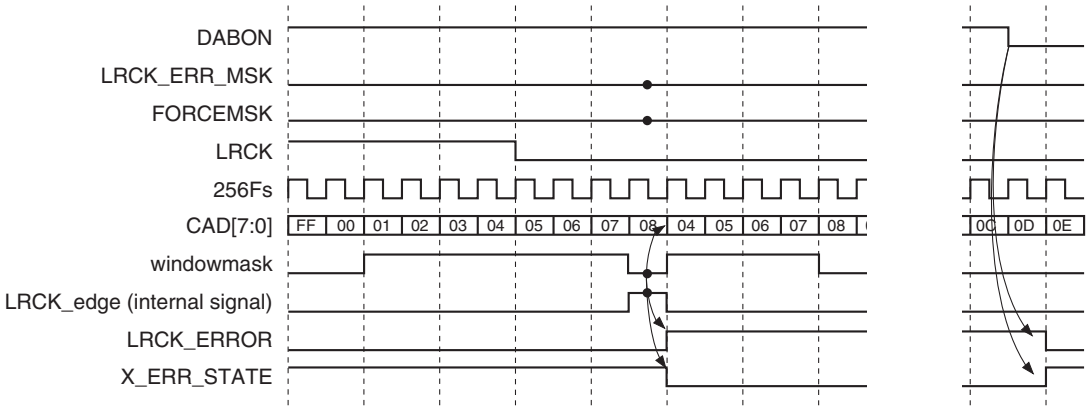
(1) When LRCK is delayed relative to the window for some reason and LRCK (LRCK_edge) is generated at a timing outside the window, a LRCK error is judged.

(2) When LRCK_ERR_MSK is “1”, LRCK error detection is masked, but noise may be generated in the audio output.

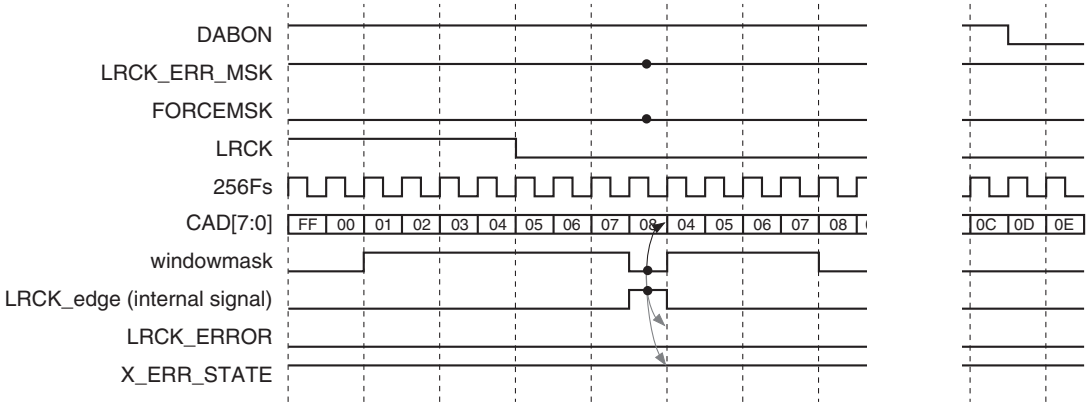
Normal operation (LRCK delayed relative to the window for some reason)



LRCK_ERROR generated (LRCK_ERR_MSK = 0, FORCEMASK = 0) → Noise generated



LRCK_ERROR generated (LRCK_ERR_MSK = 1, FORCEMASK = 0) → Noise generated



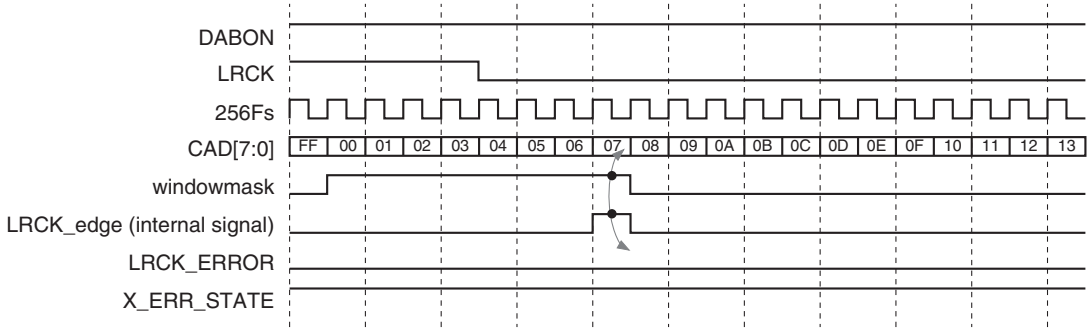
◆ **LRCK error detection (5/6)**

(1) When LRCK is delayed relative to the window for some reason and LRCK (LRCK_edge) is generated at a timing outside the window, a LRCK error is judged.

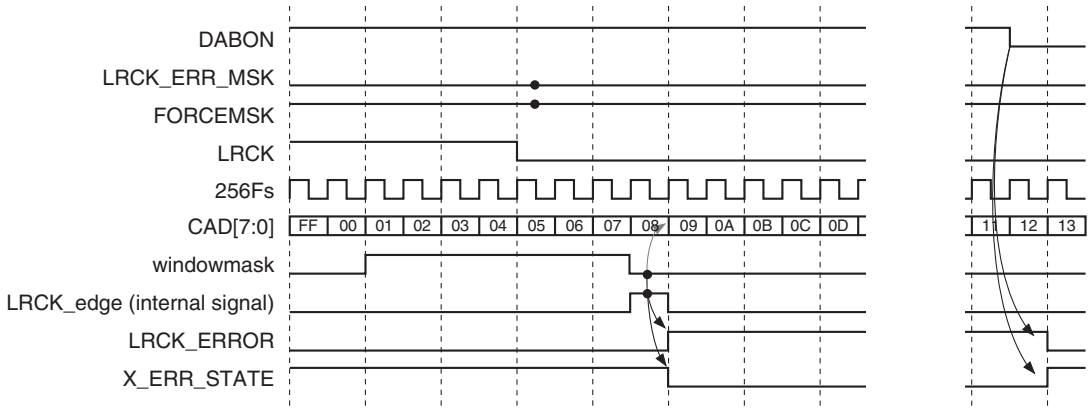
(2) When LRCK_ERR_MSK is “1”, LRCK error detection is masked.

(3) When FORCEMASK is “1”, DAB and LRCK synchronization is lost. When this unsynchronized state continues, input audio signal loading may fail, or noise may be generated in the audio output.

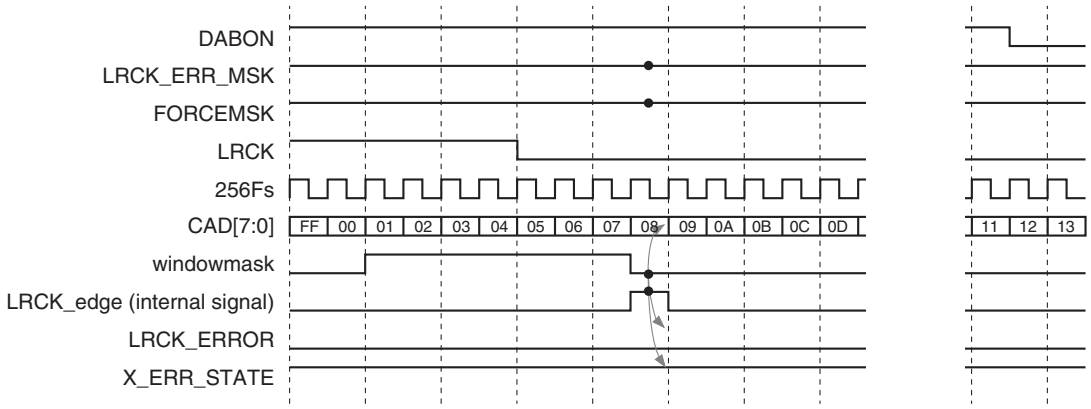
Normal operation (LRCK delayed relative to the window for some reason)



LRCK_ERROR generated (LRCK_ERR_MSK = 0, FORCEMASK = 1) → DSP and LRCK synchronization lost



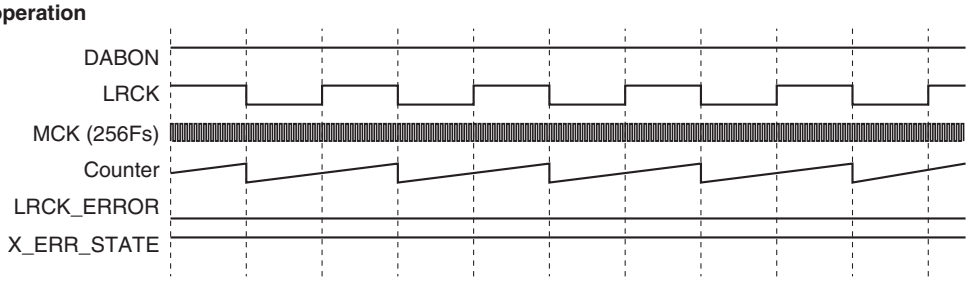
LRCK_ERROR generated (LRCK_ERR_MSK = 1, FORCEMASK = 1) → DSP and LRCK synchronization lost



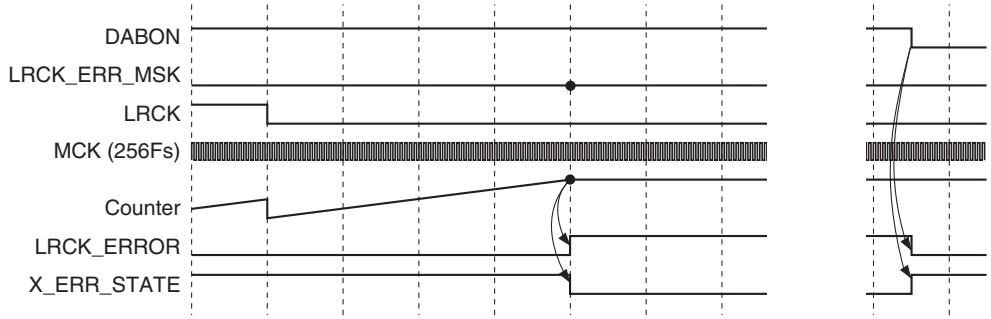
◆ **LRCK error detection (6/6)**

(1) LRCK generation is monitored at the MCK (256Fs) watchdog timer, and when LRCK is not generated, an LRCK error is judged.

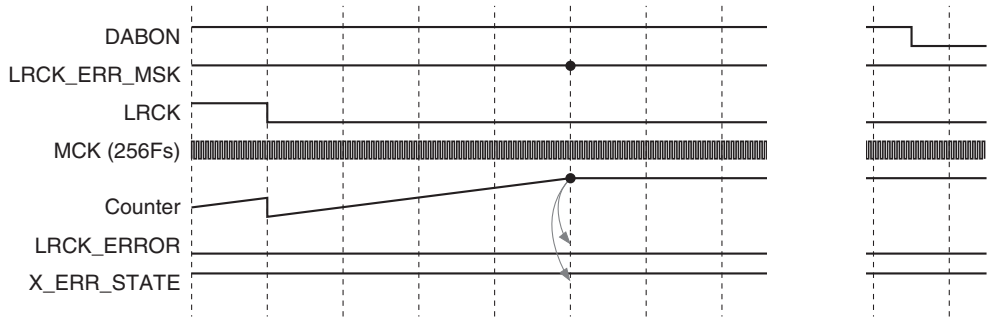
Normal operation



LRCK_ERROR generated (LRCK_ERR_MSK = 0)



LRCK_ERROR generated (LRCK_ERR_MSK = 1)

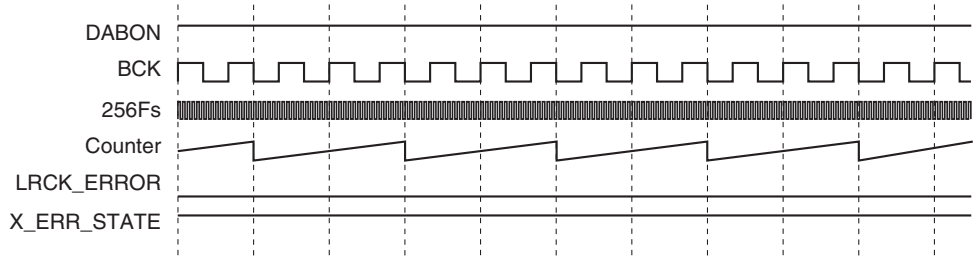


BCK Error Detection

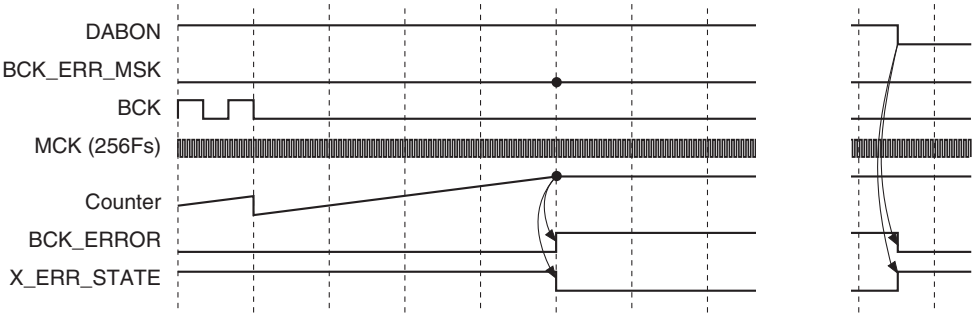
◆ BCK error detection

(1) BCK generation is monitored at the MCK (256Fs) watchdog timer, and when BCK is not generated, a BCK error is judged.

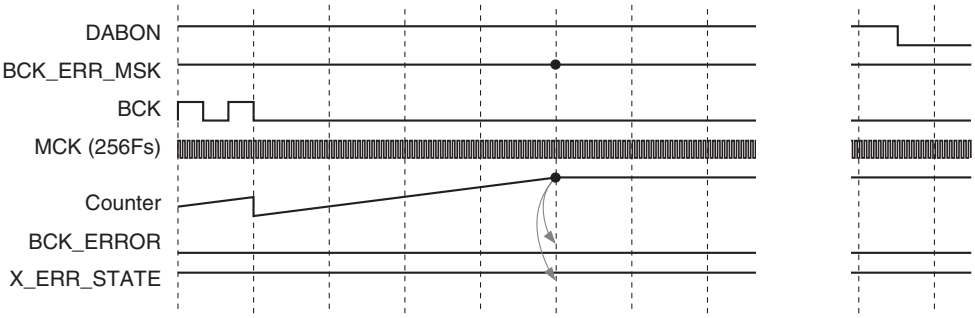
Normal operation



BCK_ERROR generated (BCK_ERR_MSK = 0)



BCK_ERROR generated (BCK_ERR_MSK = 1)

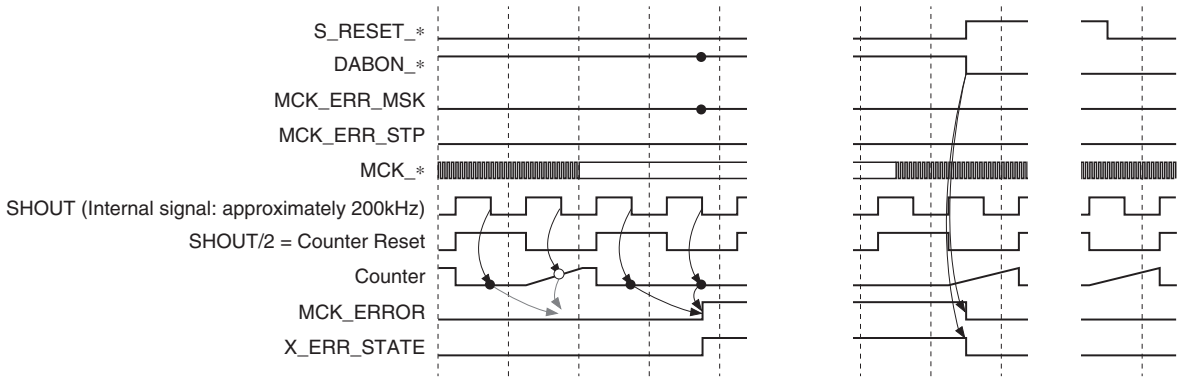


MCK Error Detection

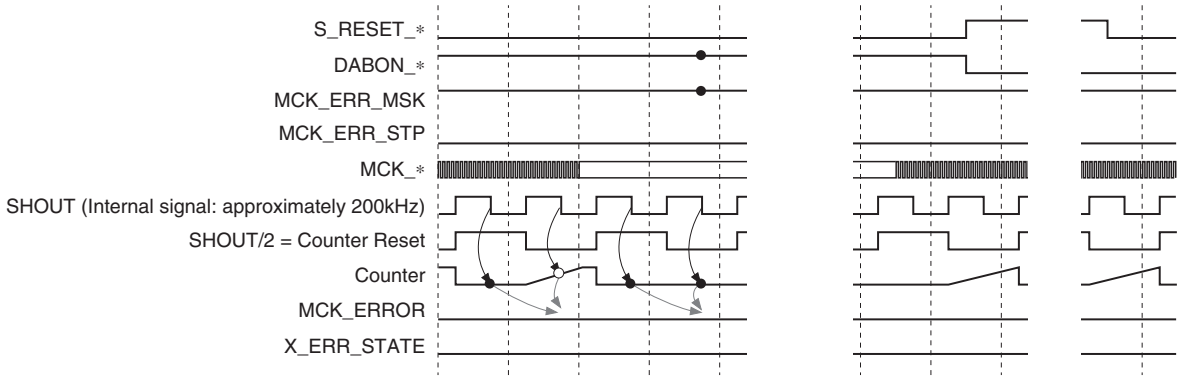
◆ MCK error detection

(1) MCK generation is monitored at the SHOUT watchdog timer, and when MCK is not generated, a MCK error is judged.

MCK_ERROR generated (MCK_ERR_MSK = 0)



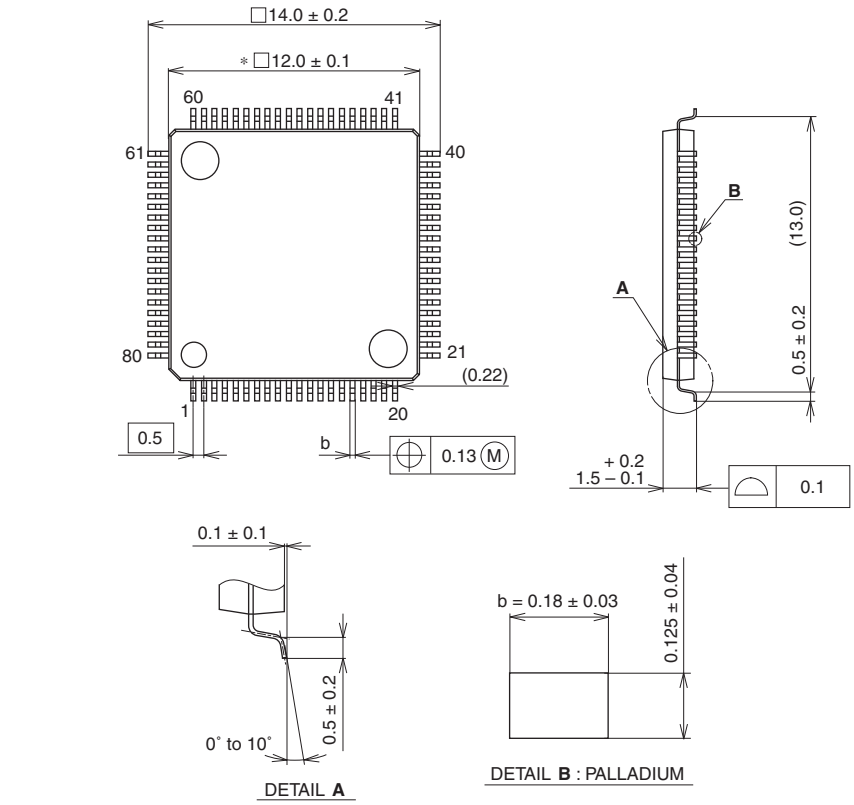
MCK_ERROR generated (MCK_ERR_MSK = 1)



Package Outline

(Unit: mm)
House Code: 75333483/75333300

80PIN LQFP (PLASTIC)



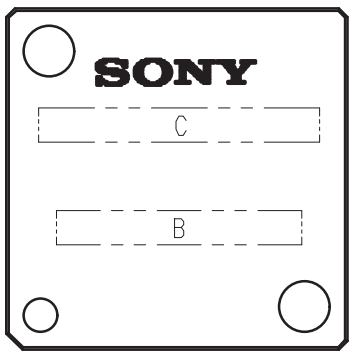
NOTE: Dimension "∗" does not include mold protrusion.

SONY CODE	LQFP-80P-L01
EIAJ CODE	P-LQFP80-12x12-0.5
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	PALLADIUM PLATING
LEAD MATERIAL	COPPER ALLOY
PACKAGE MASS	0.5g

Marking



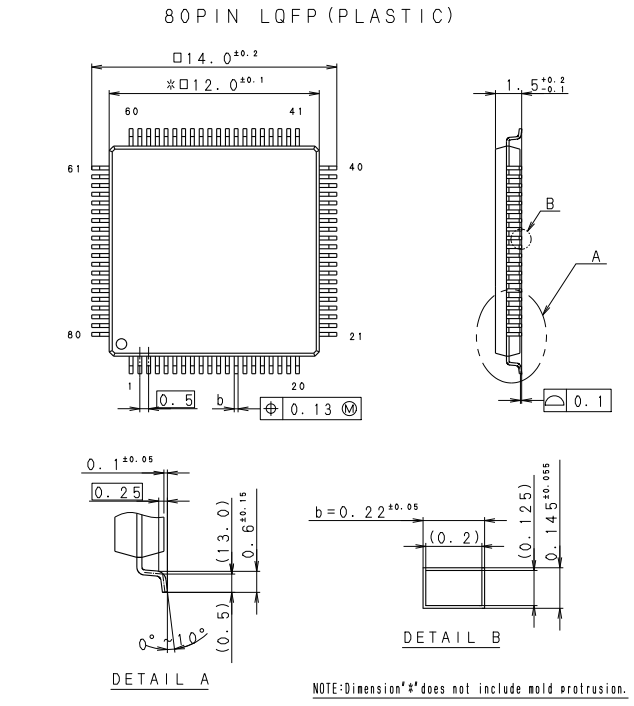
C:CXA3803R
B: Lot No. (Max. 7)

□□□□□□□

管理記号（Control No.）
製造週（Week manufactured）
製造年（西暦下 1 桁）
（Year manufactured）

Package Outline

(Unit: mm)
House Code: 75340634



NOTE:Dimension"*"does not include mold protrusion.

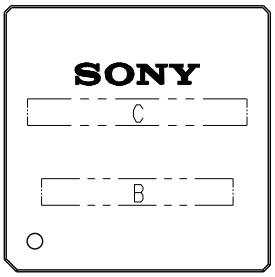
PACKAGE STRUCTURE

SONY CODE	LQFP-80P-L281
JEITA CODE	P-LQFP80-12X12-0.5
JEDEC CODE	————

PACKAGE MATERIAL	EPOXY RESIN
TERMINAL TREATMENT	Sn PLATING
TERMINAL MATERIAL	COPPER ALLOY
PACKAGE MASS	0.5g

PART No. AP-2000-80QAC2	Rev. 0
ISSUED 11.12.07	REVISED
PRODUCTION LINE	COMPILING DIV. SONY SEMICONDUCTOR.
REMARKS PKG CODE:R-80-TAC	

Marking



MARKING C: CXA3803R

注1) C部は製品名(Max10文字)を配置する. (10文字を越える場合は製品名省略標示規定に従う.)
2) B部はロット番号(Max7文字)を配置する.

< INSTRUCTIONS >
1) TYPE NO. (MAX 10 CHARACTERS) IN SECTION C.
(FOR MORE THAN 10 CHARACTERS FOLLOW RULES FOR ABBREVIATIONS.)
2) LOT NO. (MAX 7 CHARACTERS) IN SECTION B.