SONY

Zero-IF Tuner IC for Digital Satellite Broadcast

CXD2832AER

Description

The CXD2832AER is an IC developed for direct orthogonal detection of 1st IF signal (1 to 2 GHz) from RF converter block in a digital satellite broadcast receiver system. The CXD2832AER incorporates all the functions (LNA , RF gain control amplifier, VCO, mixer, baseband LPF, baseband gain control amplifier, tuning PLL) required for a satellite broadcast tuner.

Applications

- ◆ Digital TV
- ◆ STB for digital satellite broadcasting
- ◆ BD recorder

Features

- ◆ Low noise figure : 5 dB (typ.)
- ◆ Low power consumption: 400 mW (typ.) (Includes internal LNA circuit)
- ◆ Clock output for a demodulator LSI
- ◆ Input pin for controlling of power saving mode
- ◆ Small package: 28 pin VQFN 5 mm × 5 mm (0.5 mm pitch)

Absolute Maximum Ratings

◆ Supply voltage	AV_{DD}, DV_{DD}	-0.3 to +3.6 V	(Ta = 25 ˚C)
◆ Storage temperature	Tstg	-55 to +150 ˚C	

Operating Conditions

◆ Supply voltage	AV_{DD}, DV_{DD}	2.375 to 3.465 V	
◆ Operating temperature	Topr1	-20 to +85 ˚C	(AV_{DD}, DV_{DD} ≤ 2.8 V)
◆ Operating temperature	Topr2	-20 to +75 ˚C	(AV_{DD}, DV_{DD} > 2.8 V)
◆ Allowable power dissipation		2.2 W	(30 mm × 60 mm, t = 1.0 mm, mounted on 2 layer board)

Note) This IC has pins whose electrostatic discharge strength is weak as the high-frequency process is used. Handle the IC with care.

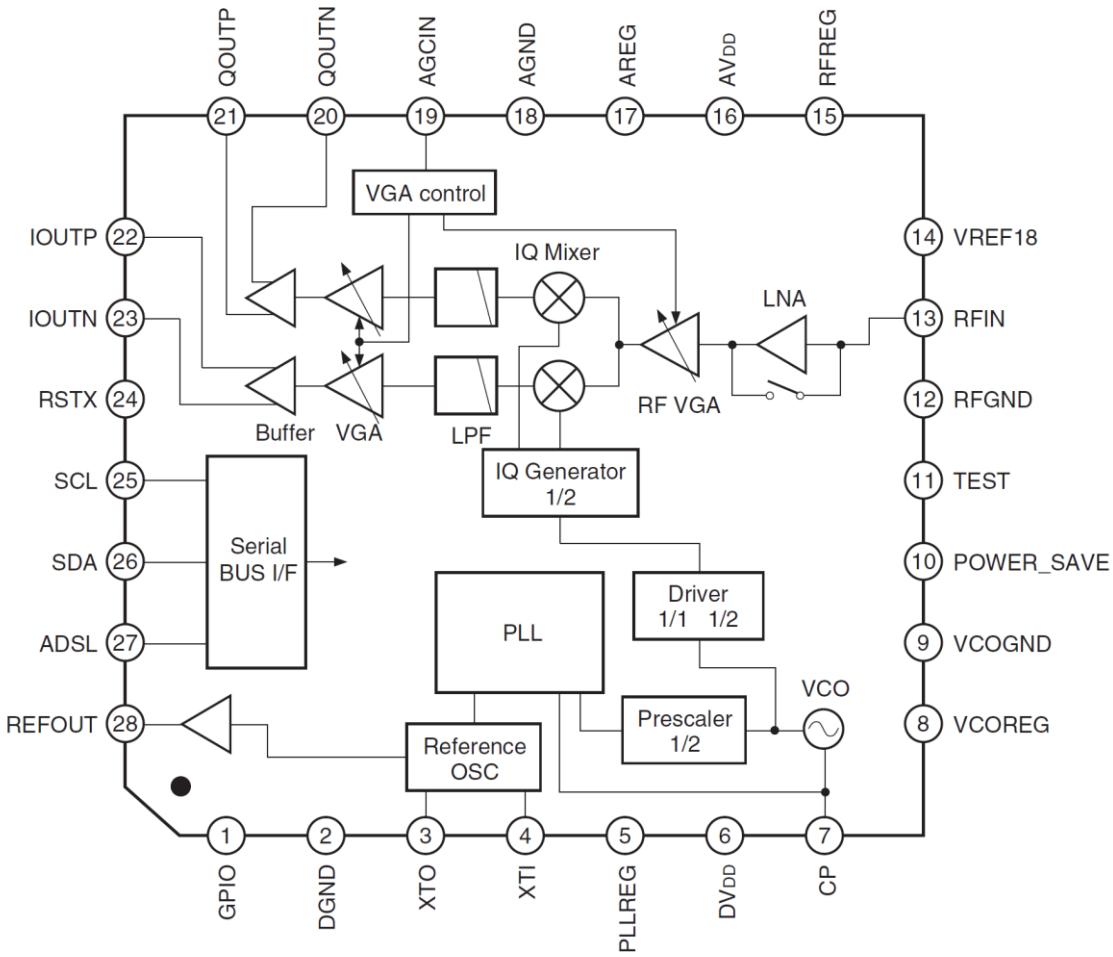
E12513

Contents

Basic Specifications

Receiving frequency range	950 to 2150	MHz
Input signal range (internal LNA enabled)	-85 to -10	dBm
Power supply voltage	2.5 or 3.3	V
Standard baseband output level	0.7	Vp-p
Tuning frequency step (PLL comparison frequency)	1	MHz
Baseband bandwidth	5 to 36 (1 MHz step variable)	MHz
Clock frequency	16 or 24 or 27	MHz

Pin configuration and Block Diagram



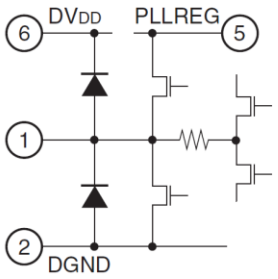
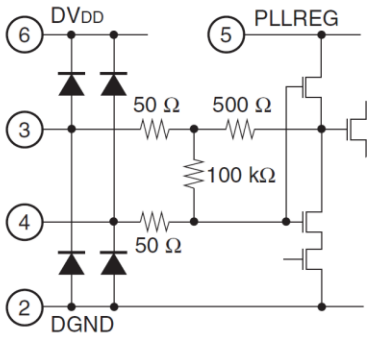
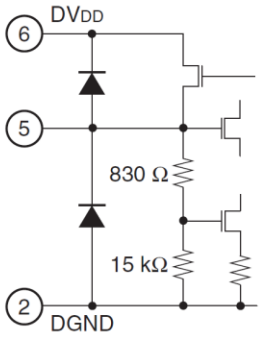
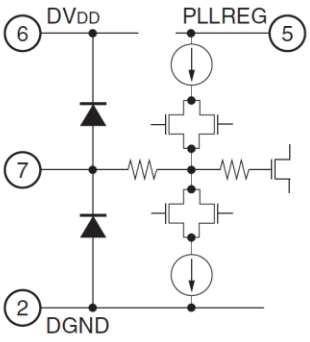
Description of Block Diagram

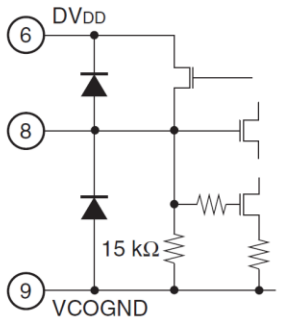
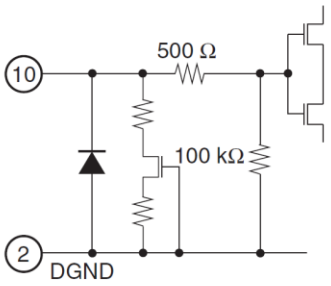
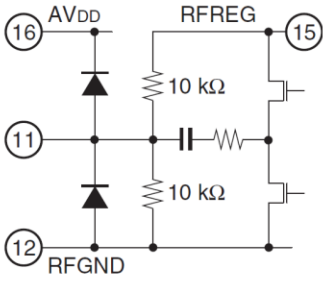
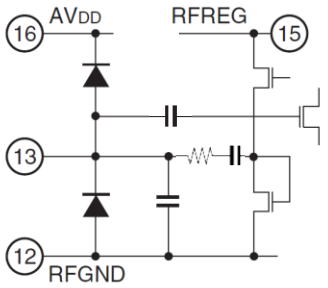
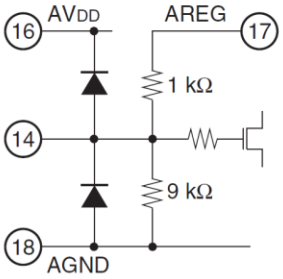
The block names shown in the block diagram above have the following functions.

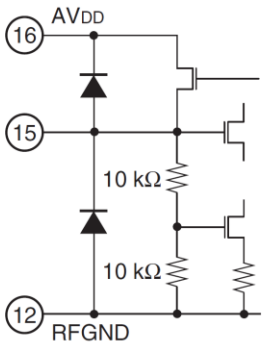
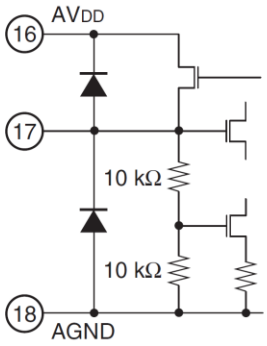
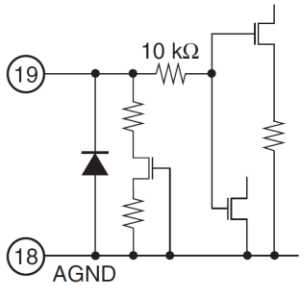
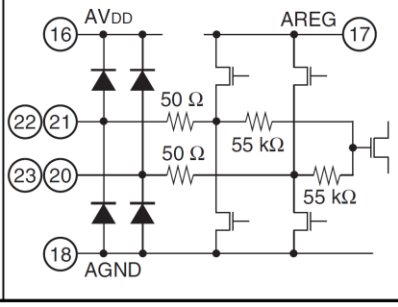
Reference OSC	Crystal oscillation circuit for reference clock
Serial BUS I/F	Interface block for serial bus
PLL	Tuning PLL
Prescaler	PLL fixed divider
VCO	VCO circuit for local signal
Divider	Frequency divider for local signal
IQ Generator	Frequency divider for IQ signal
LNA	Low Noise Amplifier
RF VGA	Gain control amplifier for RF signal
IQ Mixer	Quadrature demodulator (Mixer circuit)
LPF	Low Pass Filter
VGA	Gain control amplifier for baseband signal
Buffer	Output buffer circuit for baseband signal
VGA control	gain variation characteristic control circuit

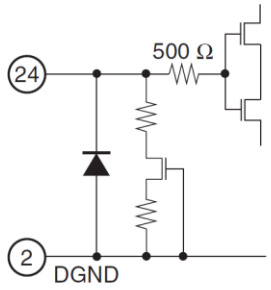
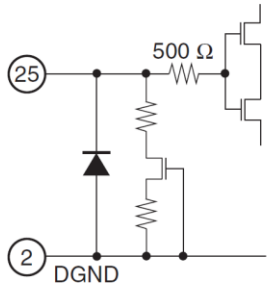
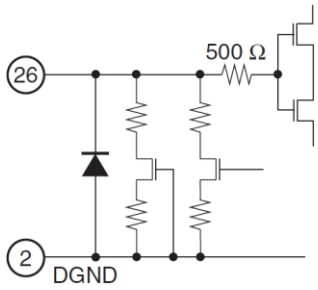
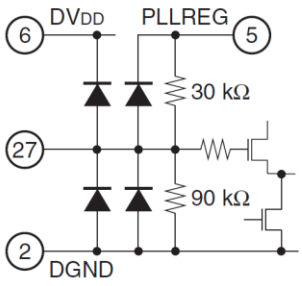
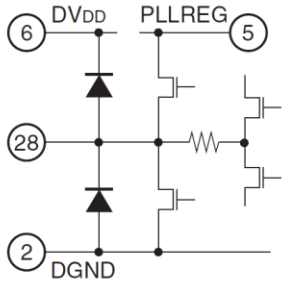
Pin Description and Input / Output Pin Equivalent Circuit

(Pin voltage shows typical DC voltage value when AGCI = 0 V)

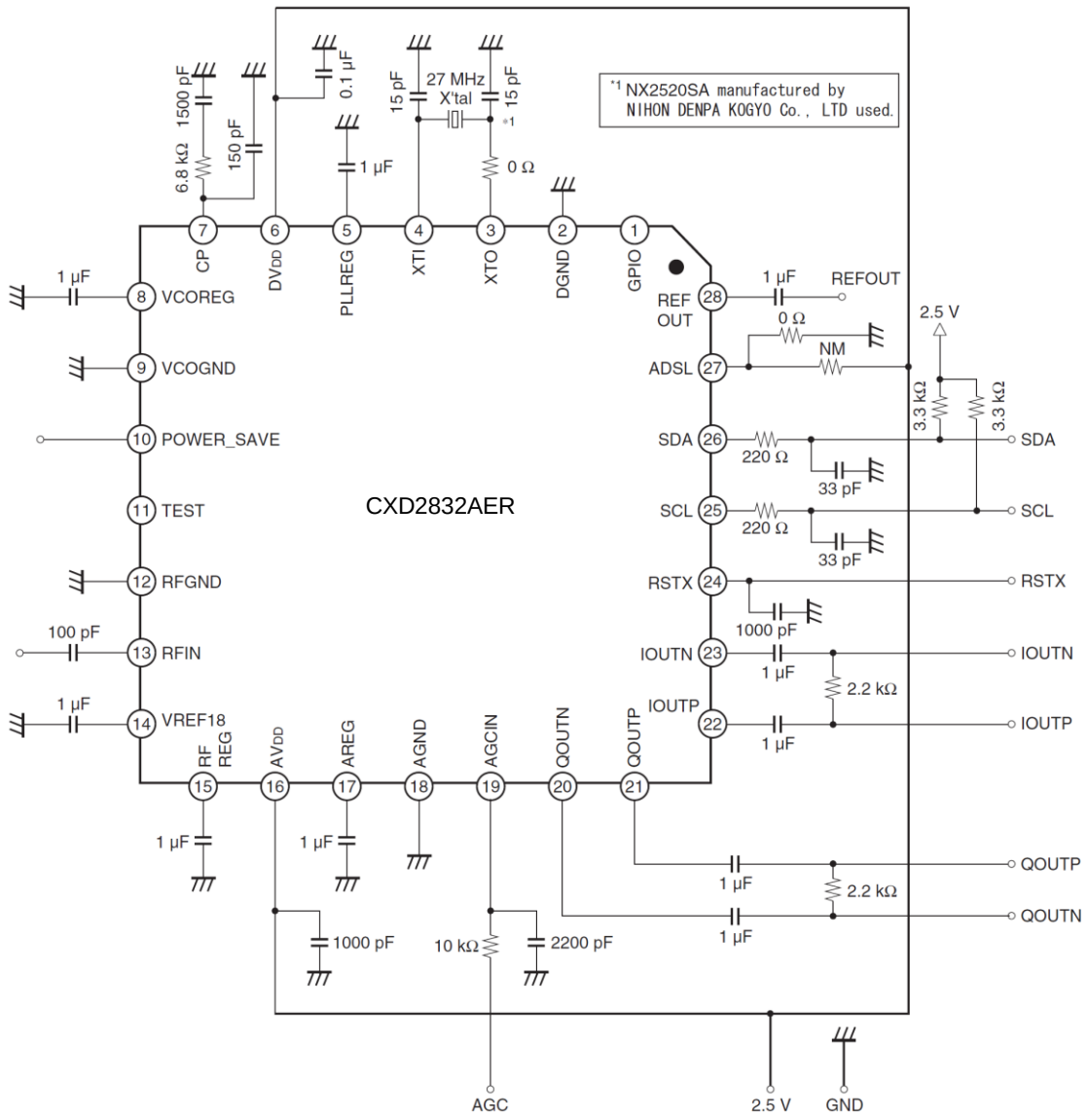
Pin No	Symbol	Pin voltage [V]	Equivalent circuit	Description
1	GPIO	0/1.9		General purpose output
2	DGND	0		GND Pin for PLL and logic circuits
3, 4	XTO XTI	0.6 0.6		Crystal oscillator connection for reference clock. When it is used as external clock input instead of crystal connection, please use XTI pin as clock input, and connect XTO to GND via capacitance.
5	PLLREG	1.9		External capacitor connection pin for regulator of PLL circuit. Please connect GND via capacitor of 1 μF or more.
6	DVDD	2.5		PLL and logic power supply
7	CP	0.9		Charge pump output for tuning PLL

Pin No	Symbol	Pin voltage [V]	Equivalent circuit	Description
8	VCOREG	1.9		External capacitor connection pin for regulator of VCO circuit. Please connect GND via capacitor of 1 μF or more.
9	VCOGND	0		GND for VCO
10	POWER_SAVE	0/2.5/3.3		Power save control pin. Crystal oscillator stops and internal circuit changes to power saving mode when High.
11	TEST	1.0		Test pin No connect
12	RFGND	0		GND for RF circuits
13	RFIN	0		Input for RF signal
14	VREF18	1.8		Connecting capacitor for internal reference voltage. Please connect GND via capacitor of 1 μF or more.

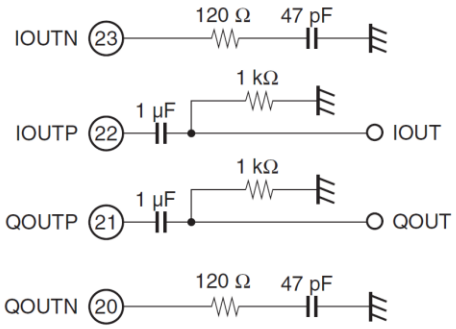
Pin No	Symbol	Pin voltage [V]	Equivalent circuit	Description
15	RFREG	2.0		External capacitor connection pin for regulator of RF circuit. Please connect GND via capacitor of 1 µF or more.
16	AVDD	2.5		
17	AREG	2.0		External capacitor connection pin for regulator of base band circuit. Please connect GND via capacitor of 1 µF or more.
18	AGND	0		GND for analog circuits
19	AGCIN	0 to 3.3		Gain control pin for internal VGA circuits.
20 21 22 23	QOUTN QOUTP IOUTP IOUTN	1.0		Baseband signal output

Pin No	Symbol	Pin voltage [V]	Equivalent circuit	Description
24	RSTX	Hi-Z		Negative logic hardware reset pin Hardware reset is necessary when power up.
25	SCL	Hi-Z		Clock input for serial bus
26	SDA	Hi-Z		Data input and output for serial bus
27	ADSL	0 to 2.2		Serial bus slave address setting
28	REFOUT	Hi-Z		Reference clock signal output

Electrical Characteristics Measurement Circuit



Measurement circuit for single-end output.



Electrical Characteristics

DC and analog characteristics

See the Electrical Characteristics Measurement Circuit on page 9

Circuit voltage = 2.5 V, Ta = 25 ˚C

Unless otherwise specified the measuring condition is RF frequency = 2150 MHz, full gain (AGCI = 0 V)

DC Items

Item	Symbol	Condition	Min	Typ.	Max	Unit
Circuit current-1	IDD-1	Current at DV_{DD} pin	48	60	70	mA
Circuit current-2	IDD-2	Current at AV_{DD} pin	72	97	125	mA
Circuit current-3	IDD-3	Current at AV_{DD} pin when internal LNA bypassed	61	79	105	mA
Power save current 1	PSIDD-1	DV_{DD} pin when clock is disabled		1	3	mA
Power save current 2	PSIDD-2	AV_{DD} pin when LNA is enabled	14	27	40	mA
Power save current 3	PSIDD-3	AV_{DD} pin when LNA is bypassed	3	9	20	mA
SDA, SCL, RSTX, POWER_SAVE pin						
High level input voltage	VIH		2.0		3.6	V
Low level input voltage	VIL		GND		1	V
SDA pin						
Low level output voltage	VOL1	Source current : 3 mA	GND		0.4	V
GPIO pin						
High level output voltage	VPH	Source current : 3 mA	1.7	1.9	2.1	V
Low level output voltage	VPL	Sink current:3 mA	0.0		0.2	V
Drive current	IGD	Source/Sink current			3	mA
AGCIN pin						
Input voltage range	VIAH		0		3.6	V
Input current	ILAH	AGCIN = 3.3 V		160	250	µA
OTHER						
Input current of RSTX pin	ILRH	Input Voltage = 3.3 V			10	µA
Input current of POWER_SAVE	ILAH	Input Voltage = 3.3 V			10	µA

Analog Characteristics

Unless otherwise specified, AGCIN voltage that gives 0.7 Vp-pd differential output level

Item	Symbol	condition	Min	Typ	Max	Unit
Input level	RFIL1	Internal LNA enabled	-85		-10	dBm
	RFIL2	Internal LNA bypassed	-75		0	dBm
IQ output level	VIQ1	Differential output *1			1.5	Vp-pd
	VIQ2	Single-end output *1			1	Vp-p
IQ phase error	EPH	When RF input level is -40 dBm	-3.0	0	+3.0	deg
IQ Amplitude error	EAMP	When RF input level is -40 dBm	-1.0	0	+1.0	dB
Noise Figure	NF1	Internal LNA enabled		5	8	dB
	NF2	Internal LNA bypassed		8	12	dB
RF input VSWR	VSWR1	Internal LNA enabled		2	2.5	
	VSWR2	Internal LNA bypassed		3	4.5	
VCO phase noise	PN1	When RF input level is -40 dBm f_{RF} = 2150 MHz 100 kHz offset		-89	-85	dBc/Hz
	PN2	10 kHz offset		-86	-83	dBc/Hz
	PN3	1 kHz offset		-83	-80	dBc/Hz
IIP3	IIP3L	Internal LNA enabled When desired signal input level is -20 dBm. Calculated from IM3 measurement result by 2 signals, f_{LO} + 5 MHz, f_{LO} + 7 MHz		9		dBm
	IIP3R	Internal LNA bypassed Same measurement condition as IIP3L		12		dBm
IIP2	IIP2L	Internal LNA enabled Calculates from IM2 by interference signal of 1040 MHz -20 dBm and 1100 MHz -20 dBm when setting desired signal f_{RF} = 2140 MHz -20 dBm		14		dBm
	IIP2R	Internal LNA bypassed Same measurement condition as IIP2L		30		dBm
RF Local Leak	LOL	Local OSC leak to RFIN	-	-	-65	dBm
PLL Reference Leak	REFL	When f_{REF} = 1 MHz	-	-65	-50	dBc
LPF attenuation 1	LPFC1	Attenuation at LPF setting value (f_c)	8	5	1	dB
LPF attenuation 2	LPFC2	Attenuation at twice frequency of LPF setting.	20	30	40	dB

Item	Symbol	condition	Min	Typ	Max	Unit
REF OUT Level	ROL	1 kΩ loaded	0.3	0.6	0.8	Vp-p
REFOUT maximum load	ROD	1 kΩ loaded			20	pF
XTI pin input level	VIXI1	When using as external input (under DV_{DD} = 0 v)	0	-	0.70	Vp-p
	VIXI2	When using as external input (under DV_{DD} = 2.5 V)	0.35	0.65	1.50	Vp-p
External clock jitter	JIT	When using as external input			10	ps
XI pin capacitance	CXI	When using as external input			5	pF

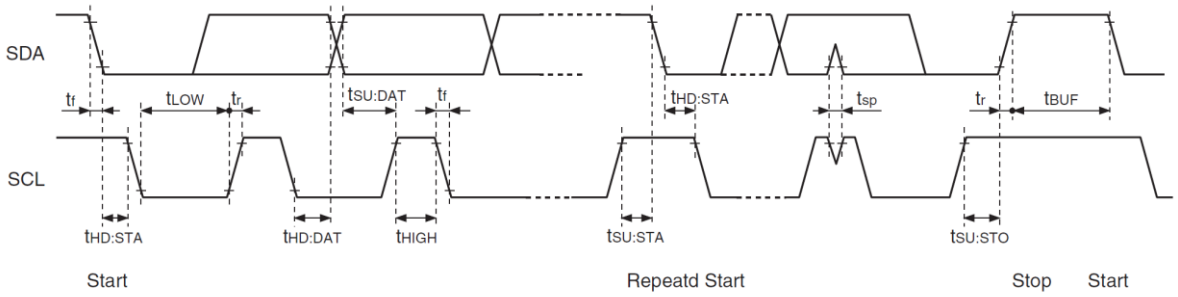
*1 IQ output level is defined with the output level that gives IM3 35 dB or more.

IM3 measurement condition is same as IIP3.

Electrical Characteristics of Logic block

(Circuit voltage = 2.5 V, Ta = 25 ˚C)

Item	Symbol	condition	Min.	Typ.	Max.	Unit
SCL clock frequency	f_{SCL}		0		400	kHz
Start - Hold time	$t_{HD:STA}$		600			ns
Stop - Setup time	$t_{SU:STO}$		600			ns
Bus free time between “STOP” condition and “START” condition	t_{BUF}		1300			ns
Data - Setup time	$t_{SU:DAT}$		100			ns
High hold time	t_{HIGH}		600			ns
Data - Hold time	$t_{HD:DAT}$		0		900	ns
Low hold time	t_{LOW}		1300			ns
Start - Setup time	$t_{SU:STA}$		600			ns
Rise time	tr				300	ns
Fall time	tf				300	ns
Spike pulse width	T_{sp}				50	ns
Capacitive load of bus line	C_b				400	pF
Hardware Reset pulse width	t_{HR}	Input at 24pin (RSTX)	1			ms



$t_{HD:STA}$ = Hold time (repeated) START condition
t_{LOW} = LOW period of the SCL clock
$t_{HD:DAT}$ = Data hold time
$t_{SU:DAT}$ = Data setup time
t_{HIGH} = HIGH period of the SCL clock
$t_{SU:STA}$ = Setup time for a repeated START condition
t_{BUF} = Bus free time between a STOP and START condition
$t_{SU:STO}$ = Setup time for STOP condition
t_r = Rise time of both SDA and SCL signals
t_f = Fall time of both SDA and SCL signals

* When SCL falls, it means START condition if SDA is "0".

* When SCL rises, it means STOP condition if SDA is "1".

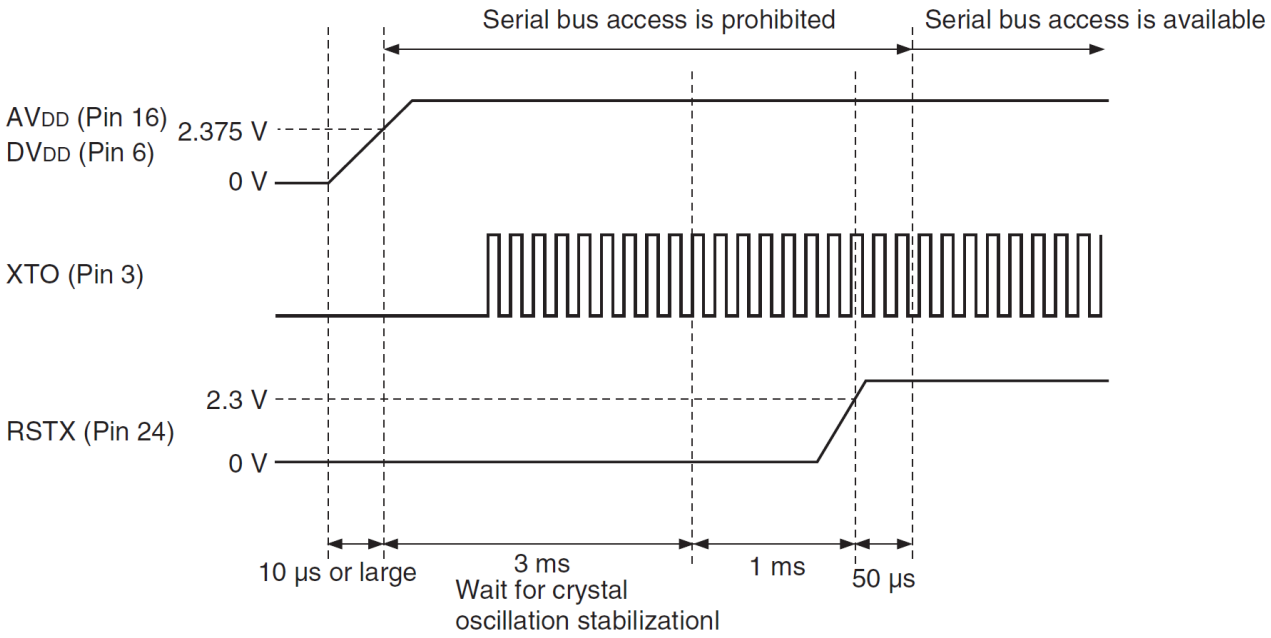
Power-on sequence

The sequence from power-on to hardware reset is below.

Set RSTX low level for more than 1 ms or more after stability time of the crystal oscillation.

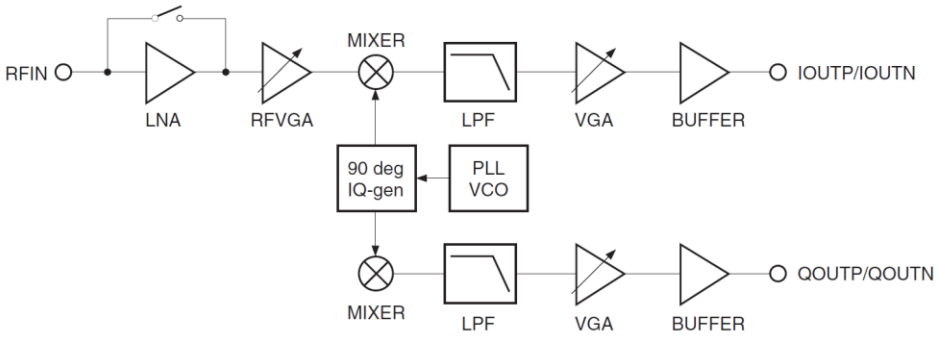
It is no problem which AV_{DD} (Pin 16) or DV_{DD} (Pin 6) start up first.

The communication of 2way serial bus is available after 50 µs after canceling hardware reset.



Description of Operation

Analog part



The signal input to RFIN is converted to baseband I-Q signals by I-Q local signal which is generated by PLL circuit and output through buffer amplifier.

LNA : Single input internal LNA which input impedance is about 75 Ω.

RFVGA : In this block, RF gain control is performed.

This block has BPF characteristics to improve immunity to out-band interferer. Center frequency and gain of BPF should be optimized by register F_CTL/G_CTL based on tuning frequency.

The following settings are recommended.

$f_{RF} < 975$	F_CTL = 11100	G_CTL = 001
$975 \leq f_{RF} < 1050$	F_CTL = 11000	G_CTL = 010
$1050 \leq f_{RF} < 1150$	F_CTL = 10100	G_CTL = 010
$1150 \leq f_{RF} < 1250$	F_CTL = 10000	G_CTL = 011
$1250 \leq f_{RF} < 1350$	F_CTL = 01100	G_CTL = 100
$1350 \leq f_{RF} < 1450$	F_CTL = 01010	G_CTL = 100
$1450 \leq f_{RF} < 1600$	F_CTL = 00111	G_CTL = 101
$1600 \leq f_{RF} < 1800$	F_CTL = 00100	G_CTL = 110
$1800 \leq f_{RF} < 2000$	F_CTL = 00010	G_CTL = 110
$2000 \leq f_{RF}$	F_CTL = 00000	G_CTL = 111

LPF: The LPF incorporates a 5th order low pass filter. It includes DC feedback circuit which reject DC offset.

This DC feedback circuit requires no external capacitor, as it includes capacitor inside IC.

VGA: Base band gain control amplifier. It includes DC feedback circuit which reject DC offset.

This DC feedback circuit requires no external capacitor, as it includes capacitor inside IC.

Buffer: Differential output buffer for the baseband signal. It can be used as a single output IC by termination one side of the differential outputs by the recommended resistor and capacitor.

Serial Bus Interface part

The internal registers of this IC are set via the 2-wire serial bus.

Registers that can be set via the bus have an 8-bit sub address, and this IC uses the sub addresses 00h to 7Fh. (See page 19 and onward for a detailed description of the registers.)

Continuous write and read are possible to registers with continuous sub addresses.

There is no limit to the number of words that can be continuously written or continuously read.

Write to read-only registers is ignored.

This serial bus can be set regardless of reference clock operation. In addition, the operation speed is also independent of the clock frequency.

Slave Address Selection

Four different slave addresses can be selected by the voltage applied to the ADSL pin to support mounting of multiple tuner ICs.

WRITE mode that sets various data and READ mode that transmits the IC internal register data to the host side are switched by setting the LSB (R/W bit) of the address byte.

Slave addresses

1	1	0	0	0	MA1	MA0	R/W

MA1, MA0 : Portion that changes according to the ADSL pin voltage

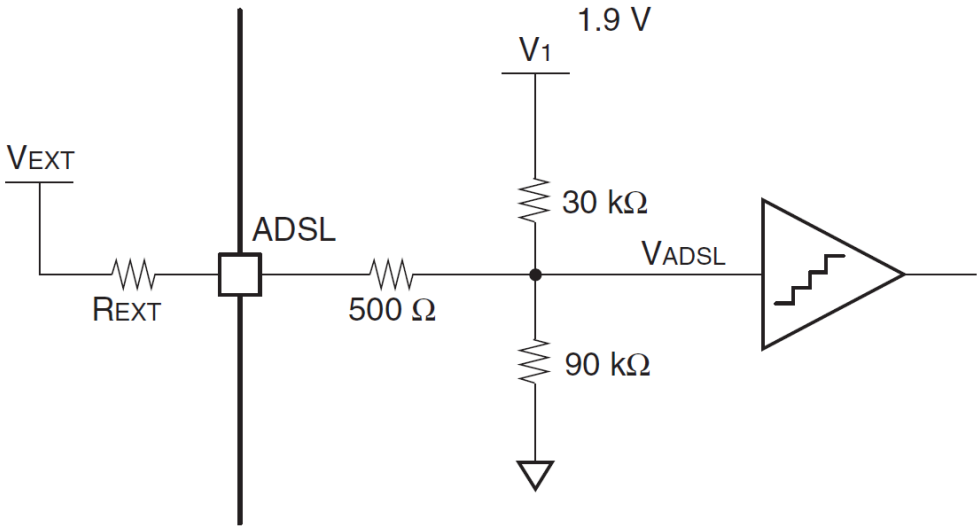
R/W : WRITE mode and READ mode switching

R/W = "0" WRITE mode

R/W = "1" READ mode

ADSL pin voltage	MA1	MA0
0 to 0.19 V	0	0
0.4 to 0.6 V	0	1
0.8 to 1.1 V	1	0
Open	inhibit	
1.71 to 2.2 V	1	1

ADSL Pin voltage is generated by the connection of resistor below.



Slave Address	ADSL Pin voltage (V)	Connection of resistor	recommended Value of R_{EXT} (Ω)
C0	0 to 0.19	Connect to GND	0
C2	0.4 to 0.6	Connect to GND via R_{EXT}	10 k
C4	0.8 to 1.1	Connect to GND via R_{EXT}	47 k
C6	1.71 to 2.2	Connect to PLLREG	0
	1.71 to 2.2	Connect to V_{DD} via R_{EXT} (in case of V_{DD}=2.5 V)	22 k or 33 k
	1.71 to 2.2	Connect to V_{DD} via R_{EXT} (in case of V_{DD}=3.3 V)	47 k, or 68 k

Writing and reading procedure

Writing register is performed as follows.

Write slave address -> Write desired sub address -> Write register setting value

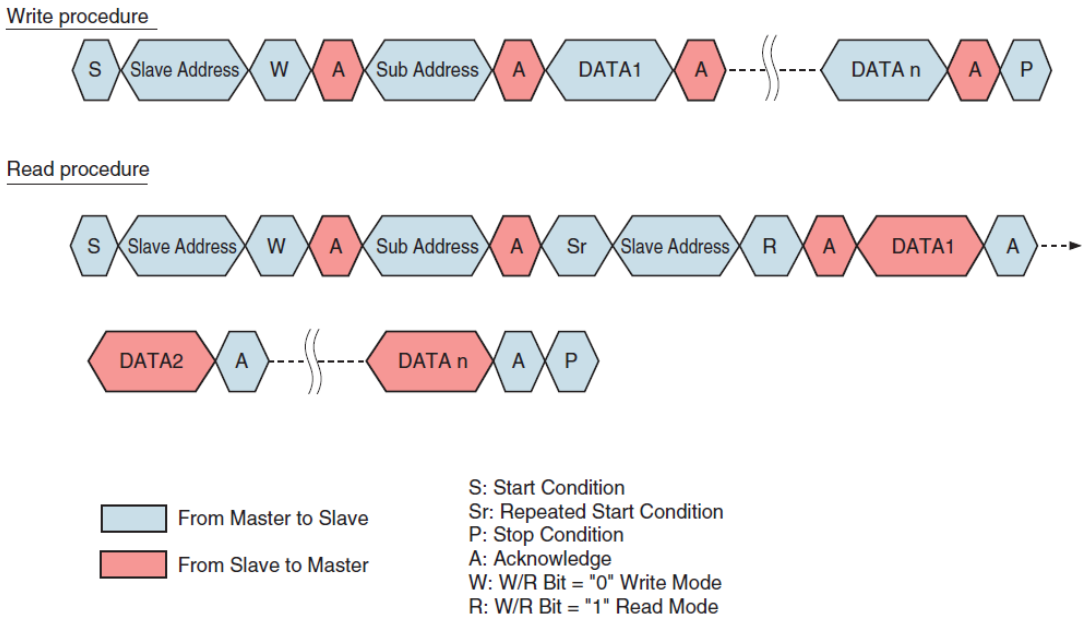
This procedure is also applied to continuous write mode that performs continuous write to consecutive sub addresses.

Reading register is performed in 1-byte units as follows.

Write slave address -> Write desired sub address -> Repeated start condition -> Write slave address -> Data read

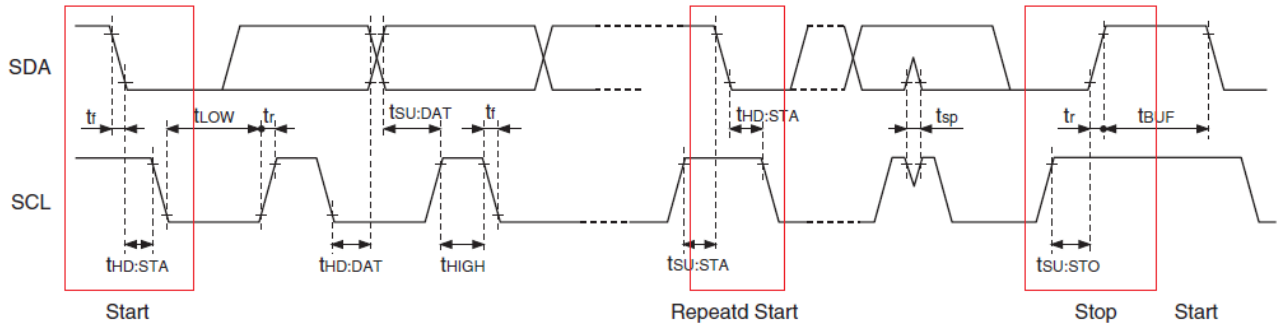
Repeated start condition can be substituted by "Stop condition -> Start condition".

This procedure is also applied to continuous read mode that performs continuous read form consecutive sub address.



Description of SCL and SDA Signal during Bus Communication

Start/Stop/Repeated start conditions signals are as shown in the figure below see the specifications for the detail timing.



Detailed Description of Registers

The data noted for each register are the initial values for this IC.

Sub address	Register name	Bit	RW	Bit position 7	6	5	4	3	2	1	0	Description
00	P_COUNT_H[7:0]	8	RW	0	0	0	0	1	0	0	0	PLL main counter frequency division ratio setting P_COUNT = {P_COUNT_H[7:0], P_COUNT_L [3:0]} The settings to the internal counters are executed when they are written to sub address 03h. * Initial value: 12'd137
01	P_COUNT_L[3:0]	4	RW	1	0	0	1					
	S_COUNT[2:0]	3	RW					1	0	0		PLL swallow counter frequency division ratio setting * Initial value: 3'd4
	RESERVE	1	RW								0	RESERVE
02	K_COUNT_H[7:0]	8	RW	0	0	0	0	0	0	0	0	Test register. Always set to 00h The values of sub Address 00 to 01 (P_COUNT/S_COUNT) are set when 00h is written to sub address 03h. So write 00h to 03h continuously when set reception frequency.
03	K_COUNT_L[7:0]	8	RW	0	0	0	0	0	0	0	0	
04	MDIV_SW	1	RW	0								When MDIV_SW is enabled, the frequency division ratio between the VCO and the MIXER changes from 1/2 to 1/4. 0:Thru. (1155 MHz ≤ f_{RF}) 1: 1/2 (950 MHz ≤ f_{RF} < 1155 MHz)
	RESERVE[6:0]	7	RW		0	0	0	0	0	0	0	RESERVE
05	CALIB_START	1	RW	0								Calibration start bit. When "1" is set, the CALIB sequence starts and the optimum VCO selection, LPF cut off frequency and CP current setting value are calculated. Always execute calibration when changing the tuning data. 1: Calibration start; this bit automatically returns to "0" after calibration ends.
	RESERVE[6:0]	7	RW		0	0	0	0	0	0	0	RESERVE
06	REF_R[7:0]	8	RW	0	0	0	1	1	0	1	1	PLL comparison frequency setting register. *Initial value: 8'd27
07	FIN[7:0]	8	RW	0	0	0	1	1	0	1	1	Reference clock frequency (crystal oscillation frequency) setting register This is used as the frequency division ratio for the system clock (1 MHz) required by the logic block. *Initial value: 8'd27
08	LT_EN	1	RW	1								Test register Please set 0.
	RESERVE[6:0]	7	RW		0	0	0	0	0	0	0	RESERVE
09	G_CTL[2:0]	3	RW	0	0	0						RFVGA gain control This must be set according to the reception frequency. Max. gain 000 Min. gain 111
	F_CTL[4:0]	5	RW				0	0	0	0	0	RFVGA peak frequency control This must be set according to the reception frequency. (See page 13) 0000: high freq., 11111: low freq

Sub address	Register name	Bit	RW	Bit position								Description
				7	6	5	4	3	2	1	0	
0A	OUT_LEVEL[1:0]	2	RW	0	0							IQ output gain and output type selection. In case of using single end output, set 2'b01 or 2'b11. 00: Default (Differential output) 01: Single end output (+ 4.4 dB) 10: Reserve 11: Single end output (-2.4 dB)
	HP_MODE	1	RW			0						Pass bandwidth control of DC feedback 0: normal 1: Low
	GAIN_STEP[1:0]	2	RW				0	0				Test register
	RESERVE[2:0]	3	RW						0	0	0	RESERVE
0B	RESERVE[7:0]	8	RW	0	0	0	0	0	0	0	0	RESERVE
0C	RESERVE[7:0]	8	RW	0	0	0	0	0	0	0	0	RESERVE
0D	PORT	1	RW	0								RESERVE
	RESERVE[6:0]	7	RW		0	0	0	0	0	0	0	RESERVE
0E	REFOUTEN	1	RW	1								REFOUT circuit enable * 1: Enable 0: Disable
	XOSC_SEL[4:0]	5	RW		1	1	1	1	1			Crystal oscillator drive current setting register, 1 LSB = 25 μA (Max: 775 μA). The crystal oscillator is stopped and external clock input is available by setting 5'b0_0000. * Initial value: 5'b1_1111 (775 μA)
	RESERVE[1:0]	2	RW							0	0	RESERVE
0F	RESERVE[7:0]	8	RW	0	0	0	0	0	0	0	0	RESERVE
10	RESERVE[7:0]	8	RW	0	0	0	0	0	0	0	0	RESERVE
11	PS_EN	1	RW	0								Power save setting 0: Reception (Normal status) 1: Powe saving
	PS_XOSC_EN	1	RW		0							Crystal oscillator operating setting when PS_EN = H 0: Stop crystal oscillation 1: Continuos oscillation
	RESERVE[5:0]	6	RW			0	0	0	0	0	0	RESERVE
12	LNASW	1	RW	0								Internal LNA setting 0: Internal LNA ON 1: LNA bypassed
	LNA_IADJ	1	RW		0							Test register
	IT_MODE	1	RW			1						Test register
	RFREG_VADJ[1:0]	2	RW				0	0				Test register
	LNA_EN	1	RW						1			Enabler of LNA circuit 0: LNA Disable 1: LNA Enable
	RFVGA_EN	1	RW							1		Enabler of RFVGA circuit. 0: RFVGA Disable 1: RFVGA Enable
	RFREG_EN	1	RW								1	Enabler of regulator for RF circuits. 0: RFREG Disable 1: RFREG Enable
13	RESERVE[7:0]	8	RW	0	0	0	0	0	0	0	0	RESERVE
14	RESERVE[7:0]	8	RW	0	0	0	0	0	0	0	0	RESERVE

Sub address	Register name	Bit	RW	Bit position								Description
				7	6	5	4	3	2	1	0	
15	BBTEST_EN[1:0]	2	RW	0	0							Test register
	MIX_EN	1	RW			1						Enabler of Mixer circuits. 0: Mixer Disable 1: Mixer Enable
	RESERVE[4:0]	5	RW				0	0	0	0	0	RESERVE
16	OUT_EN_MODE	1	RW	0								Output mute setting during LPF calibration 0: Mute after power up only 1: Mute while every calibration sequence.
	BB_EN	1	RW		1							Enabler of Base band circuits 0: Disable 1: Enable
	RESERVE[5:0]	6	RW			0	0	0	0	0	0	RESERVE
17	RESERVE[7:0]	8	RW	0	0	0	0	0	0	0	0	RESERVE
18	RESERVE[7:0]	8	RW	0	0	0	0	0	0	0	0	RESERVE
19	RESERVE[7:0]	8	RW	0	0	0	0	0	0	0	0	RESERVE
1A	RESERVE[7:0]	8	RW	0	0	0	0	0	0	0	0	RESERVE
1B	FRAC_MODE	1	RW	0								Test register
	ORDER	1	RW		1							Test register
	ACC_RST	1	RW			0						Test register
	DITHER_EN	1	RW				1					Test register
	RESERVE[3:0]	4	RW					0	0	0	0	RESERVE
1C	CP_I_CAL_EN	1	RW	1								Test register
	VCO_CAL_EN	1	RW		1							Test register
	RESERVE[5:0]	6	RW			0	0	0	0	0	0	RESERVE
1D	RESERVE[7:0]	8	RW	0	0	0	0	0	0	0	0	RESERVE
1E	RESERVE[7:0]	8	RW	0	0	0	0	0	0	0	0	RESERVE
1F	PFD_EN	1	RW	1								Test register
	PFD_TUP	1	RW		0							Test register
1F	PFD_TDN	1	RW			0						Test register
	PFD_MODE[1:0]	2	RW				0	0				Test register
	RESERVE[2:0]	3	RW						0	0	0	RESERVE
20	ODBUF_EN[1:0]	2	RW	0	0							Test register
	MONI_EN	1	RW			0						Test register
	CLK_SRC_DIV_EN	1	RW				1					Test register
	DSM_CLK_EN	1	RW					1				Test register
	DSM_CLK_REF_SEL	1	RW						1			Test register
	RESERVE[1:0]	2	RW							0	0	RESERVE
21	RESERVE[7:0]	8	RW	0	0	0	0	0	0	0	0	RESERVE
22	RESERVE[7:0]	8	RW	0	0	0	0	0	0	0	0	RESERVE

Sub address	Register name	Bit	RW	Bit position								Description
				7	6	5	4	3	2	1	0	
23	REFOUT_BUF_CURR	2	RW	0	0							Driving current setting of REFOUT 11: 1.25 mA 10: 750 μA 01: 500 μA *00 : 1 mA
	REFOUT_AMP_ZL	2	RW			0	0					Load register setting of REFOUT 11: 1.12 kΩ 10: 1.25 kΩ 01: 1.75 kΩ * 00:1.5 kΩ
	REFOUT_AMP_CURR	2	RW					0	0			Current setting for REFOUT amplifier circuit 11: 900 μA 10: 700 μA 01: 300 μA 00: 500 μA
	RESERVE[1:0]	2	RW							0	0	RESERVE
24	DIV_RST	1	RW	0								Test register
	CP_EN	1	RW		1							Test register
	RESERVE[5:0]	6	RW			0	0	0	0	0	0	RESERVE
25	CP_I_H[7:0]	8	RW	0	0	1	1	1	1	0	0	Test register
26	CP_I_L[1:0]	2	RW	0	0							
	RESERVE[5:0]	6	RW			0	0	0	0	0	0	RESERVE
27	IREF_EN	1	RW	1								PLL block and crystal oscillator circuit reference current source enable. The crystal oscillator circuit is stopped by setting this to disable. * 1: Enable 0: Disable
	CPDA_OUT_EN	1	RW		0							Test register
	CP_AMP_EN	1	RW			1						Test register
	R2_BANK[1:0]	2	RW				0	0				Test register
	C2_BANK[1:0]	2	RW						0	0		Test register
	RESERVE	1	RW								0	RESERVE
28	VCO_M_EN	1	RW	0								Test register
	VCO_L_EN	1	RW		1							Test register
	VCO_CSW[4:0]	5	RW			1	1	1	1	1		Test register
	RESERVE	1	RW								0	RESERVE
29	VCO_RSW[3:0]	4	RW	0	1	1	1					Test register Set to initial value
	R2_RANGE	1	RW					0				Test register
	DIV_BIAS[1:0]	2	RW						0	0		Test register
	MDIV_EN	1	RW								1	Enabler of circuit between VCO and MIXER * 1: Enable 0: Disable

Sub address	Register name	Bit	RW	Bit position								Description
				7	6	5	4	3	2	1	0	
2A	VCO_BUF_M_EN	1	RW	0								Test register
	VCO_BUF_L_EN	1	RW		1							Test register
	VCOBUF_EN	1	RW			1						Test register
	DMPS_EN	1	RW				1					Enabler of Dual-Modulus divide * 1: Enable 0: Disable
	CML2CMOS_EN	1	RW					1				Enabler of buffer circuit of PLL circuit. * 1: Enable 0: Disable
	VCO_FC_CLK_EN	1	RW						0			Test register
	IQGEN_EN	1	RW							1		Enabler of IQ Generator * 1: Enable 0: Disable
	RESERVE	1	RW								1	RESERVE
2B	RESERVE[7:0]	8	RW	0	0	0	0	0	0	0	0	RESERVE
2C	RESERVE[7:0]	8	RW	0	0	0	0	0	0	0	0	RESERVE
2D	GPIO[1:0]	2	RW	0	0							GPIO output setting 2'b00: GPIO OFF 2'b01: GPIO ON
	MONI_SEL[3:0]	4	RW			0	0	0	0			Test register * Initial value: 4'd0
	RESERVE[1:0]	2	RW							0	0	RESERVE
2E	RESERVE[7:0]	8	RW	0	0	0	0	0	0	0	0	RESERVE
2F	RESERVE[7:0]	8	RW	0	0	0	0	0	0	0	0	RESERVE
30	RST_L_DTCT	1	RW	0								Test register
	LCK_DTCT_CYCLE[1:0]	2	RW		0	0						Test register
	UNLCK_DTCT_CYCLE[1:0]	2	RW				0	0				Test register
	RESERVE[2:0]	3	RW						0	0	0	RESERVE
31	FREQCTR_START	1	RW	0								Test register
	FC_CLK_DIV_TEST[1:0]	2	RW		0	0						Test register
	RESERVE[4:0]	5	RW				0	0	0	0	0	RESERVE
32	FVCO_H[7:0]	8	RW	0	1	0	0	0	1	0	0	Test register
33	FVCO_L[4:0]	5	RW	1	1	0	0	0				
	RESERVE[2:0]	3	RW						0	0	0	RESERVE
34	KC0[7:0]	8	RW	0	0	0	0	1	0	1	0	CP current automatic calculation parameter. Normally use the initial value. * Initial value: 8'd10
35	KC1[7:0]	8	RW	0	0	0	1	1	1	1	0	CP current automatic calculation parameter. Normally use the initial value. * Initial value: 8'd30
36	KBW[7:0]	8	RW	0	1	1	1	1	0	0	0	CP current automatic calculation parameter. Normally use the initial value. * Initial value: 8'd120

Sub address	Register name	Bit	RW	Bit position								Description
				7	6	5	4	3	2	1	0	
37	LPF_ADJ_EN	1	RW	1								LPF calibration enabler 0: Calibration disable 1: Normal condition(Using calibration)
	LPFADJ_TG_FREQ[5:0]	6	RW		0	0	0	0	1	1		LPF cutoff frequency setting (MHz) Set in binary. Valid range is d5 to d36 d37 to d62 is forbidden. d63 set the maximum cutoff frequency.
	LPFADJ_MANUAL_EN	1	RW								0	Test register
38	LPFADJ_MANUAL[7:0]	8	RW	0	0	0	0	0	0	0	0	Test register
39	LPF_CTL[7:0]	8	R	0	0	0	0	0	0	0	0	Test register
3A	FREQ_CTR_H[7:0]	8	R	0	0	0	0	0	0	0	0	Test register
3B	FREQ_CTR_L[4:0]	5	R	0	0	0	0	0				
	VCO_CAL_ERR	1	R						0			VCO calibration error flag * 0: — 1: Error
	RESERVE[1:0]	2	RW							0	0	RESERVE
3C	CAL_FVCO_ENX	1	RW	0								Test register
	TEST_SEL[3:0]	4	RW		0	0	0	0				Test register
	RESERVE[2:0]	3	RW						0	0	0	RESERVE
3D	CLK1M_SILENT_EN	1	RW	0								Test register
	VCO_CLK_REF_SEL	1	RW		0							Test register
	RESERVE[5:0]	6	RW			0	0	0	0	0	0	RESERVE
7E	EXTRA1[7:0]	8	RW	0	0	0	0	0	0	0	0	Test register
7F	VER[3:0]	4	R	0	1	1	1					IC version indication
	CHIP_TYPE[3:0]	4	R					0	0	0	1	IC internal chip version indication

Please write the initial value when you need to write the test registers due to burst write.

Tuning Procedure

Main Counter and Swallow Counter Settings

The tuning frequency is obtained by the following formulas.

RF = fosc/4 = 1/2 × fref ×(8P + S) (950 ≤ RF < 1155 MHz) MDIV_SW = 1'b1

RF = fosc/2 = fref × (8P + S) (1155 ≤ RF ≤ 2150 MHz) MDIV_SW = 1'b0

RF : Tuning frequency

fosc : Oscillation frequency of VCO circuit

fref : Reference frequency

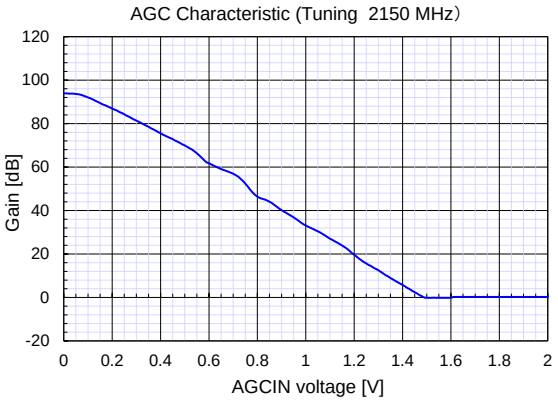
REF_R should be the value which satisfy the equation below

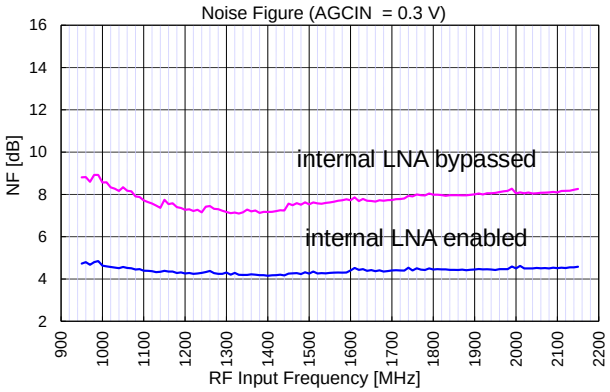
(crystal oscillation frequency) / REF_R = 1 MHz

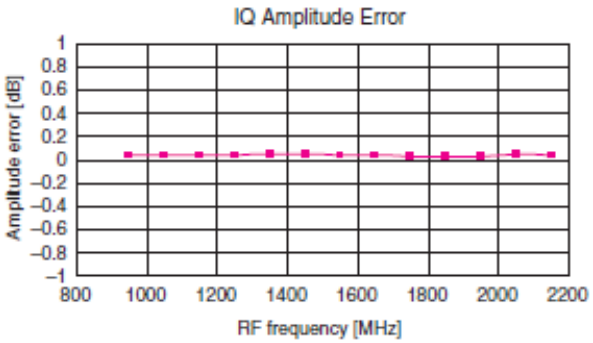
P : Main counter frequency division ratio

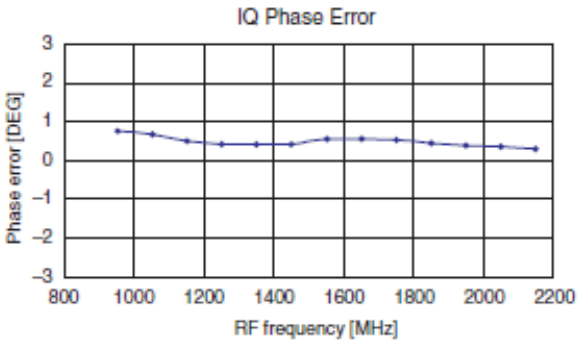
S : Swallow counter frequency division ratio

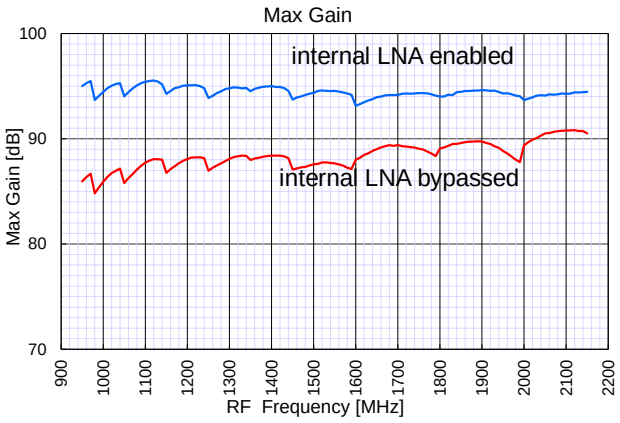
Example of Representative Characteristics

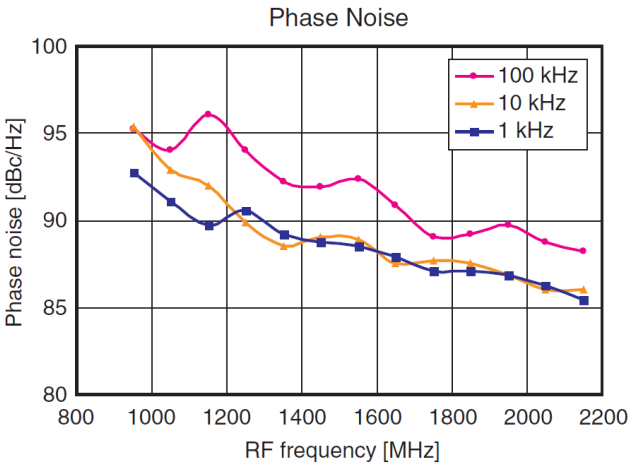


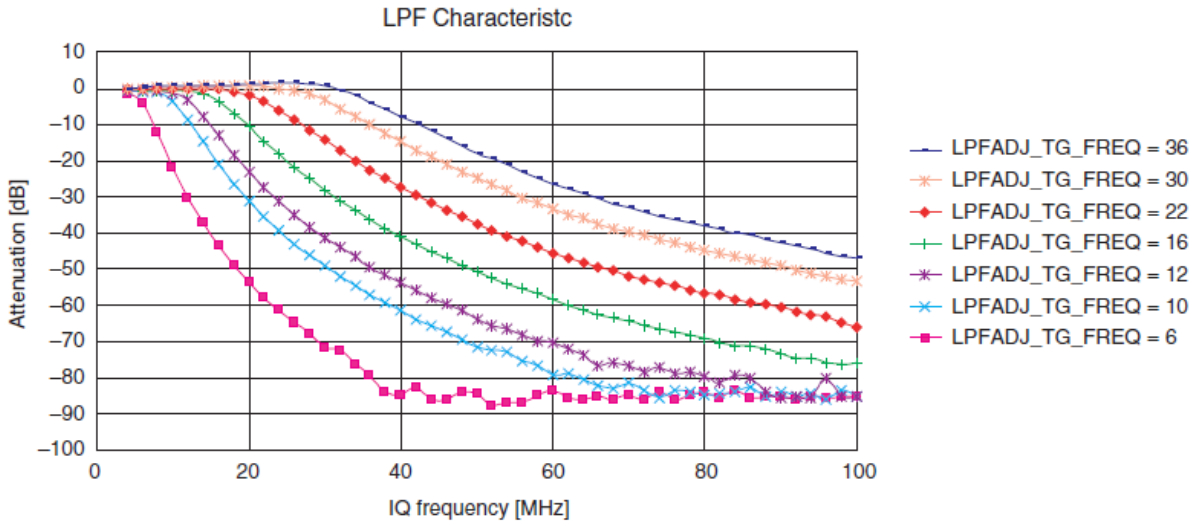


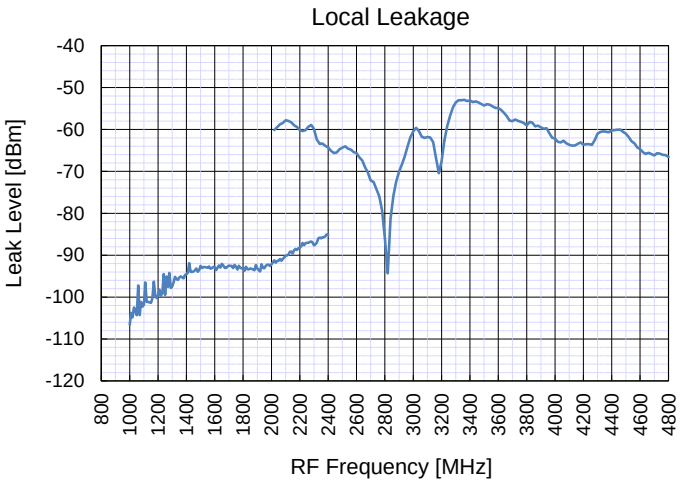


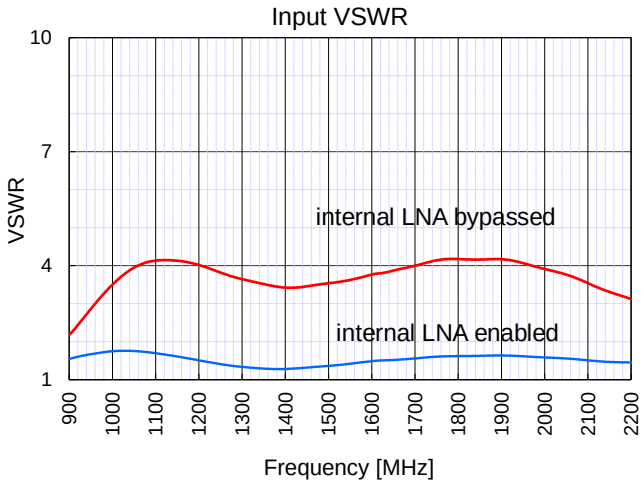






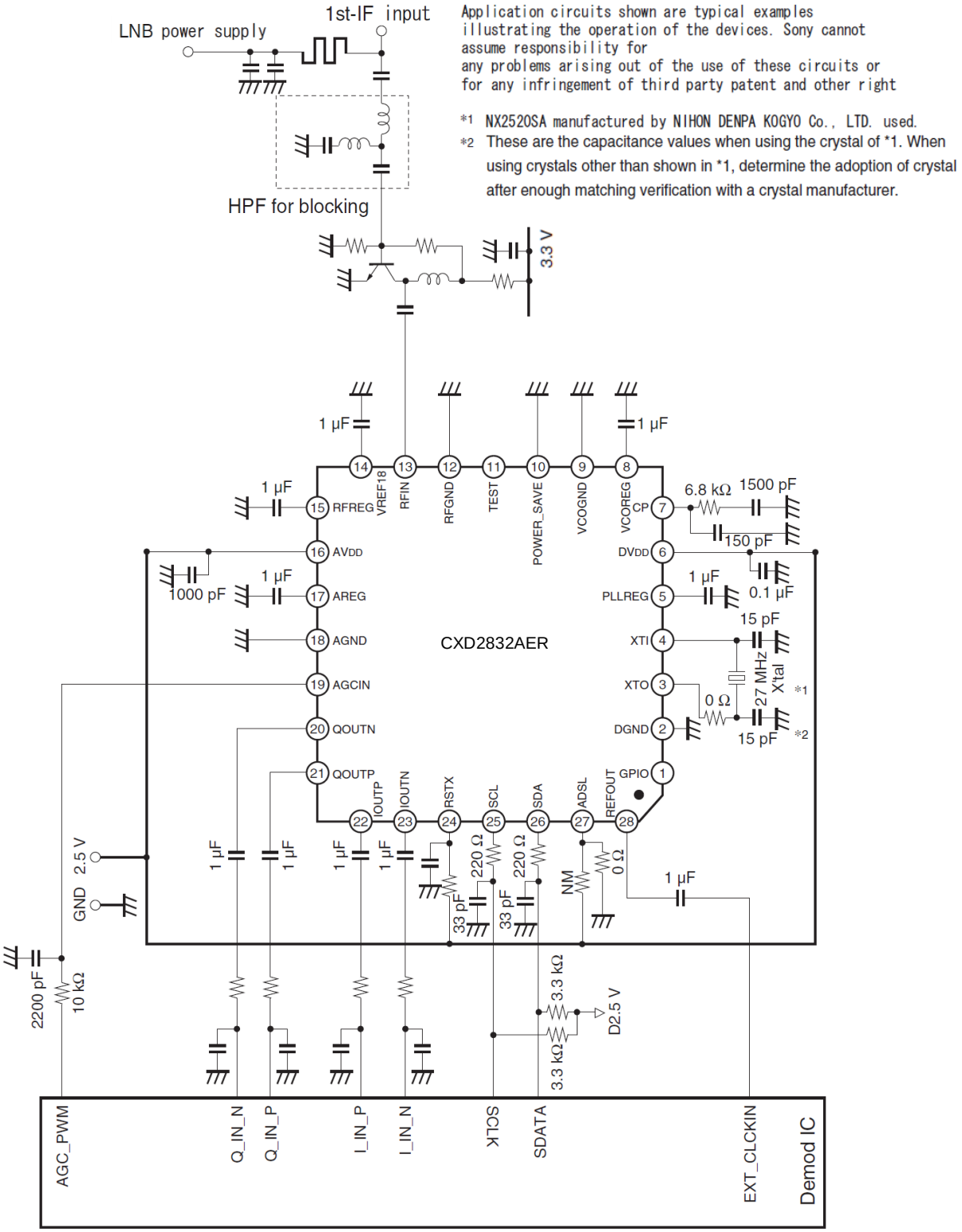

LPF Characteristc
Attenuation [dB]
10
0
−10
−20
−30
−40
−50
−60
−70
−80
−90
−100
0
20
40
60
80
100
IQ frequency [MHz]
LPFADJ_TG_FREQ = 36
LPFADJ_TG_FREQ = 30
LPFADJ_TG_FREQ = 22
LPFADJ_TG_FREQ = 16
LPFADJ_TG_FREQ = 12
LPFADJ_TG_FREQ = 10
LPFADJ_TG_FREQ = 6


Local Leakage
Leak Level [dBm]
-40
-50
-60
-70
-80
-90
-100
-110
-120
800
1000
1200
1400
1600
1800
2000
2200
2400
2600
2800
3000
3200
3400
3600
3800
4000
4200
4400
4600
4800
RF Frequency [MHz]

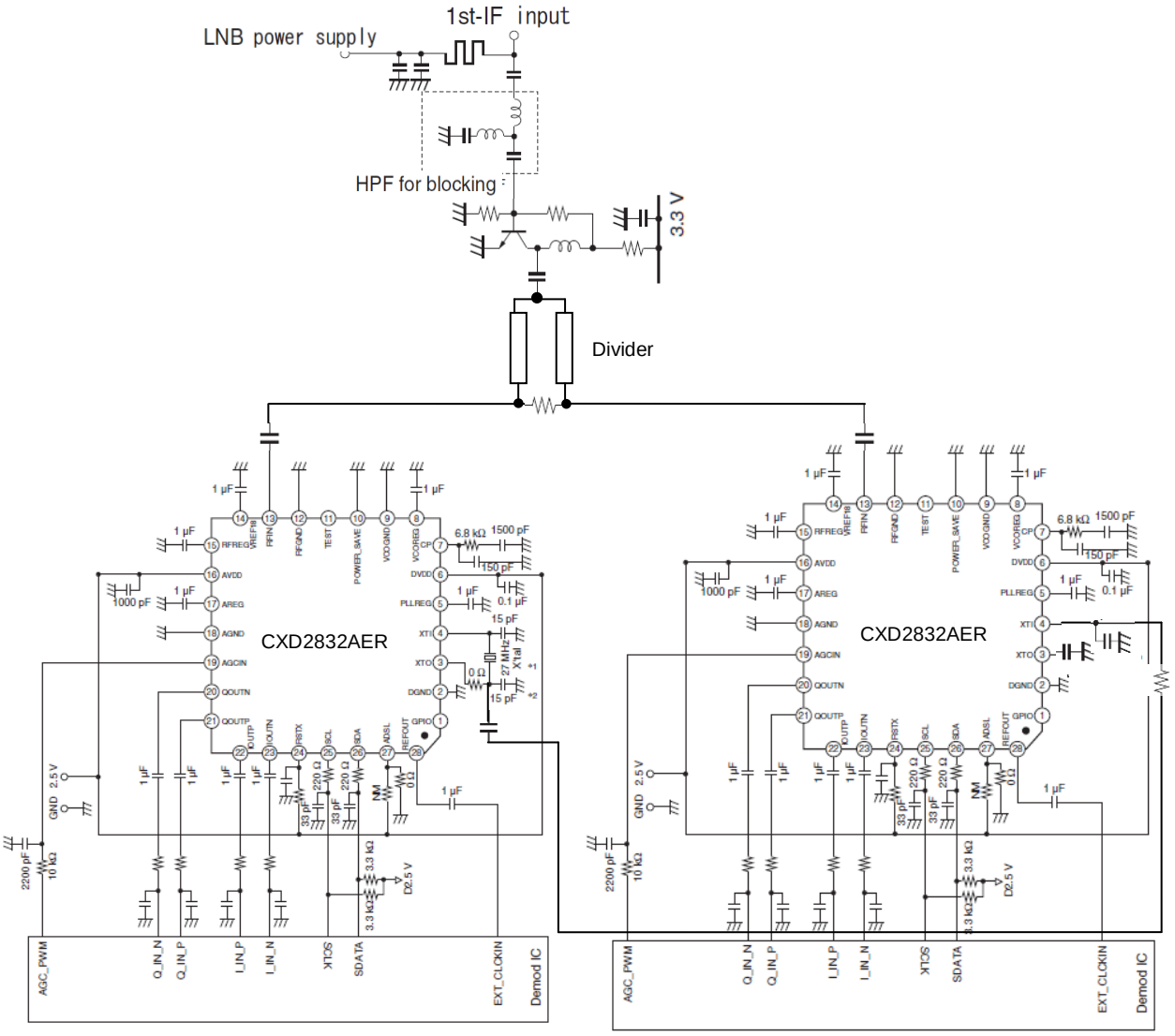

Input VSWR
VSWR
10
7
4
1
internal LNA bypassed
internal LNA enabled
900
1000
1100
1200
1300
1400
1500
1600
1700
1800
1900
2000
2100
2200
Frequency [MHz]

Application Circuit

Application for Single tuner



Application for double tuner

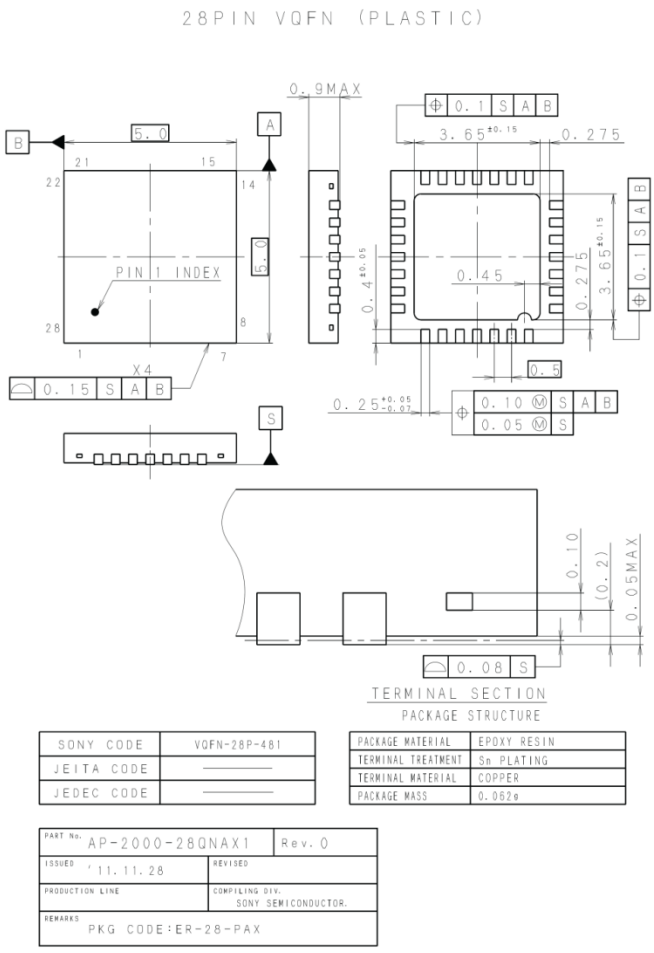


In case of using two or more the CXD2832AER simultaneously, please be careful also of a pattern layout or a shield so that degradation of the receiving performance by interference does not occur.

Please contact our sales member if you plan to use 3 or more the CXD2832AER in connection.

Package outline

(Unit :mm)

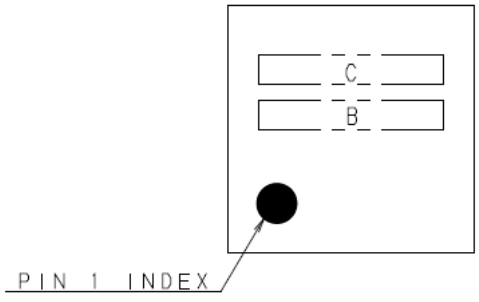


SONY CODE	VQFN-28P-481
JEITA CODE	————
JEDEC CODE	————

PACKAGE MATERIAL	EPOXY RESIN
TERMINAL TREATMENT	Sn PLATING
TERMINAL MATERIAL	COPPER
PACKAGE MASS	0.062g

PART No. AP-2000-28QNAX1	Rev. 0
ISSUED '11.11.28	REVISED
PRODUCTION LINE	COMPILING DIV. SONY SEMICONDUCTOR.
REMARKS PKG CODE:ER-28-PAX	

Marking



MARKING C: D2832A

< INSTRUCTIONS >

1) TYPE NO. (MAX 7 CHARACTERS) IN SECTION C.
(FOR MORE THAN 7 CHARACTERS FOLLOW RULES FOR ABBREVIATIONS.)
2) LOT NO. (MAX 7 CHARACTERS) IN SECTION B.