QUAD COMPARATOR INTERFACE CIRCUIT

- MINIMUM HYSTERESIS VOLTAGE AT EACH INPUT : 0.3 V
- OUTPUT CURRENT : 15 mA
- LARGE SUPPLY VOLTAGE RANGE : + 10 V TO + 35 V
- INTERNAL THERMAL PROTECTION
- INPUT AND OUTPUT CLAMPING PROTECTION DIODES

DESCRIPTION

The ESM1602B is a quadruple comparator intended to provide an interface between signal processing and transmitting lines in very noisy industrial surroundings.

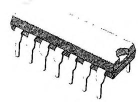
Output of each comparator, used as line driver, is well protected against powerful overvoltages. The output is a common emitter stage including complementary transistors. This arrangement ensures that no simultaneous conduction of high and low stages can occur in the presence of noise signals. Short-circuit currents toward V_{CC} and ground are limited to the same value.

The ESM1602B can operate as receiver on a line transmitting noisy high-voltage signals. It has the same input stage as ESM1600B. Hysteresis effect, internally implemented on inputs of each comparator provides an excellent noise immunity. In addition each input is also protected against overvoltages.

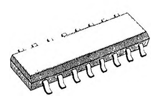
The ESM1602B can operate in a wide supply voltage range (standard operational amplifier ± 15 V supply or single + 12 V or + 24 V supplies used in industrial electronic sets).

Moreover, internal thermal protection circuitry cuts out the output current of the four comparators when power dissipation becomes excessive.

DIP-14/2
(Plastic)



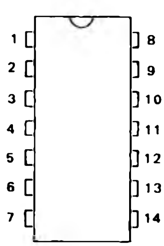
SO-16J



ORDER CODES : ESM1602B (DIP-14)
ESM1602BFP (SO-16J)

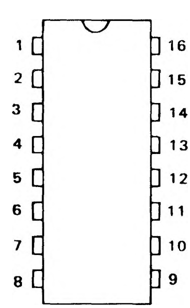
PIN CONNECTION (top view)

DIP-14



1 - Inverting input 1
2 - Non-inverting input 1
3 - Output 1
4 - Non-inverting input 2
5 - Inverting input 2
6 - Output 2
7 - GND
8 - Output 3
9 - Inverting input 3
10 - Non-inverting input 3
11 - Output 4
12 - Non-inverting input 4
13 - Inverting input 4
14 - V_{CC}

SO-16J

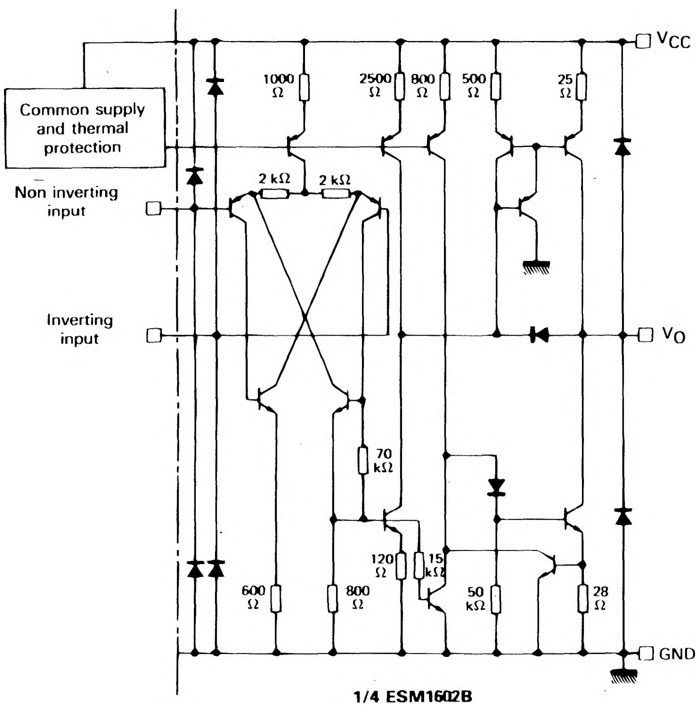


1 - Inverting input 1
2 - Non-inverting input 1
3 - Output 1
4 - Non-inverting input 2
5 - Inverting input 2
6 - Output 2
7 - GND
8 - N.C.
9 - N.C.
10 - Output 3
11 - Inverting input 3
12 - Non-inverting input 3
13 - Output 4
14 - Non inverting input 4
15 - inverting input 4
16 - V_{CC}

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	45	V
V_{ID}	Differential Input Voltage	45	V
V_I	Input Voltage	– 0.7 to + 45	V
$I_{O(max)}$	Output Current	Internally Limited	mA
P_{tot}	Power Dissipation	Internally Limited	W
T_{op}	Operating Ambient Temperature Range	– 25 to + 85	°C
T_{stg}	Storage Temperature Range	– 40 to + 150	°C

SCHEMATIC DIAGRAM

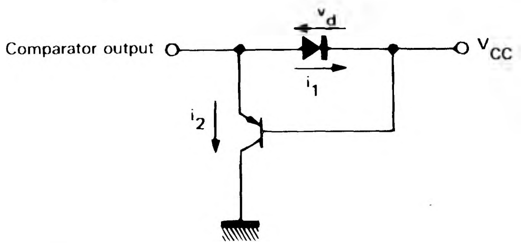


1/4 ESM1602B

ELECTRICAL CHARACTERISTICS V_{CC} = + 35 V, – 25 °C ≤ T_{amb} ≤ + 85 °C
(unless otherwise specified)

Symbol	Parameter	Value			Unit	Fig.
		Min.	Typ.	Max.		
V_I^+ V_I^-	Input Voltage Range - Note 1 Non-inverting Input Inverting Input	 0 2	 – –	 33 33	V	–
V_C	Input Control Voltage (2 V < V_{CM} < 33 V) - Note 2	150	–	500	mV	8
I_{IB}	Input Bias Current - Note 3	–	1	5	μA	–
I_{SC}	Short-circuit Output Current V_{CC} = + 10 to + 35 V	 6	 –	 25	mA	 9
V_{CC}-V_O	Output Saturation Voltage (high level) - (I_O = – 10 mA)	–	1	1.5	V	11
V_O	Output Saturation Voltage (low level) - (I_O = + 10 mA)	–	1	1.6	V	12
I_{CC}	Supply Current R_L = ∞ for the 4 Comparators R_L Common for the Comparators	 – –	 4 10	 6 13	mA	 13,14
S_{VO}	Output Slew-rate (R_L = 3 KΩ, T_{amb} = + 25 °C)	1	–	–	V/μs	–
V_F	Input Protective Diode Forward Voltage (I = 20 mA, T_{amb} = + 25 °C)	–	–	1.5	V	–
–	Energy of Pulses against which Circuit Output is Protected (T_{amb} = + 25 °C) - Note 4	 –	 –	 20	mJ	–
–	Pulsed Current Applied to Protective Output Diodes (T_{amb} = + 25 °C) - Note 5	 –	– 0.4	 –	A	15

Notes :
1. When negative input is biased between 0 and 2 volts output is always low.
2. Comparator hysteresis voltage on positive input on the one hand and negative input on the other hand equals sum of input control voltages V_{C1} + V_{C2} or V_{C3} + V_{C4}.
3. Input current flows out of the circuit owing to PNP input stage. This current is constant and independent of output level. So no load change is transmitted to inputs.
4. By definition, a circuit is immunized against powerful signals when no durable characteristic change occurs after the application of these signals and when the circuit has not been destroyed.
   In industrial surroundings, parasitic signals contain usually high voltage (over 200 V) AC harmonics having variable impedance of 500 Ω to 10 KΩ.
   The power dissipation of these signals is divided between clamping diodes and the V_{CC}. Simulation is used to determine the maximum energy level. The injected current value cannot in any case exceed 3 A.
5. Output protective diodes are individually by means of positive and negative discharge voltages of a capacitor. The negative discharge control occurs through a single diode. During positive discharge, due to the properties of integration, a grounded collector PNP transistor appears in parallel with the clamping diode connected to V_{CC}. A part of the current flows through this transistor, V_{CE} being greater than V_{CC}. If T is the total discharge duration, energy dissipated in the circuit is :



$$W = \int_{0}^{T} [\, i_1 \cdot v_d + i_2 (V_{CC} + v_d) \,]\, dt$$

For a certain injected current, the lower the current I_2, that is to say the lower the PNP current gain the smaller the energy is dissipated in the circuit. Topology and technological processes have been chosen to shorten this current gain.

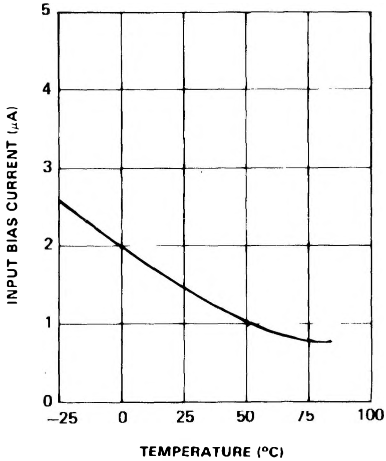


Fig. 1 – INPUT BIAS CURRENT.

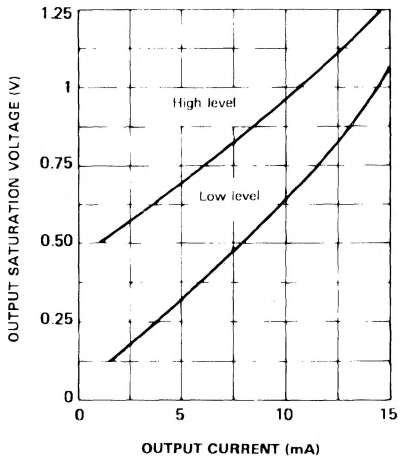


Fig. 2 – OUTPUT SATURATION VOLTAGE.

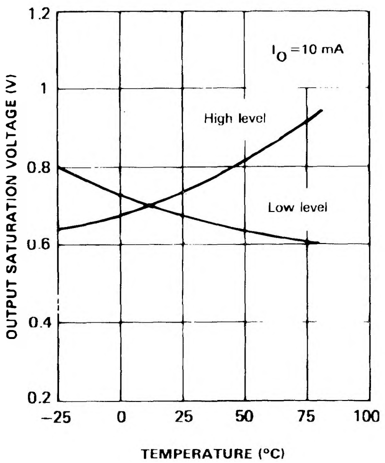


Fig. 3 – OUTPUT SATURATION VOLTAGE.

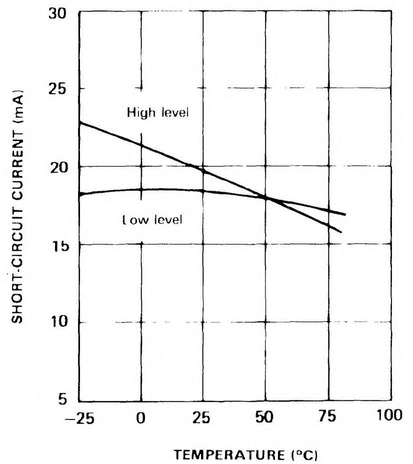


Fig. 4 – SHORT CIRCUIT CURRENT.

TYPICAL APPLICATIONS

Figure 5 : Conversion of DTL, TTL, MOS Signals on a Transmitting Line.

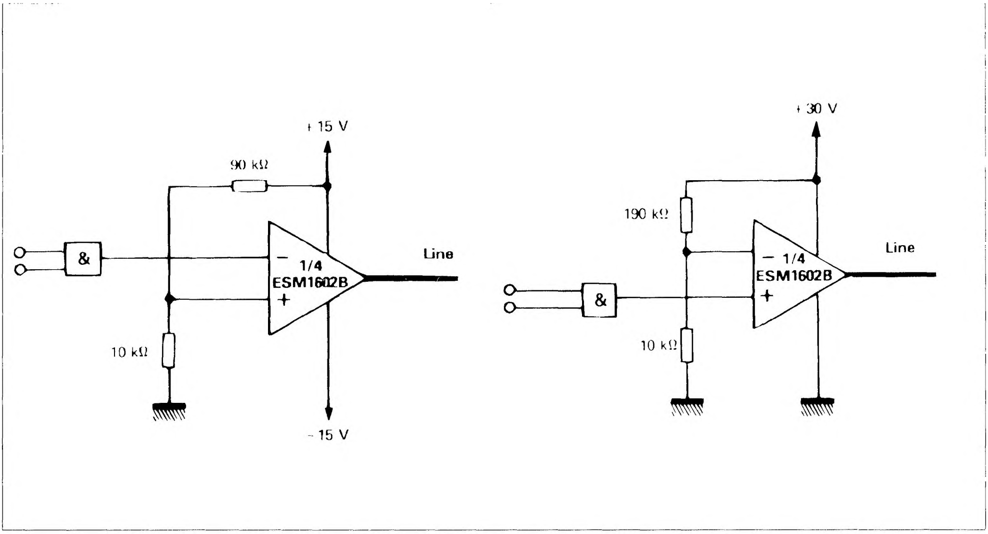


Figure 6 : Reception of Highly Noisy Signals.

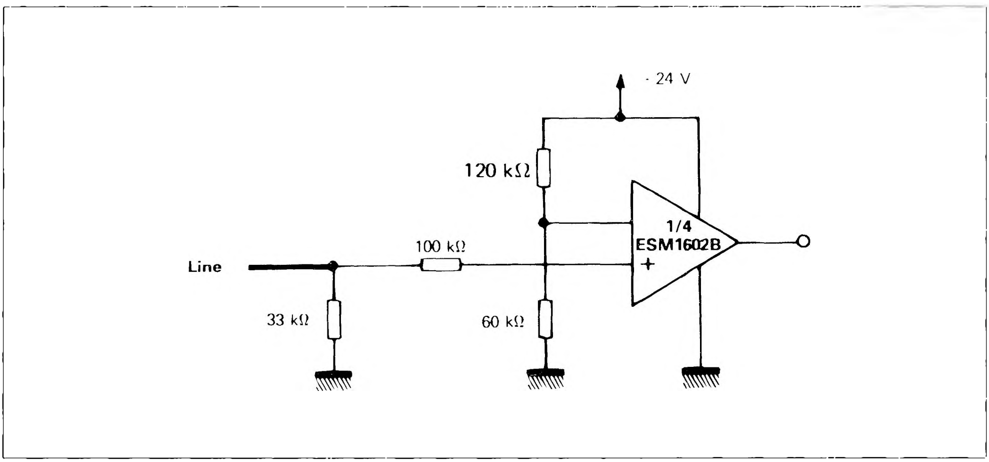
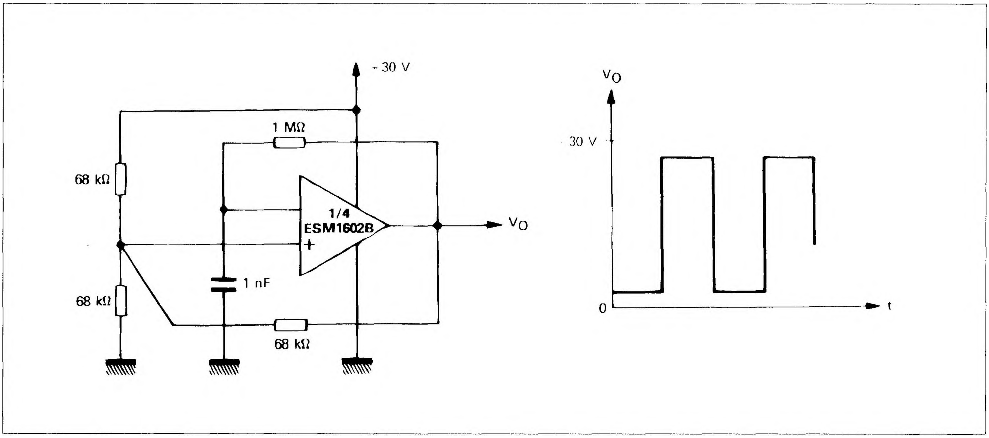


Figure 7 : Free-running Square Wave Oscillator.



TEST CIRCUITS

Figure 8.

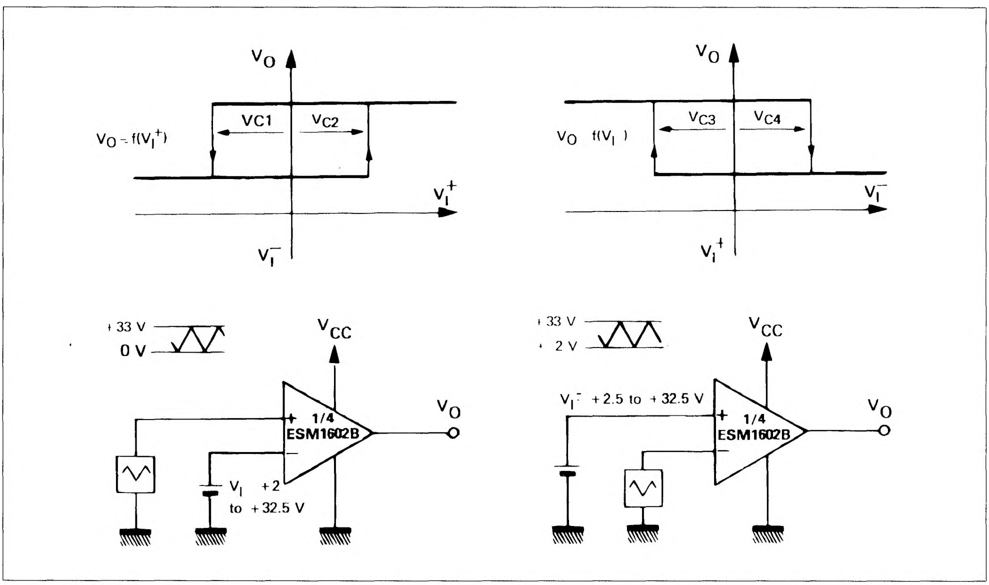


Figure 9.

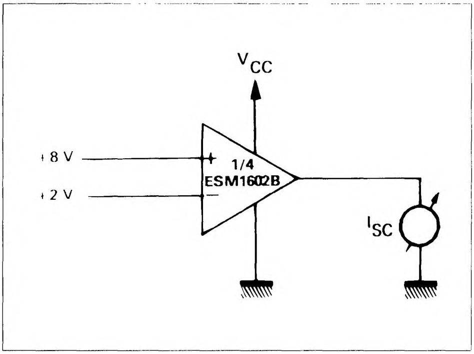


Figure 10.

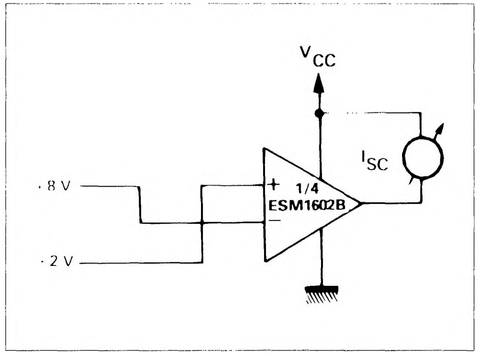


Figure 11.

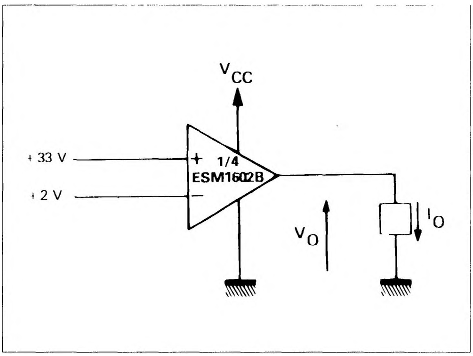


Figure 12.

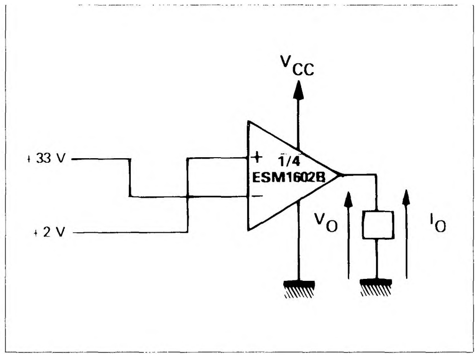


Figure 13.

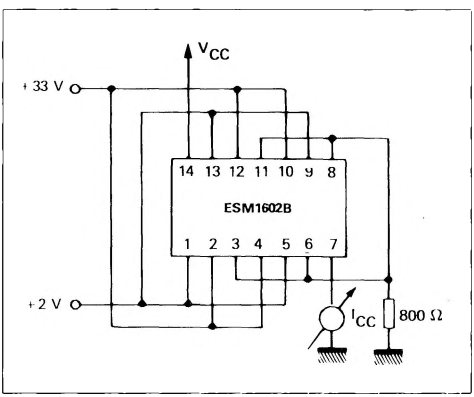


Figure 14.

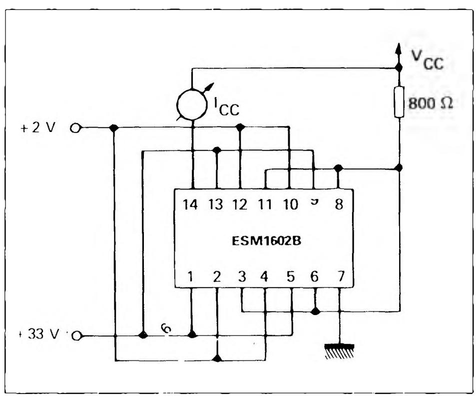


Figure 15.

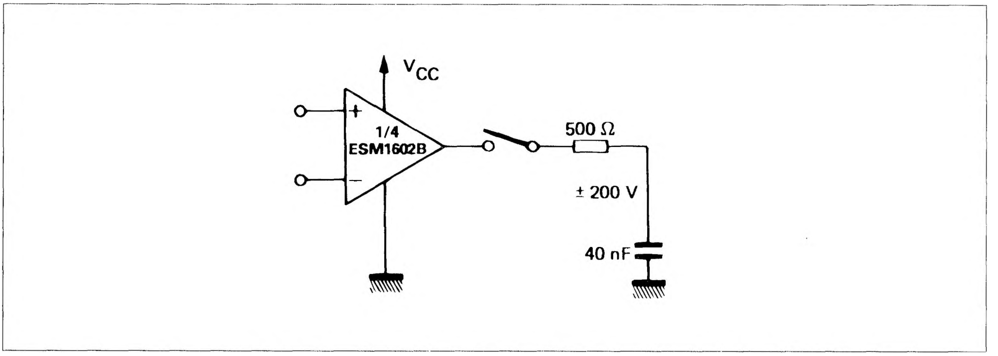


Figure 16 : Response Time.