SGS-THOMSON
MICROELECTRONICS

ETC5040X
ETC5040AX

EXTENDED TEMPERATURE RANGE
PCM MONOLITHIC FILTER

- EXCEEDS ALL D3/D4 AND CCITT SPECIFICATIONS
- + 5 V, – 5 V POWER SUPPLIES
- LOW POWER CONSUMPTION :
- 45 mW (600 Ω -0 dBm load)
- 30 mW (power amps disabled)
- POWER DOWN MODE : 0.5 mW
- 20 dB GAIN ADJUST RANGE
- NO EXTERNAL ANTI-ALIASING COMPONENTS
- SIN x/x CORRECTION IN RECEIVE FILTER
- 50/60 Hz REJECTION IN TRANSMIT FILTER
- TTL AND CMOS COMPATIBLE LOGIC
- ALL INPUTS PROTECTED AGAINST STATIC DISCHARGE DUE TO HANDLING

DIP16
(Ceramic)

ORDER CODES : ETC5040X
ETC5040AX

DESCRIPTION

The ETC5040A filter is a monolithic circuit containing both transmit and receive filters specifically designed for PCM CODEC filtering applications in 8 kHz sampled systems.

The filter is manufactured using double-poly silicon gate CMOS technology. Switched capacitor integrators are used to simulate classical LC ladder filters which exhibit low component sensitivity.

TRANSMIT FILTER STAGE

The transmit filter is fifth order elliptic low pass filter in series with a fourth order Chebychev high pass filter. It provides a flat response in the passband and rejection of signals below 200 Hz and above 3.4 kHz.

RECEIVE FILTER STAGE

The receive filter is a fifth order elliptic low pass filter designed to reconstruct the voice signal from the decoded/demultiplexed signal which, as a result of the sampling process, is a stair-step signal having the inherent sin x/x frequency response. The receive filter approximates the function required to compensate for the degraded frequency response and restore the flat pass-band response.
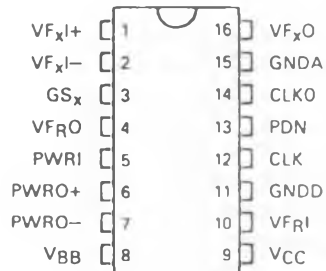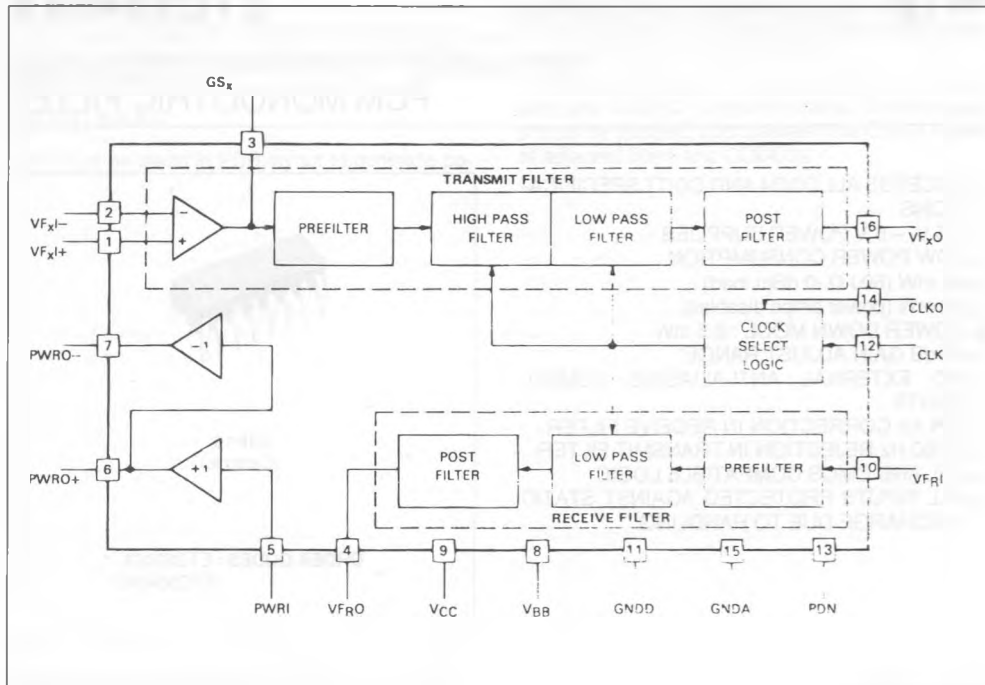
PIN CONNECTION

VF_xI+	1	16 VF_xO
VF_xI-	2	15 GNDA
GS_x	3	14 CLKO
VF_RO	4	13 PDN
PWRI	5	12 CLK
PWRO+	6	11 GNDD
PWRO–	7	10 VF_RI
V_{BB}	8	9 V_{CC}

Figure 1 : Block Diagram.

PIN DESCRIPTION

Name	Pin Type	N°	Description
VF_xI^+	I	1	The Non-inverting Input to the Transmit Filter Stage
VF_xI^-	I	2	The Inverting Input to the Transmit Filter Stage
GS_x	O	3	The output used for gain adjustments of the transmit filter.
VF_RO	O	4	The Low Power Receive Filter Output. This pin can directly drive the receive port of an electronic hybrid.
PWRI	I	5	The Input to the Receive Filter Defferential Power Amplifier
PWRO$^+$	O	6	The Non-inverting Output of the Receive Filter Power Amplifier. This output can directly interface conventional transformer hybrids.
PWRO$^-$	O	7	The Inverting Output of the Receive Filter Power Amplifier. This output can be used with PWRO$^+$ to differentially drive a transformer hybrid.
V_{BB}	S	8	The Negative Power Supply Pin. Recommended input is -5 V.
V_{CC}	S	9	The Positive Power Supply Pin. The recommended input is 5 V.
VF_RI	I	10	The Input Pin for the Receive Filter Stage
GNDD	GND	11	Digital Ground Input Pin. All digital signals are referenced to this pin.
CLK	I	12	Master Input Clock. Input frequency can be selected as 2.048 MHz, 1.544 MHz or 1.536 MHz.
PDN	I	13	The input pin used to power down the ETC5040/ETC5040A during idle periods. Logic 1 (V_{CC}) input voltage causes a power down condition. An internal pull-up is provided.
CLKO	I	14	This input pin selects internal counters in accordance with the CLK input clock frequency : **CLK Connect CLK to :** 2048 kHz V_{CC} 1544 kHz GNDD 1536 kHz V_{BB} An internal pull-up is provided.
GNDA	GND	15	Analog Ground Input Pin. All analog signals are referenced to this pin. Not Internally connecded to GNDD.
VF_xO	O	16	The Output of the Transmit Filter Stage

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	± 7	V
V_{in}	Input Voltage	± 7	V
T_A	Operating Temperature Range	-25 to $+125$	°C
T_{stg}	Storage Temperature	-65 to $+150$	°C
P_D	Power Dissipation	1/Package	W
	Output Short-circuit Duration	Continuous	
	Lead Temperature	300	°C

DC ELECTRICAL CHARACTERSITICS

$T_A = 40\ °C$ to $+ 85\ °C$, $V_{CC} = 5.0\ V \pm 5\ \%$, $V_{BB} = - 5.0\ V \pm 5\ \%$, clock frequency is 2.048 MHz. Typical parameters are specified at $T_A = + 25\ °C$, $V_{CC} = 5.0\ V$, $V_{BB} = - 5.0\ V$ (unless otherwise specified). Digital interface voltages measured with respect to digital ground, GNDD. Analog voltages measured with respect to analog ground, GNDA.

POWER DISSIPATION

Symbol	Parameter	Min.	Typ.	Max.	Unit
I_{CCO}	V_{CC} Standby Current (PDN = V_{DD}, power down mode)	–	–	400	μA
I_{BBO}	V_{BB} Standby Current (PDN = V_{DD}, power down mode)	– 400	–	–	μA
I_{CC1}	V_{CC} Operating Current (PWRI = V_{BB}, power amp inactive)	–	–	5.0	mA
I_{BB1}	V_{BB} Operating Current (PWRI = V_{BB}, power amp inactive)	– 5.0	–	–	mA
I_{CC2}	V_{CC} Operating Current (note 1)	–	–	7.0	mA
I_{BB2}	V_{BB} Operating Current (note 1)	–7.0	–	–	mA

DIGITAL INTERFACE

Symbol	Parameter	Min.	Typ.	Max.	Unit
I_{INC}	Input Current, CLK ($0\ V \leq V_{IN} \leq V_{CC}$)	– 10	–	10	μA
I_{INP}	Input Current, PDN ($0\ V \leq V_{IN} \leq V_{CC} - 2\ V$)	– 100	–	–	μA
I_{INO}	Input Current, CLKO ($V_{BB} \leq V_{IN} \leq V_{CC} - 2\ V$)	– 10	–	– 0.1	μA
V_{IL}	Input Low Voltage, CLK, PDN	0	–	0.8	V
V_{IH}	Input High Voltage, CLK, PDN	2.2	–	V_{CC}	V
V_{ILO}	Input Low Voltage, CLKO	V_{BB}	–	$V_{BB} + 0.5$	V
V_{IIO}	Input Intermediate Voltage, CLKO	– 0.8	–	0.8	V
V_{IHO}	Input High Voltage, CLKO	$V_{CC} - 0.5$	–	V_{CC}	V

TRANSMIT INPUT AMP. OP.

Symbol	Parameter	Min.	Typ.	Max.	Unit
$IB_x I$	Input Leakage Current, $VF_x I$ ($V_{BB} \leq VF_x I \leq V_{CC}$)	– 100	–	100	nA
$RI_x I$	Input Resistance $VF_x I$ ($V_{BB} \leq VF_x I \leq V_{CC}$)	10	–	–	MΩ
$VOS_x I$	Input Offset Voltage, $VF_x I$ ($- 2.5 \leq V_{IN} \leq + 2.5\ V$)	– 20	–	20	mV
V_{CM}	Common-mode Range, $VF_x I$	– 2.5	–	2.5	V
CMRR	Common-mode Rejection Ratio ($- 2.5\ V \leq V_{IN} \leq 2.5\ V$)	60	–	–	dB
PSRR	Power Supply Rejection of V_{CC} or V_{BB}	60	–	–	dB
R_{OL}	Open Loop Output Resistance GS_x	–	1	–	kΩ
R_L	Minimum Load Resistance, GS_x	10	–	–	kΩ
C_L	Maximum Load Capacitance, GS_x	–	–	100	pF
$V_{Ox} I$	Output Voltage Swing, GS_x ($R_L \geq 10\ k\Omega$)	± 2.5	–	–	V
A_{VOL}	Open Loop Voltage Gain, GS_x ($R_l \geq 10\ k\Omega$)	5.000	–	–	V/V
F_C	Open Loop Unity Gain Bandwidth, GS_x	–	2	–	MHz

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AC ELECTRICAL CHARACTERSITICS

$T_A = -40$ C to 85 C All parameters are specified for a signal level of 0 dBm0 at 1 kHz. The 0 dBm0 level is assumed to be 1.54 Vrms measured at the output of the transmit or receive filter. (unless otherwise specified).

TRANSMIT FILTER (note 2)

Symbol	Parameter		Min.	Typ.	Max.	Unit
RL_x	Minimum Load Resistance -2.5 V $< V_{OUT} < +2.5$ V -3.2 V $< V_{OUT} < +3.2$ V		3 10	– –	– –	kΩ
CL_x	Load Capacitance VF_xO		–	–	100	pF
	Output Resistance, VF_xO		–	–	4	Ω
PSRR1	V_{CC} Power Supply Rejection VF_xI (f = 1 kHz, $VF_xI+ = 0$ Vrms)		30	–	–	dB
PSRR2	V_{BB} Power Supply Rejection, VF_xO. (same as above)		35	–	–	dB
GA_x	Absolute Gain (f = 1 kHz) ETC5040A ETC5040		2.850 2.875		3.100 3.125	dB
GR_x	Gain Relative to GA_x Below 50 Hz 50 Hz 60 Hz 200 Hz ETC5040 ETC5040A 300 Hz to 3 kHz ETC5040 ETC5040A 3.3 kHz ETC5040 ETC5040A 3.4 kHz 4.0 kHz 4.6 kHz and Above		– – – – 1.5 – 1.5 – 0.125 – 0.15 – 0.35 – 0.35 – 0.70 – –	– – 41 – 35 – – – – – – – – 15 –	– 35 – 35 – 30 0.1 0.05 0.125 0.15 0.15 0.125 – 0.1 – 14 – 32	dB
DA_x	Absolute Delay at 1 kHz		–	–	230	µs
	Differential Envelope Delay from 1 kHz to 2.6 kHz		–	–	60	µs
DP_x1	Single Frequency Distortion Products		–	–	– 48	dB
DP_x2	Distortion at Maximum Signal Level 1.6 Vrms, 1 kHz Signal applied to VF_xI+, Gain = 20 dB. $R_L = 10$ kΩ		– –	– –	– 45	dB
NC_x1	Total C Message Noise at VF_xO		–	–	6	dBrncO
NCx2	Total C Message Noise at VF_xO Gain setting Op Amp at 20 dB, non Inverting. Note 3, 0 °C ≤ T_A ≤ + 70 °C		– –	– –	7	dBrncO
GA_xT	Temperature Coefficient of 1 kHz Gain		–	0.0004	–	dB/°C
GA_xS	Supply Voltage Coefficient of 1 kHz Gain		–	0.01	–	dB/V
CT_{RX}	Crosstalk, Receive to Transmit 20 Log $\dfrac{VF_xO}{VF_RO}$ Receive Filter Output = 2.2 Vrms, $VF_xI+ = 0$ Vrms, f = 0.2 kHz to 3.4 kHz, Measure VF_xO		– –	– –	– 70	dB
GR_xL	Gaintracking Relative to GA_x Output Level = + 3 dBmO + 2 dBmO to – 40 dBmO – 40 dBmO to – 55 dBmO		– 0.1 – 0.05 – 0.1	– – –	0.1 0.05 0.1	dB

AC ELECTRICAL CHARACTERSITICS (continued)

RECEIVE FILTER (unless otherwise noted, the receive filter is preceded by a sin x/x filter within an input signal level of 1.54 Vrms).

Symbol	Parameter	Min.	Typ.	Max.	Unit
IB_R	Input Leakage Current, VF_RI ($-3.2\ V \leq VIN \leq 3.2\ V$)	-100	$-$	100	nA
RI_R	Input Resistance, VF_RI	10	$-$	$-$	MΩ
RO_R	Output Resistance, VF_RO	$-$	$-$	4	Ω
CL_R	Load Capacitance, VF_RO	$-$	$-$	100	pF
RL_R	Load Resistance, VF_RO	10	$-$	$-$	kΩ
PSRR3	Power Supply Rejection of V_{CC} or V_{BB} (VF_RO VF_RI connected to GNDA, f = 1 kHz)	35	$-$	$-$	dB
VOS_RO	Output DC Offset, VF_RO (VF_RI connected to GNDA)	-200	$-$	$+200$	mV
GA_R	Absolute Gain (f = 1 kHz) ETC5040 ETC5040A	 -0.15 -0.125	 $-$ $-$	 0.15 0.125	dB
GR_R	Gain Relative to Gain at 1 kHz below 300 Hz 300 Hz to 3.0 kHz ETC5040 ETC5040A 3.3 kHz 3.4 kHz 4.0 kHz 4.6 kHz and above	$-$ -0.15 -0.175 -0.35 -0.70 $-$ $-$	$-$ $-$ $-$ $-$ $-$ $-$ $-$	0.15 0.15 0.175 0.03 -0.1 -14 -32	dB
DA_R	Absolute Delay at 1 kHz	$-$	$-$	100	µs
DD_R	Differential Envelope Delay 1 kHz to 2.6 kHz	$-$	$-$	100	µs
DP_R1	Single Frequency Distortion Products (f = 1 kHz)	$-$	$-$	-48	dB
DP_R2	Distortion at Maximum Signal Level 2.2 Vrms Input to Sin x/x Filter, f = 1 kHz, RL = 10 kΩ	$-$	$-$	-45	dB
NC_R	Total C-message Noise at VF_RO	$-$	$-$	6	dBrnc0
GA_RT	Temperature Coefficient of 1 kHz Gain	$-$	0.0004	$-$	dB/°C
GA_RS	Supply Voltage Coefficient of 1 kHz Gain	$-$	0.01	$-$	dB/V
CT_{XR}	Crosstalk, Transmit to Receive $20 \log \dfrac{VF_RO}{VF_XO}$ (transmit filter output = 2.2 Vrms, VF_RI = 0 Vrms, f= 0.3 kHz to 3.4 kHz, measure VF_RO)	$-$	-80	-70	dB
GR_RL	Gaintraking Relative to GA_P Output Level = 3 dBm0 + 2 dBm0 to -40 dBm0 -40 dBm0 to 55 dBm0	 -0.1 -0.05 -0.1	 $-$ $-$ $-$	 0.1 0.05 0.1	dB

AC ELECTRICAL CHARACTERSITICS (continued)

RECEIVE OUTPUT POWER AMPLIFIER

Symbol	Parameter	Min.	Typ.	Max.	Unit
IBP	Input Leakage Current. PWRI (-3.2 V $\leq V_{IN} \leq 3.2$ V)	0.1	–	4	µA
RIP	Input Resistance, PWRI	10	–	–	MΩ
ROP1	Output Resistance, PWRO $^+$, PWRO $^-$ (amplifier active)	–	1	–	Ω
CLP	Load Capacitance. PWRO $^-$, PWRO $^-$	–	–	500	pF
GA$_P$ $^+$	Gain, PWRI to PWRO $^+$ ($R_L = 600$ Ω connected between)	–	1	–	V/V
GA$_P$ $-$	Gain, PWRI to PWRO $^-$ PWRO $^+$ and PWRO $^-$. Input, Level = 0 dBmO (note 4)	–	-1	–	V/V
GR$_P$L	Gaintraking Relative to OdBmO Output Level V = 2.05 Vrms. $R_L = 600$ Ω (notes 4, 5) V = 1.75 Vrms, $R_L = 300$ Ω (notes 4, 5)	-0.1 -0.1	– –	0.1 0.1	dB
S/D$_P$	Signal / Distortion V = 2.05 Vrms. $R_L = 600$ Ω (notes 4, 5) V = 1.75 Vrms. $R_L = 300$ Ω (notes 4, 5)	– –	– –	-45 -45	dB
VOSP	Output DC Offset. PWRO $^+$, PWRO $^-$ (PWRI connected to GNDA)	-50	–	50	mV
PSRR5	Power Supply Rejection of V_{CC} ot V_{BB} (PWRI connected to GNDA)	45	–	–	dB

Notes : 1. Maximum power consumption depend on the load impedance connected to the power amplifier. The specification listed assumes 0 dBm is delivered to 600 Ω connected from PWRO + PWRO.
2. Transmit filter input op amp set to the non inverting unity gain mode, with VF$_x$I+ = 1.1 Vrms, unless otherwise noted.
3. The 0 dBm level for the filter is assumed to be 1.54 Vrms measured at the output of the XMT or RCV filter.
4. The 0 dBm0 level for the power amplifiers is load dependent. For $R_L = -600$ Ω to GNDA, the 0 dBm0 level is 1.43 Vrms measured at the amplifier output. For $R_L = 300$ Ω the 0dBm0 level is 1.22 Vrms.
5. VF$_R$O connected to PWRI, input signal applied to VF$_R$I.

TYPICAL PERFORMANCE CHARACTERISTICS

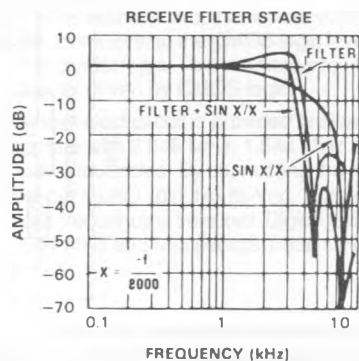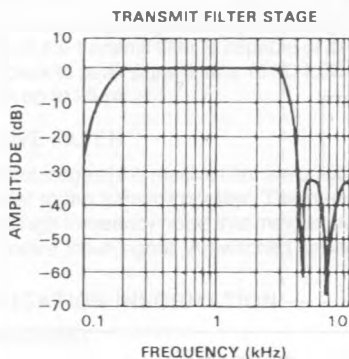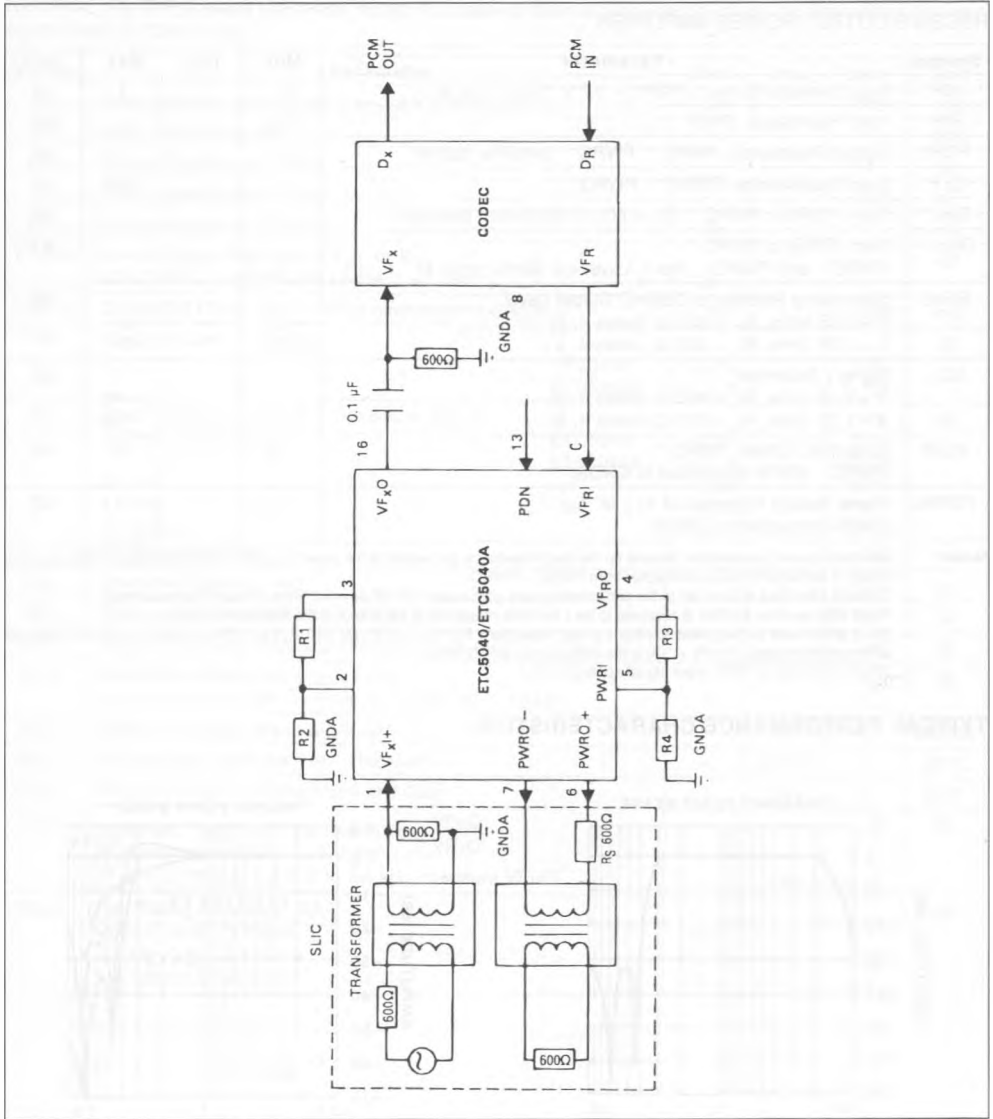TRANSMIT FILTER STAGE

RECEIVE FILTER STAGE

Figure 2 : Interface Circuit for CODEC.

Notes : 1. Transmit voltage gain = $\dfrac{R1 + R2}{R2} \times \sqrt{2}$ (the filter itself introduces a 3 dB gain) (R1 + R2 ⩾ 10 KΩ).

2. Receive gain = $\dfrac{R4}{R3 + R4}$

(R3 + R4 > 10 kΩ)

3. In the configuration shown, the receive filter power amplifiers will drive a 600 Ω T or R termination to a signal level of 8.5 dBm. An alternative arrangement using a transformer winding ratio equivalent to 1.414 1 and 300 Ω resistor Rs will provide a maximum signal level of 10 dBm across 600 Ω termination impedance.

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FUNCTIONAL DESCRIPTION

ETC 5040A monolithic filter contains four main sections ; Transmit Filter. Receive Filter, Receive Filter Power Amplifier, and Frequency Divider/Select Logic (figure 1). A brief description of the circuit operation for each section is provided below.

TRANSMIT FILTER

The input stage of the transmit filter is a CMOS operational amplifier which provides an input resistance greater than 10 MΩ, a voltage gain of greater than 10.000 low power consumption (less than 3 mW), high power supply rejection. and is capable of driving a 10 kΩ load parallel with up to 25 pF. The inputs and output of the amplifier are accessible for added flexibility. Non-inverting mode, inverting mode. or differential amplifier mode operation can be implemented with external resistors. It can also be connected to provide a gain of up to 20 dB without degrading the overall filter performance.

The input stage is followed by a prefilter which is two-pole RC active low pass filter designed to attenuate high frequency noise before the input signal enters the switched-capacitor high pass and low pass filters.

A high pass filter is provided to reject 200 Hz or lower noise which may exist in the signal path. The low pass portion of the switched-capacitor filter provides stopband attenuation which exceeds the D3 and D4 specifications as well as the CCITT G712 recommendations.

The output of the transmit filter, the postfilter, is also a two-pole RC active low pass filter which attenuates clock frequency noise by at least 40 dB. The output of the transmit filter is capable of driving a $\pm$ 3.2 V peak to peak signal into a 10 kΩ load in parallel with up to 25 pF.

RECEIVE FILTER

The input stage of the receive filter is a prefilter which is similar to the transmit prefilter. The prefilter attenuates high frequency noise that may be present on the receive input signal. A switched capacitor low pass filter follows the prefilter to provide the necessary passband flatness, stopband rejection and sin x/x gain correction. A postfilter which is similar to the transmit postfilter follows the low pass stage. It attenuates clock frequency noise and provides a low output impedance capable of directly driving an electronic subscriber-line-interface circuit.

RECEIVE FILTER POWER AMPLIFIERS

Two power amplifiers are also provided to interface to transformer coupled line circuits. These two amplifiers are driven by the output of the receive postfilter through gain setting resistors, R3, R4 (figure 2). The power amplifiers can be deactivated, when not required. by connecting the power amplifier input (pin 5) to the negative power supply V_{BB}. This reduces the total filter power consumption by approximately 10 mW-20 mW depending on output signal amplitude.

POWER DOWN CONTROL

A power down mode is also provided. A logic 1 power down command applied on the PDN pin (pin 13) will reduce the total filter power consumption to less than 1 mW and turn the power amplifier outputs into high impedance state.

FREQUENCY DIVIDER AND SELECT LOGIC CIRCUIT

This circuit divides the external clock frequency down to the switching frequency of the low pass switched capacitor filters. The divider also contains a TTL-CMOS interface circuit which converts the external TTL clock level to the CMOS logic level required for the divider logic. This interface circuit can also be directly driven by CMOS logic.

A frequency select circuit is provided to allow the filter to operate with 2.048 MHz, 1.544 MHz or 1.536 MHz clock frequencies. By connecting the frequency select pin CLKO (pin 14) to V_{CC}, a 2.048 MHz clock input frequency is selected. Digital ground selects 1.544 MHz and V_{BB} selects 1.536 MHz.

APPLICATION INFORMATION

GAIN ADJUST

Figure 2 shows the signal path interconnections between the ETC5040/ETC5040A and single-channel CODEC. The transmit RC coupling components have been chosen both for minimum passband droop and to present the correct impedance to the CODEC during sampling.

Optimum noise and distortion performance will be obtained from the ETC5040/ETC5040A filter when operated with system peak overload voltages of $\pm$ 2.5 V to $\pm$ 3.2 V at VFxO and VF$_R$O. When interfacing to a PCM CODEC with a peak overload voltage outside this range, further gain or attenuation may be required.