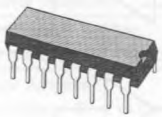
SGS-THOMSON MICROELECTRONICS

# ETC5040
# ETC5040A

## PCM MONOLITHIC FILTER

- EXCEEDS ALL D3/D4 AND CCITT SPECIFICATIONS
- + 5V, – 5V POWER SUPPLIES
- LOW POWER CONSUMPTION :
  45mW (600Ω – 0dBm load)
  30mW (power amps disabled)
- POWER DOWN MODE : 0.5mW
- 20 dB GAIN ADJUST RANGE
- NO EXTERNAL ANTI-ALIASING COMPONENTS
- SIN x/x CORRECTION IN RECEIVE FILTER
- 50/60Hz REJECTION IN TRANSMIT FILTER
- TTL AND CMOS COMPATIBLE LOGIC
- ALL INPUTS PROTECTED AGAINST STATIC DISCHARGE DUE TO HANDLING



**DIP16**
(Ceramic)

**ORDER CODES :** ETC5040J
ETC5040AJ

### DESCRIPTION

The ETC5040/ETC5040A filter is a monolithic circuit containing both transmit and receive filters specifically designed for PCM CODEC filtering applications in 8kHz sampled systems.

The filter is manufactured using double-poly silicon gate CMOS technology. Switched capacitor integrators are used to simulate classical LC ladder filters which exhibit low component sensitivity.

#### TRANSMIT FILTER STAGE

The transmit filter is fifth order elliptic low pass filter in series with a fourth order Chebychev high pass filter. It provides a flat response in the passband and rejection of signals below 200Hz and above 3.4kHz.

#### RECEIVE FILTER STAGE

The receive filter is a fifth order elliptic low pass filter designed to reconstruct the voice signal from the decoded/demultiplexed signal which, as a result of the sampling process, is a stair-step signal having the inherent sin x/x frequency response. The receive filter approximates the function required to compensate for the degraded frequency response and restores the flat pass-band response.

### PIN CONNECTION

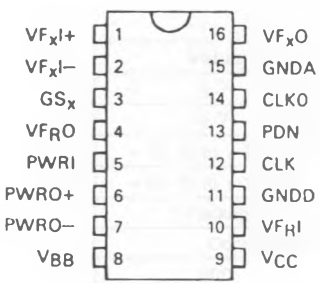
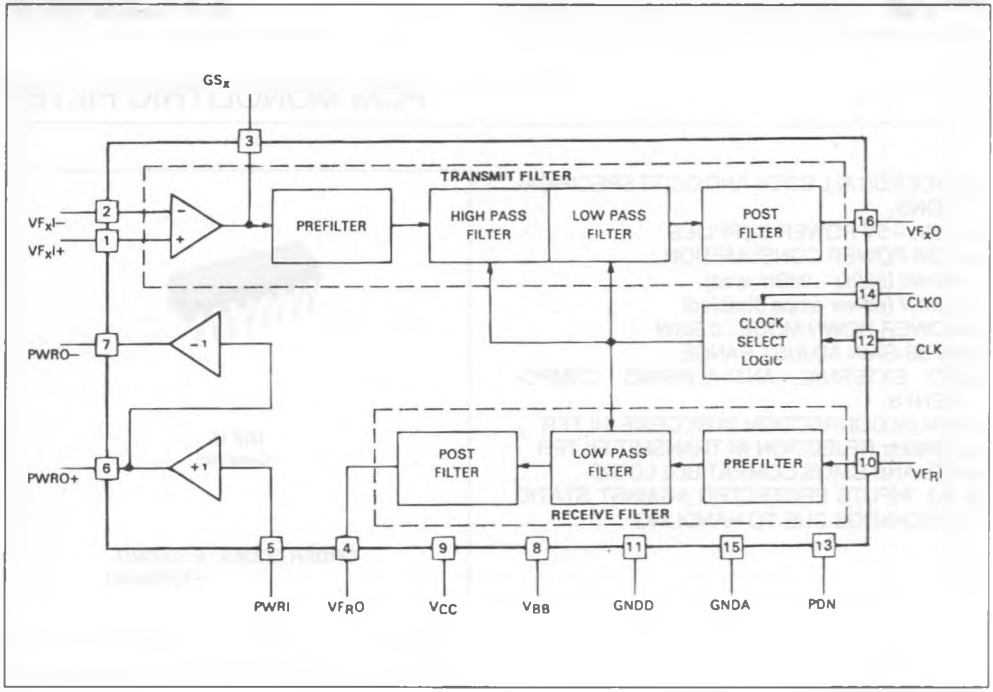


**Figure 1 :** Block Diagram.



## PIN DESCRIPTION

| Name | Pin Type | N° | Description |
|---|---|---|---|
| $VF_XI^+$ | I | 1 | The Non-inverting Input to the Transmit Filter Stage |
| $VF_XI^-$ | I | 2 | The Inverting Input to the Transmit Filter Stage |
| $GS_x$ | O | 3 | The output used for gain adjustments of the transmit filter |
| $VF_RO$ | O | 4 | The Low Power receive Filter Output. This pin can directly drive the receive port of an electronic hybrid. |
| PWRI | I | 5 | The Input to the Receive Filter Defferential Power Amplifier. |
| $PWRO^+$ | O | 6 | The Non-inverting Output of the receive Filter Power Amplifier. This output can directly interface conventional transformer hybrids. |
| $PWRO^-$ | O | 7 | The Inverting Output of the receive Filter Power Amplifier. This output can be used with $PWRO^+$ to differentially drive a transformer hybrid. |
| $V_{BB}$ | S | 8 | The Negative Power Supply Pin. Recommended input is – 5 V. |
| $V_{CC}$ | S | 9 | The Positive Power Supply Pin. The recommended input is 5 V. |
| $VF_RI$ | I | 10 | The Input Pin for the Receive Filter Stage. |
| GNDD | GND | 11 | Digital Ground Input Pin. All digital signals are referenced to this pin. |
| CLK | I | 12 | Master Input Clock. Input frequency can be selected as 2.048 MHz, 1.544 MHz or 1.536 MHz. |
| PDN | I | 13 | The input pin used to power down the ETC5040/ETC5040A during idle periods. Logic 1 ($V_{CC}$) input voltage causes a power down condition. An Internal Pull-up is provided. |
| CLKO | I | 14 | This input pin selects internal counters in accordance with the CLK input clock frequency :<br>CLK Connect CLKO to :<br>2048 kHz $V_{CC}$<br>1544 kHz GNDD<br>1536 kHz $V_{BB}$<br>An Internal Pull-up is provided. |
| GNDA | GND | 15 | Analog Ground Input Pin. All analog signals are referenced to this pin. Not internally connected to GNDD. |
| $VF_xO$ | O | 16 | The Output of the Transmit Filter Stage. |

## ABSOLUTE MAXIMUM RATINGS

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{CC}$ | Supply Voltage | ± 7 | V |
| $V_{in}$ | Input Voltage | ± 7 | V |
| $T_A$ | Operating Temperature Range | – 25 °C to + 125 °C | °C |
| $T_{stg}$ | Storage Temperature | – 65 °C to + 150 °C | °C |
| $P_D$ | Power Dissipation | 1/Package | W |
| | Output Short-circuit Duration | Continuous | |
| | Lead Temperature | 300 | °C |

## DC ELECTRICAL CHARACTERISTICS

$T_A$ = 0 °C to + 70 °C, $V_{CC}$ = 5.0 V ± 5 %, $V_{BB}$ = – 5.0 V ± 5 %, clock frequency is 2.048 MHz. Typical parameters are specified at $T_A$ = + 25 °C, $V_{CC}$ = 5.0 V, $V_{BB}$ = – 5.0 V (unless otherwise specified). Digital interface voltages measured with respect to digital ground, GNDD. Analog voltages measured with respect to analog ground, GNDA.

POWER DISSIPATION

| Symbol | Parameter | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| $I_{CCO}$ | $V_{CC}$ Standby Current (PDN = $V_{CC}$, power down mode) | – | 50 | 100 | µA |
| $I_{BBO}$ | $V_{BB}$ Standby Current (PDN = $V_{CC}$, power down mode) | – 100 | – 50 | – | µA |
| $I_{CC1}$ | $V_{CC}$ Operating Current (PWRI = $V_{BB}$, power amp inactive) | – | 3.0 | 4.0 | mA |
| $I_{BB1}$ | $V_{BB}$ Operating Current (PWRI = $V_{BB}$, power amp inactive) | – 4.0 | – 3.0 | – | mA |
| $I_{CC2}$ | $V_{CC}$ Operating Current (note 1) | – | 4.6 | 6.4 | mA |
| $I_{BB2}$ | $V_{BB}$ Operating Current (note 1) | – 6.4 | – 4.6 | – | mA |

DIGITAL INTERFACE

| Symbol | Parameter | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| $I_{INC}$ | Input Current, CLK (0 V ≤ $V_{IN}$ ≤ $V_{CC}$) | – 10 | – | 10 | µA |
| $I_{INP}$ | Input Current, PDN (0 V ≤ $V_{IN}$ ≤ $V_{CC}$ – 2 V) | – 100 | – | – | µA |
| $I_{INO}$ | Input Current, CLKO ($V_{BB}$ ≤ $V_{IN}$ ≤ $V_{CC}$ – 2 V) | – 10 | – | – 0.1 | µA |
| $V_{IL}$ | Input Low Voltage, CLK, PDN | 0 | – | 0.8 | V |
| $V_{IH}$ | Input High Voltage, CLK, PDN | 2.2 | – | $V_{CC}$ | V |
| $V_{ILO}$ | Input Low Voltage, CLKO | $V_{BB}$ | – | $V_{BB}$ + 0.5 | V |
| $V_{IIO}$ | Input Intermediate Voltage, CLKO | – 0.8 | – | 0.8 | V |
| $V_{IHO}$ | Input High Voltage, CLKO | $V_{CC}$ – 0.5 | – | $V_{CC}$ | V |

TRANSMIT INPUT AMP. OP.

| Symbol | Parameter | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| $IB_xI$ | Input Leakage Current, $VF_xI$ ($V_{BB}$ ≤ $VF_xI$ ≤ $V_{CC}$) | – 100 | – | 100 | nA |
| $RI_xI$ | Input Resistance $VF_xI$ ($V_{BB}$ ≤ $VF_xI$ ≤ $V_{CC}$) | 10 | – | – | MΩ |
| $VOS_xI$ | Input Offset Voltage, $VF_xI$ (– 2.5 ≤ $V_{IN}$ ≤ + 2.5 V) | – 20 | – | 20 | mV |
| $V_{CM}$ | Common-mode Range, $VF_xI$ | – 2.5 | – | 2.5 | V |
| CMRR | Common-mode Rejection Ratio (– 2.5 V ≤ $V_{IN}$ ≤ 2.5 V) | 60 | – | – | dB |
| PSRR | Power Supply Rejection of $V_{CC}$ or $V_{BB}$ | 60 | – | – | dB |
| $R_{OL}$ | Open Loop Output Resistance $GS_x$ | – | 1 | – | kΩ |
| $R_L$ | Minimum Load Resistance, $GS_x$ | 10 | – | – | kΩ |
| $C_L$ | Maximum Load Capacitance, $GS_x$ | – | – | 100 | pF |
| $V_{OxI}$ | Output Voltage Swing, $GS_x$ ($R_L$ ≥ 10 kΩ) | ± 2.5 | – | – | V |
| $A_{VOL}$ | Open Loop Voltage Gain, $GS_x$ ($R_L$ ≥ 10 kΩ) | 5000 | – | – | V/V |
| $F_C$ | Open Loop Unity Gain Bandwidth, $GS_x$ | – | 2 | – | MHz |

## AC ELECTRICAL CHARACTERISTICS

$T_A$ = 25 °C. All parameters are specified for a signal level of 0dBm0 at 1kHz. The 0dBm0 level is assumed to be 1.54Vrms measured at the output of the transmit or receive filter. (unless otherwise specified).

TRANSMIT FILTER (note 2)

| Symbol | Parameter | | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $RL_x$ | Minimum Load Resistance | | | | | kΩ |
| | – 2.5 V < $V_{OUT}$ < + 2.5 V | | 3 | – | – | |
| | – 3.2 V < $V_{OUT}$ < + 3.2 V | | 10 | – | – | |
| $CL_x$ | Load Capacitance $VF_xO$ | | – | – | 100 | pF |
| | Output Resistance, $VF_xO$ | | – | 1 | 3. | Ω |
| PSRR1 | $V_{CC}$ Power Supply Rejection $VF_xI$ (f = 1 kHz, $VF_xI$+ = 0 Vrms) | | 30 | – | – | dB |
| PSRR2 | $V_{BB}$ Power Supply Rejection, $VF_xO$. (same as above) | | 35 | – | – | dB |
| $GA_x$ | Absolute Gain (f = 1 kHz) | ETC5040A | | | | dB |
| | | ETC5040 | 2.9<br>2.875 | 3.0<br>3.0 | 3.1<br>3.125 | |
| $GR_x$ | Gain Relative to $GA_x$ | | | | | dB |
| | Below 50 Hz | | – | – | – 35 | |
| | 50 Hz | | – | – 41 | – 35 | |
| | 60 Hz | | – | – 35 | – 30 | |
| | 200 Hz | ETC5040A | – 1.5 | – | 0 | |
| | | ETC5040 | – 1.5 | – | 0.05 | |
| | 300 Hz to 3 kHz | ETC5040A | – 0.125 | – | 0.125 | |
| | | ETC5040 | – 0.15 | – | 0.15 | |
| | 3.3 kHz | ETC5040A | – 0.35 | – | 0.03 | |
| | | ETC5040 | – 0.35 | – | 0.125 | |
| | 3.4 kHz | | – 0.70 | – | – 0.1 | |
| | 4.0 kHz | | – | – 15 | – 14 | |
| | 4.6 kHz and above | | – | – | – 32 | |
| $DA_x$ | Absolute Delay at 1 kHz | | – | – | 230 | µs |
| | Differencial Envelope Delay from 1 kHz to 2.6 kHz | | – | – | 60 | µs |
| $DP_x1$ | Single Frequency Distortion Products | | – | – | – 48 | dB |
| $DP_x2$ | Distortion at Maximum Signal Level<br>1.6 Vrms, 1 kHz Signal applied to $VF_xI$+, Gain = 20 dB,<br>$R_L$ = 10 kΩ | | – | – | – 45 | dB |
| $NC_x1$ | Total C Message Noise at $VF_xO$ | | – | 2 | 5 | dBrncO |
| $NC_x2$ | Total C Message Noise at $VF_xO$<br>Gain setting Op Amp at 20 dB, non Inverting, Note 3,<br>0 °C ≤ $T_A$ ≤ + 70 °C | | – | 3 | 6 | dBrncO |
| $GA_xT$ | Temperature Coefficient of 1 kHz Gain | | – | 0.0004 | – | dB/°C |
| $GA_xS$ | Supply Voltage Coefficient of 1 kHz Gain | | – | 0.01 | – | dB/V |
| $CT_{RX}$ | Crosstalk, Receive to Transmit 20 Log $\frac{VF_xO}{VF_RO}$<br>Receive Filter Output = 2.2 Vrms,<br>$VF_xI$+ = 0 Vrms, f = 0.2 kHz to 3.4 kHz, Measure $VF_xO$ | | – | – | – 70 | dB |
| $GR_xL$ | Gaintracking Relative to $GA_x$ | | | | | dB |
| | Output Level = + 3 dBmO | | – 0.1 | – | 0.1 | |
| | + 2 dBmO to – 40 dBmO | | – 0.05 | – | 0.05 | |
| | – 40 dBmO to – 55 dBmO | | – 0.1 | – | 0.1 | |

## AC ELECTRICAL CHARACTERISTICS (continued)

RECEIVE FILTER (unless otherwise noted, the receive filter is preceded by a sin x/x filter with an input signal level of 1.54 Vrms).

| Symbol | Parameter | | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $IB_R$ | Input Leakage Current, $VF_RI$ (– 3.2 V ≤ VIN ≤ 3.2 V) | | – 100 | – | 100 | nA |
| $RI_R$ | Input Resistance, $VF_RI$ | | 10 | – | – | MΩ |
| $RO_R$ | Output Resistance, $VF_RO$ | | – | 1 | 3 | Ω |
| $CL_R$ | Load Capacitance, $VF_RO$ | | – | – | 100 | pF |
| $RL_R$ | Load Resistance, $VF_RO$ | | 10 | – | – | kΩ |
| PSRR3 | Power Supply Rejection of $V_{CC}$ or $V_{BB}$<br>$VF_RO$ ($VF_RI$ connected to GNDA, f = 1 kHz) | | 35 | – | – | dB |
| $VOS_RO$ | Output DC Offset, $VF_RO$ ($VF_RI$ connected to GNDA) | | – 200 | – | + 200 | mV |
| $GA_R$ | Absolute Gain (f = 1 kHz) | | | | | dB |
| | | ETC5040A | – 0.1 | 0 | 0.1 | |
| | | ETC5040 | – 0.125 | 0 | 0.125 | |
| $GR_R$ | Gain Relative to Gain at 1 kHz below 300 Hz | | – | – | 0.125 | dB |
| | 300 Hz to 3.0 kHz | ETC5040A | – 0.125 | – | 0.125 | |
| | | ETC5040 | – 0.15 | – | 0.15 | |
| | 3.3 kHz | | – 0.35 | – | 0.03 | |
| | 3.4 kHz | | – 0.70 | – | – 0.1 | |
| | 4.0 kHz | | – | – | – 14 | |
| | 4.6 kHz and Above | | – | – | – 32 | |
| $DA_R$ | Absolute Delay at 1 kHz | | – | – | 100 | µs |
| $DD_R$ | Differential Envelope Delay 1 kHz to 2.6 kHz | | – | – | 100 | µs |
| $DP_R1$ | Single Frequency Distortion Products (f = 1 kHz) | | – | – | – 48 | dB |
| $DP_R2$ | Distortion at Maximum Signal Level<br>2.2 Vrms Input to Sin x/x Filter, f = 1 kHz, $R_L$ = 10 kΩ | | – | – | – 45 | dB |
| $NC_R$ | Total C–message Noise at $VF_RO$ | | – | 3 | 5 | dBrnc0 |
| $GA_RT$ | Temperature Coefficient of 1 kHz Gain | | – | 0.0004 | – | dB/°C |
| $GA_RS$ | Supply Voltage Coefficient of 1 kHz Gain | | – | 0.01 | – | dB/V |
| $CT_{XR}$ | Crosstalk, Transmit to Receive 20 log $\frac{VF_RO}{VF_XO}$<br>(transmit filter output = 2. 2 Vrms,<br>$VF_RI$ = 0 Vrms, f = 0.3 kHz to 3.4 kHz, measure $VF_RO$) | | – | – 80 | – 70 | dB |
| $GR_RL$ | Gaintraking Relative to $GA_R$ | | | | | dB |
| | Output Level = 3 dBm0 | | – 0.1 | – | 0.1 | |
| | + 2 dBm0 to – 40 dBm0 | | – 0.05 | – | 0.05 | |
| | – 40 dBm0 to – 55 dBm0 | | – 0.1 | – | 0.1 | |

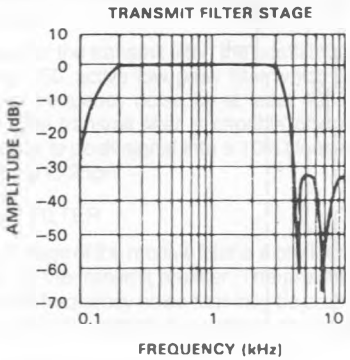
## AC ELECTRICAL CHARACTERISTICS (continued)

RECEIVE OUTPUT POWER AMPLIFIER

| Symbol | Parameter | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| IBP | Input Leakage Current, PWRI ($-3.2\ V \le V_{IN} \le 3.2\ V$) | 0.1 | – | 3 | µA |
| RIP | Input Resistance, PWRI | 10 | – | – | MΩ |
| ROP1 | Output Resistance, PWRO $^+$, PWRO $^-$ (amplifiers active) | – | 1 | – | Ω |
| CLP | Load Capacitance, PWRO $^+$, PWRO $^-$ | – | – | 500 | pF |
| $GA_P{}^+$ | Gain, PWRI to PWRO + ($R_L$ = 600 Ω connected between) | – | 1 | – | V/V |
| $GA_P{}^-$ | Gain, PWRI to PWRO –<br>PWRO $^+$ and PWRO $^-$, Input Level = 0 dBm0 (note 4) | – | – 1 | – | V/V |
| $GR_PL$ | Gaintraking Relative to OdBmO Output Level<br>V = 2.05 Vrms, $R_L$ = 600 Ω (notes 4, 5)<br>V = 1.75 Vrms, $R_L$ = 300 Ω (notes 4, 5) | <br>– 0.1<br>– 0.1 | <br>–<br>– | <br>0.1<br>0.1 | dB |
| $S/D_P$ | Signal/Distortion<br>V = 2.05 Vrms, $R_L$ = 600 Ω (notes 4, 5)<br>V = 1.75 Vrms, $R_L$ = 300 Ω (notes 4, 5) | <br>–<br>– | <br>–<br>– | <br>– 45<br>– 45 | dB |
| VOSP | Output DC offset, PWRO $^+$, PWRO $^-$ (PWRI connected to GNDA) | – 50 | – | 50 | mV |
| PSRR5 | Power Supply Rejection of $V_{CC}$ or $V_{BB}$<br>(PWRI connected to GNDA) | 45 | – | – | dB |

**Notes :** 1. Maximum power consumption depend on the load impedance connected to the power amplifier. The specification listed assumes 0 dBm is delivred to 600Ω connected from PWRO + PWRO.
2. Transmit filter input op amp set to the non inverting unity gain mode, with $VF_xI+$ = 1.1Vrms, unless otherwise noted.
3. The 0dBm level for the filter is assumed to be 1.54Vrms measured at the output of the XMT or RCV filter.
4. The 0dBm0 level for the power amplifiers is load dependent. For $R_L$ = – 600Ω to GNDA, the 0dBm0 level is 1.43Vrms measured at the amplifier output. For $R_L$ = 300Ω the 0dBm0 level is 1.22Vrms.
5. $VF_RO$ connected to PWRI, input signal applied to $VF_RI$.

## TYPICAL PERFORMANCE CHARACTERISTICS



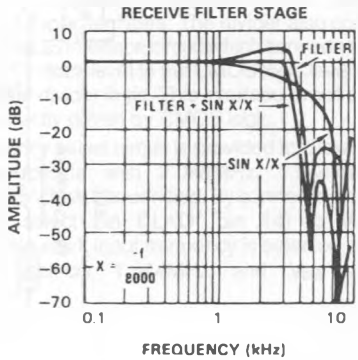
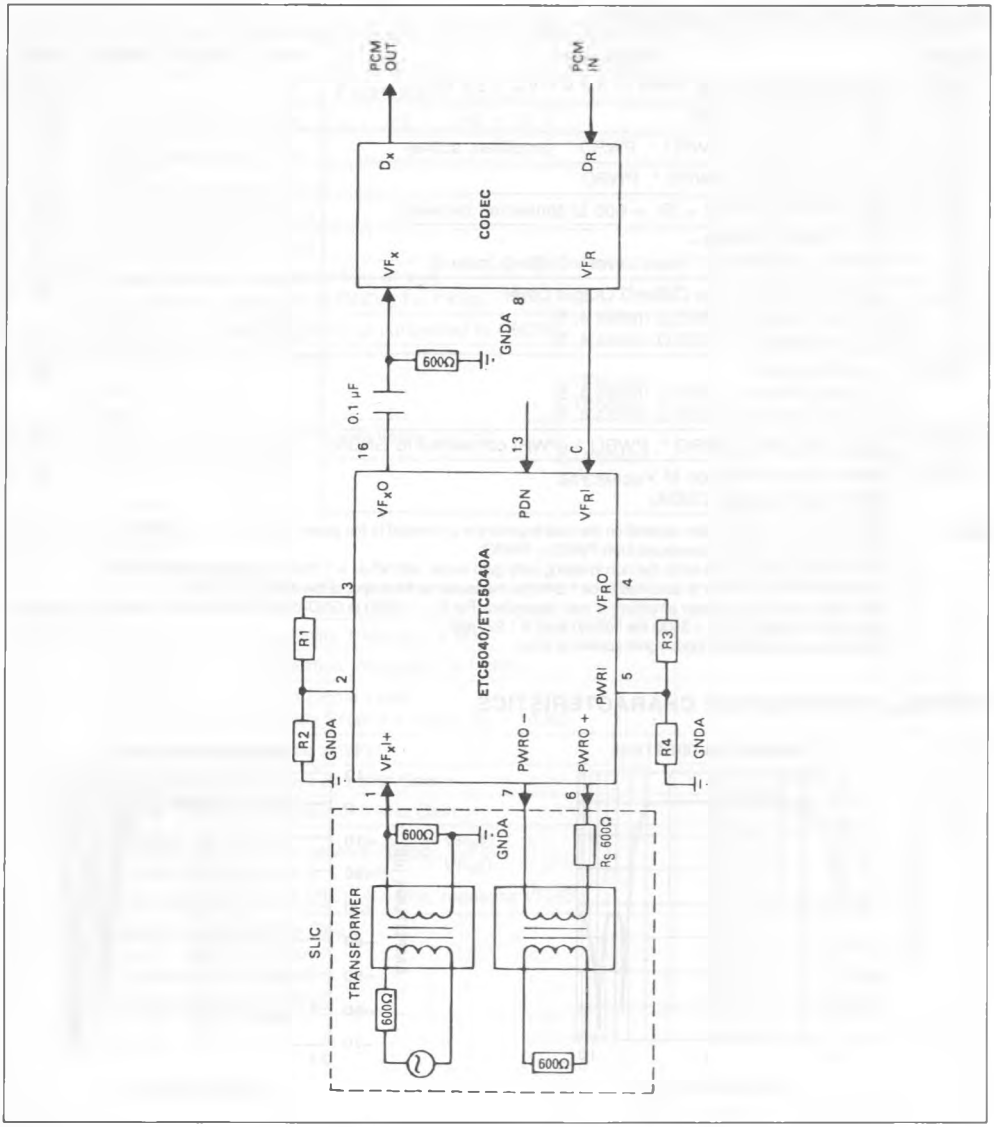



**Figure 2 :** Interface Circuit for CODEC.




**Notes :** 1. Transmit voltage gain = $\frac{R1 + R2}{R2} \times \sqrt{2}$ (the filter itself introduces a 3dB gain) (R1 + R2 ≥ 10kΩ).

2. Receive gain = $\frac{R4}{R3 + R4}$
(R3 + R4 ≥ 10kΩ)

3. In the configuration shown, the receive filter power amplifiers will drive a 600Ω T or R termination to a signal level of 8.5dBm. An alternative arrangement using a transformer winding ratio equivalent to 1.414 : 1 and 300Ω resistor $R_S$ will provide a maximum signal level of 10dBm across 600Ω termination impedance.

## FUNCTIONAL DESCRIPTION

The ETC 5040/ETC 5040A monolithic filter contains four main sections ; Transmit Filter, Receive Filter, Receive Filter Power Amplifier, and Frequency Divider/Select Logic (figure 1). A brief description of the circuit operation for each section is provided below.

### TRANSMIT FILTER

The input stage of the transmit filter is a CMOS operational amplifier which provides an input resistance greater than 10MΩ, a voltage gain of greater than 5.000, low power consumption (less than 3mW), high power supply rejection, and is capable of driving a 10kΩ load in parallel with up to 25pF. The inputs and output of the amplifier are accessible for added flexibility. Non-inverting mode, inverting mode, or differential amplifier mode operation can be implemented with external resistors. It can also be connected to provide a gain of up to 20dB without degrading the overall filter performance.

The input stage is followed by a prefilter which is a two pole RC active low pass filter designed to attenuate high frequency noise before the input signal enters the switched-capacitor high pass and low pass filters.

A high pass filter is provided to reject 200Hz or lower noise which may exist in the signal path. The low pass portion of the switched-capacitor filter provides stopband attenuation which exceeds the D3 and D4 specifications as well as the CCITT G712 recommendations.

The output of the transmit filter, the postfilter, is also a two-pole RC active low pass filter which attenuates clock frequency noise by at least 40dB. The output of the transmit filter is capable of driving a ± 3.2V peak to peak signal into a 10kΩ load in parallel with up to 25pF.

### RECEIVE FILTER

The input stage of the receive filter is a prefilter which is similar to the transmit prefilter. The prefilter attenuates high frequency noise that may be present on the receive input signal. A switched capacitor low pass filter follows the prefilter to provide the necessary passband flatness, stopband rejection and sin x/x gain correction. A postfilter which is similar to the transmit postfilter follows the low pass stage. It attenuates clock frequency noise and provides a low output impedance capable of directly driving an electronic subscriber-line-interface circuit.

### RECEIVE FILTER POWER AMPLIFIERS

Two power amplifiers are also provided to interface to transformer coupled line circuits. These two amplifiers are driven by the output of the receive postfilter through gain setting resistors, R3, R4 (figure 2). The power amplifiers can be deactivated, when not required, by connecting the power amplifier input (pin 5) to the negative power supply $V_{BB}$. This reduces the total filter power consumption by approximately 10mW-20mW depending on output signal amplitude.

### POWER DOWN CONTROL

A power down mode is also provided. A logic 1 power down command applied on the PDN pin (pin 13) will reduce the total filter power consumption to less than 1mW and turn the power amplifier outputs into high impedance state.

### FREQUENCY DIVIDER AND SELECT LOGIC CIRCUIT

This circuit divides the external clock frequency down to the switching frequency of the low pass switched capacitor filters. The divider also contains a TTL-CMOS interface circuit which converts the external TTL clock level to the CMOS logic level required for the divider logic. This interface circuit can also be directly driven by CMOS logic.

A frequency select circuit is provided to allow the filter to operate with 2.048MHz, 1.544MHz or 1.536MHz clock frequencies. By connecting the frequency select pin CLKO (pin 14) to $V_{CC}$, a 2.048MHz clock input frequency is selected. Digital ground selects 1.544MHz and $V_{BB}$ selects 1.536MHz.

## APPLICATIONS INFORMATION

### GAIN ADJUST

Figure 2 shows the signal path interconnections between the ETC5040/ETC5040A and single-channel CODEC. The transmit RC coupling components have been chosen both for minimum passband droop and to present the correct impedance to the CODEC during sampling.

Optimum noise and distortion performance will be obtained from the ETC5040/ETC5040A filter when operated with system peak overload voltages of ± 2.5V to ± 3.2V at $VF_XO$ and $VF_RO$. When interfacing to a PCM CODEC with a peak overload voltage outside this range, further gain or attenuation may be required.

For example, the ETC5040/ETC5040A filter can be used with CODEC which has a 5.5V peak overload voltage. A gain stage following the transmit filter output and an attenuation stage following the CODEC output are required.

BOARD LAYOUT

Care must be taken in PCB layout to minimize power supply and ground noise. Analog ground (GNDA) of each filter should be connected to digital ground (GNDD) at a single point, which should be bypassed to both power supplies.

Further power supply decoupling adjacent to each filter and CODEC is recommended. Ground loops should be avoided, both between the GNDA traces of adjacent filters and CODECs.