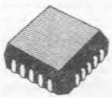
SGS-THOMSON MICROELECTRONICS

ETC5040FN/A

PCM RECEIVE/TRANSMIT FILTER

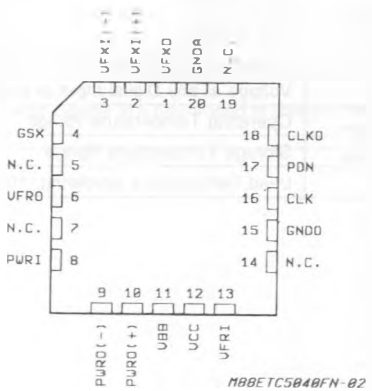
- EXCEEDS ALL D3/D4 AND CCITT SPECIFICATIONS
- + 5 V, – 5 V POWER SUPPLIES
- LOW POWER CONSUMPTION :
  45 mW (600 Ω - O dBm load)
  30 mW (power amps disabled)
- POWER DOWN MODE : 0.5mW
- 20 dB GAIN ADJUST RANGE
- NO EXTERNAL ANTI-ALIASING COMPONENTS
- SIN x/x CORRECTION IN RECEIVE FILTER
- 50/60 Hz REJECTION IN TRANSMIT FILTER
- TTL AND CMOS COMPATIBLE LOGIC
- ALL INPUTS PROTECTED AGAINST STATIC DISCHARGE DUE TO HANDLING



PLCC20

ORDER CODES : ETC5040FN
ETC5040FN/A

PIN CONNECTION



DESCRIPTION

The ETC5040FN ETC5040FN/A filter is a monolithic circuit containing both transmit and receive filters specifically designed for PCM CODEC filtering applications in 8 kHz sampled systems.

The filter is manufactured using double-poly silicon gate CMOS technology. Switched capacitor integrators are used to simulate classical LC ladder filters which exhibit low component sensitivity.

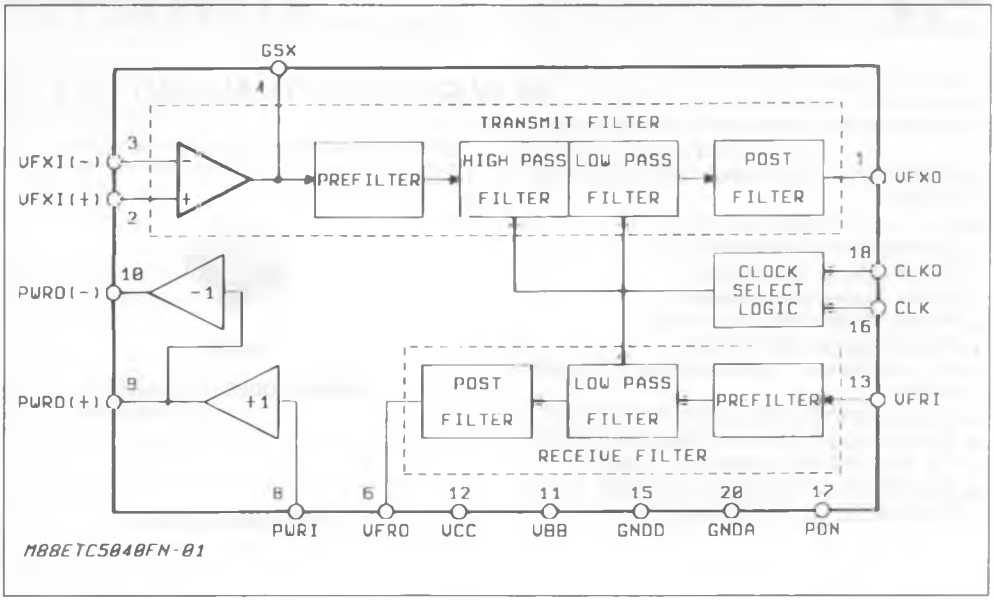
TRANSMIT FILTER STAGE

The transmit filter is fifth order elliptic low pass filter in series with a fourth order Chebychev high pass filter. It provides a flat response in the pass-band and rejection of signals below 200 Hz and above 3.4 kHz.

RECEIVE FILTER STAGE

The receive filter is a fifth order elliptic low pass filter designed to reconstruct the voice signal from the decoded/demultiplexed signal which, as a result of the sampling process, is a stair-step signal having the inherent sin x/x frequency response. The receive filter approximates the function required to compensate for the degraded frequency response and restore the flat pass-band response.

Figure 1 : Block Diagram.



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	V_{CC} to GNDA	7	V
V_{BB}	V_{BB} to GNDA	– 7	V
V_{IN}, V_{OUT}	Voltage at any Analog Input or Output	V_{CC} + 0.3 to V_{BB} – 0.3	V
	Voltage at any Digital Input or Output	V_{CC} + 0.3 to GNDA – 0.3	V
T_{oper}	Operating Temperature Range	– 25 to + 125	°C
T_{stg}	Storage Temperature Range	– 65 to + 150	°C
	Lead Temperature (soldering, 10 seconds)	300	°C

PIN DESCRIPTION

Name	Pin Type *	N°	Function	Description
VF_XO	O	1		The output of the transmit filter stage.
VF_XI+	I	2		The non-inverting input to the transmit filter stage.
VF_XI-	I	3		The inverting input to the transmit filter stage.
GS_X	O	4		The output used for gain adjustments of the transmit filter.
VF_RO	O	6		The low power receive filter output. This pin can directly drive the receive port of an electronic hybrid.
PWRI	I	8		The input to the receive filter differential power amplifier.
PWRO+	O	9		The non-inverting output of the receive filter power amplifier. This output can directly interface conventional transformer hybrids.
PWRO–	O	10		The inverting output of thr receive filter power amplifier. This output can be used with PWRO+ to differentially drive a transformer hybrid.
V_{BB}	S	11		The negative power supply pin. Recommended input is – 5 V.
V_{CC}	S	12		The positive power supply pin. The recommended input is 5 V.
VF_RI	I	13		The input pin for the receive filter stage.
GNDD	GND	15		Digital Ground Input Pin. All digital signals are referenced to this pin.
CLK	I	16		Master Input Clock. Input frequency can be selected as 2.048 MHz, 1.544 MHz or 1.536 MHz.
PDN	I	17		The input pin used to power down the ETC5040FN *, ETC5040FN/A during idle periods. Logic 1 (V_{CC}) input voltage causes a power down condition. An internal pull-up is provided.
CLKO	I	18		This input pin selects internal counters in accordance with the CLK input clock frequency : **CLK** **Connect CLKO to :** 2048 kHz V_{CC} 1544 kHz GNDD 1536 kHz V_{BB} An internal pull-up is provided.
GNDA	GND	20		Analog Ground Input Pin. All analog signals are referenced to this pin. Not internally connected to GNDD.

* I : Input, O : Output, S : Power supply.

ELECTRICAL OPERATING CHARACTERISTICS V_{CC} = 5.0 V ± 5 %, V_{BB} = – 5.0 V ± 5 %, GNDA = 0 V, T_A = 0 °C to 70 °C (unless otherwise noted) ; typical characteristics specified at T_A = 25 °C ; all signals are referenced to GNDA.

POWER DISSIPATION

Symbol	Parameter	Min.	Typ.	Max.	Unit
I_{CCO}	V_{CC} Standby Current (PDN = V_{DD}, power down mode)	–	50	100	µA
I_{BBO}	V_{BB} Standby Current (PDN = V_{DD}, power down mode)	– 100	– 50	–	µA
I_{CC1}	V_{CC} Operating Current (PWRI = V_{BB}, power amp inactive)	–	3.0	4.0	mA
I_{BB1}	V_{BB} Operating Current (PWRI = V_{BB}, power amp inactive)	– 4.0	– 3.0	–	mA
I_{CC2}	V_{CC} Operating Current (note 1)	–	4.6	6.4	mA
I_{BB2}	V_{BB} Operating Current (note 1)	– 6.4	– 4.6	–	mA

DIGITAL INTERFACE

Symbol	Parameter	Min.	Typ.	Max.	Unit
I_{INC}	Input Current, CLK (0 V ≤ V_{IN} ≤ V_{CC})	– 10	–	10	µA
I_{INP}	Input Current, PDN (0 V ≤ V_{IN} ≤ V_{CC}–2 V)	– 100	–	–	µA
I_{INO}	Input Current, CLKO (V_{BB} ≤ V_{IN} ≤ V_{CC}–2 V)	– 10	–	– 0.1	µA
V_{IL}	Input Low Voltage, CLK, PDN	0	–	0.8	V
V_{IH}	Input High Voltage, CLK, PDN	2.2	–	V_{CC}	V
V_{ILO}	Input Low Voltage, CLKO	V_{BB}	–	V_{BB}+0.5	V
V_{IIO}	Input Intermediate Voltage, CLKO	– 0.8	–	0.8	V
V_{IHO}	Input High Voltage, CLKO	V_{CC}–0.5	–	V_{CC}	V

TRANSMIT INPUT AMP. OP.

Symbol	Parameter	Min.	Typ.	Max.	Unit
$IB_X I$	Input Leakage Current, $VF_X I$ (V_{BB} ≤ $VF_X I$ ≤ V_{CC})	– 100	–	100	nA
$RI_X I$	Input Resistance $VF_X I$ (V_{BB} ≤ $VF_X I$ ≤ V_{CC})	10	–	–	MΩ
$VOS_X I$	Input Offset Voltage, $VF_X I$ (– 2.5 V ≤ V_{IN} ≤ + 2.5 V)	– 20	–	20	mV
V_{CM}	Common-mode Range, $VF_X I$	– 2.5	–	2.5	V
CMRR	Common-mode Rejection Ratio (– 2.5 V ≤ V_{IN} ≤ 2.5 V)	60	–	–	dB
PSRR	Power Supply Rejection of V_{CC} or V_{BB}	60	–	–	dB
R_{OL}	Open Loop Output Resistance GS_X	–	1	–	kΩ
R_L	Minimum Load Resistance, GS_X	10	–	–	kΩ
CL	Maximum Load Capacitance, GSX	–	–	100	pF
$VO_X I$	Output Voltage Swing, GS_X (R_L ≥ 10 kΩ)	± 2.5	–	–	V
A_{VOL}	Open Loop Voltage Gain, GS_X (R_l ≥ 10 kΩ)	5.000	–	–	V/V
F_C	Open Loop Unity Gain Bandwidth, GS_X	–	2	–	MHz

AC ELECTRICAL CHARACTERISTICS T_A = + 25 °C. All parameters are specified for a signal level of 0 dBm0 at 1 kHz. The 0 dBm0 level is assumed to be 1.54 Vrms measured at the output of the transmit or receive filter. (unless otherwise specified)

TRANSMIT FILTER (note 2)

Symbol	Parameter		Min.	Typ.	Max.	Unit
RL_X	Minimum Load Resistance					kΩ
	– 2.5 V < V_{out} < + 2.5 V		3	–	–	
	– 3.2 V < V_{out} < + 3.2 V		10	–	–	
CL_X	Load Capacitance, VF_XO		–	–	100	pF
	Output Resistance, VF_XO		–	1	3	Ω
PSRR1	V_{CC} Power Supply Rejection VF_XI (f = 1 kHz, VF_XI+ = 0 Vms)		30	–	–	dB
PSRR2	V_{BB} Power Supply Rejection, VF_XO (same as above)		35	–	–	dB
GA_X	Absolute Gain (f = 1 kHz)					dB
		ETC5040FN/A	2.9	3.0	3.1	
		ETC5040FN	2.875	3.0	3.125	
GR_X	Gain Relative to GA_X					dB
	Below 50 Hz		–	–	– 35	
	50 Hz		–	– 41	– 35	
	60 Hz		–	– 35	– 30	
	200 Hz	ETC5040FN/A	– 1.5	–	0	
		ETC5040FN	– 1.5	–	0.05	
	300 Hz to 3 kHz	ETC5040FN/A	– 0.125	–	0.125	
		ETC5040FN	– 0.15	–	0.15	
	3.3 kHz	ETC5040FN/A	– 0.35	–	0.03	
		ETC5040FN	– 0.35	–	0.125	
	3.4 kHz		– 0.70	–	– 0.1	
	4.0 kHz		–	– 15	– 14	
	4.6 kHz and Above		–	–	– 32	
DA_X	Absolute Delay at 1 kHz		–	–	230	µs
	Differential envelope Delay from 1 kHz to 2.6 kHz		–	–	60	µs
DP_X1	Single Frequency Distortion Products		–	–	– 48	dB
DP_X2	Distortion at Maximum Signal Level 1.6 Vrms, 1 kHz Signal Applied to VF_XI+, gain = 20 dB, R_L = 10 kΩ		–	–	– 45	dB
NC_X1	Total C Message Noise at VF_XO		–	2	5	dBrnco
NC_X2	Total C message Noise at VF_XO Gain Setting 0p Amp at 20 dB, non inverting, note. 3.0 °C ≤ T_A ≤ + 70 °C		–	3	6	dBrnco
GA_XT	Temperature Coefficient of 1 kHz Gain		–	0.0004	–	dB/°C
GA_XS	Supply Voltage Coefficient of 1 kHz Gain		–	0.01	–	dB/V
CT_{RX}	Crosstalk, receive to transmit 20 $\log \frac{VF_XO}{VF_RO}$					dB
	Receive Filter Output = 2.2 Vrms, VFX_XI+ = 0 Vrms, f = 0.2 kHz to 3.4 kHz, measure VF_XO		–	–	– 70	
GR_XL	Gaintracking Relative to GA_X					dB
	Output Level = + 3 dBm0		– 0.1	–	0.1	
	+ 2 dBm0 to – 40 dBm0		– 0.05	–	0.05	
	– 40 dBm0 to – 55 dBm0		– 0.1	–	0.1	

AC ELECTRICAL CHARACTERISTICS (continued)

RECEIVE FILTER (unless otherwise noted, the receive filter is preceeded by a sin X/X filter with an input signal level of 1.54 Vrms)

Symbol	Parameter	Min.	Typ.	Max.	Unit
IB_R	Input Leakage Current, VF_RI ($-3.2\ V \le V_{IN} \le 3.2\ V$)	– 100	–	100	nA
RI_R	Input Resistance, VF_RI	10	–	–	MΩ
RO_R	Output Resistance, VF_RO	–	1	3	Ω
CL_R	Load Capacitance, VF_RO	–	–	100	pF
RL_R	Load Resistance, VF_RO	10	–	–	kΩ
PSRR3	Power Supply Rejection of V_{CC} or V_{BB} (VF_RO, VF_RI Connected to GNDA, f = 1 kHz)	35	–	–	dB
VOS_RO	Output DC Offset, VF_RO (VF_RI connected to GNDA)	– 200	–	+ 200	mV
GA_R	Absolute Gain (f = 1 kHz)				dB
	ETC5040FN/A	– 0.1	0	0.1	
	ETC5040FN	– 0.125	0	0.125	
GR_R	Gain Relative to Gain at 1 kHz Below 300 Hz	–	–	0.125	dB
	300 Hz to 3.0 kHz ETC5040FN/A	– 0.125	–	0.125	
	ETC5040FN	– 0.15	–	0.15	
	3.3 kHz	– 0.35	–	0.03	
	3.4 kHz	– 0.70	–	– 0.1	
	4.0 kHz	–	–	– 14	
	4.6 kHz and Above	–	–	– 32	
DA_R	Absolute Delay at 1 kHz	–	–	100	µs
DD_R	Differential Envelope Delay 1 kHz to 2.6 kHz	–	–	100	µs
DP_R1	Single Frequency Distortion Products (f = 1 kHz)	–	–	– 48	dB
DP_R2	Distortion at Maximum Signal Level 2.2 Vrms Input to Sin X/X Filter, f = 1 kHz, R_L = 10 kΩ	–	–	– 45	dB
NC_R	Total C Message Noise at VF_RO	–	3	5	dBrnc0
GA_RT	Temperature Coefficient of 1 kHz Gain	–	0.0004	–	dB/°C
GA_RS	Supply Voltage Coefficient of 1 kHz Gain	–	0.01	–	dB/V
CT_{XR}	Crosstalk, transmit to receive 20 log $\frac{VF_RO}{VF_XO}$ (transmit filter output = 2.2 Vrms, VF_RI = 0 Vrms, f = 0.3 kHz to 3.4 kHz, measure VF_RO)	–	– 80	– 70	dB
GR_RL	Gaintracking Relative to GA_R				dB
	Output Level = 3 dBm0	– 0.1	–	0.1	
	+ 2 dBm0 to – 40 dBm0	– 0.05	–	0.05	
	– 40 dBm0 to 55 dBm0	– 0.1	–	0.1	

RECEIVE OUTPUT POWER AMPLIFIER

Symbol	Parameter	Min.	Typ.	Max.	Unit
IBP	Input Leakage Current, PWRI ($-3.2\ V \le V_{IN} \le 3.2\ V$)	0.1	–	3	µA
RIP	Input Resistance, PWRI	10	–	–	MΩ
ROP1	Output Resistance, PWRO+, PWRO– (amplifiers active)	–	1	3	Ω
CLP	Load Capacitance, PWRO+, PWRO–	–	–	500	pF

AC ELECTRICAL CHARACTERISTICS (continued)

RECEIVER OUTPUT POWER AMPLIFIER (continued)

Symbol	Parameter	Min.	Typ.	Max.	Unit
GAp+ GAp–	Gain, PWRI to PWRO+ (R_L = 600 Ω connected between) Gain, PWRI to PWRO– PWRO+ and PWRO– input, level = 0 dBm0 (note 4)	– –	1 – 1	– –	V/V V/V
GRpL	Gaintraking Relative to 0dBm0 Output Level V = 2.05 Vrms, R_L = 600 Ω (notes 4, 5) V = 1.75 Vrms, R_L = 300 Ω (notes 4, 5)	 – 0.1 – 0.1	 – –	 0.1 0.1	dB
S/Dp	Signal/distortion V = 2.05 Vrms, R_L = 600 Ω (notes 4, 5) V = 1.75 Vrms, R_L = 300 Ω (notes 4, 5)	 – –	 – –	 – 45 – 45	dB
VOSP	Output DC Offset, PWRO+, PWRO– (PWRI connected to GNDA)	– 50	–	50	mV
PSRR5	Power Supply Rejection of V_{CC} or V_{BB} (PWRI connected to GNDA)	45	–	–	dB

Notes : 1. Maximum power consumption depend on the load impedance connected to the power amplifier. The specification listed assumes 0 dBm is delivered to 600 Ω connected from PWRO + PWRO –.
2. Transmit filter input op amp set to the non-inverting unity gain mode, with VF_XI+ = 1.1 Vrms, unless otherwise noted.
3. The 0 dBm0 level for the filter is assumed to be 1.54 Vrms measured at the output of the XMT or RCV filter.
4. The 0 dBm0 level for the power amplifiers is load dependent. For R_L = 600 Ω to GNDA, the 0 dBm0 level is 1.43 Vrms measured at the amplifier output. For R_L = 300 Ω the dBm0 level is 1.22 Vrms.
5. VF_RO connected to PWRI, input signal applied to VF_RI.

TYPICAL PERFORMANCE CHARACTERISTICS

Figure 1 : Transmit Filter Stage.

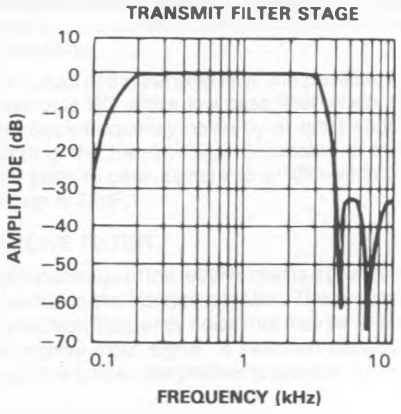


Figure 2 : Receive Filter Stage.

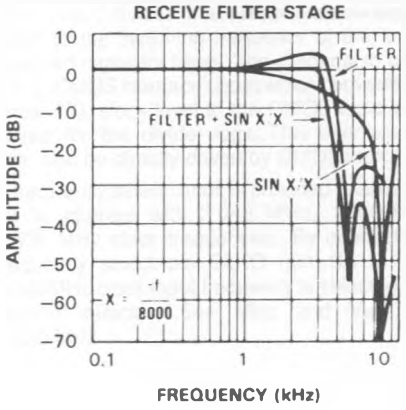
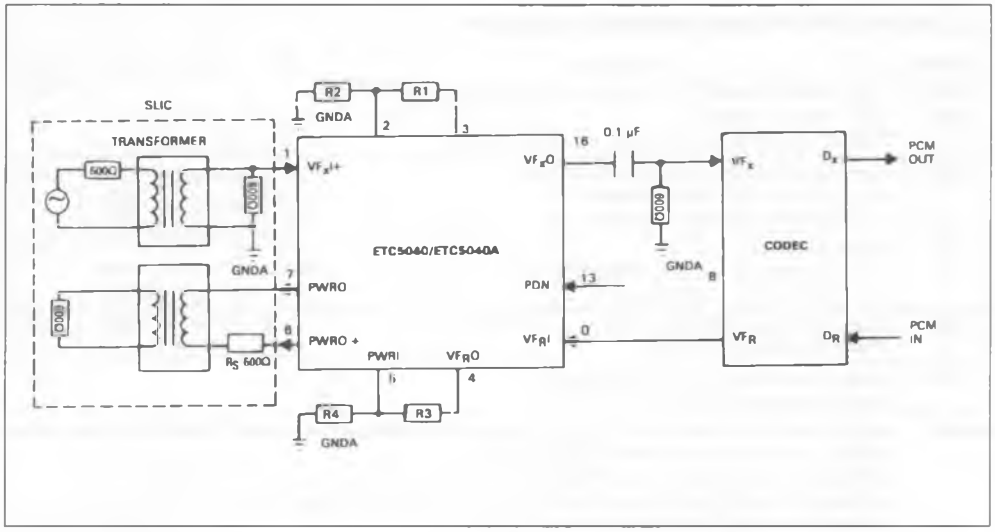


Figure 3 : Interface Circuit For CODEC.



Notes : 1. Transmit Voltage gain = $\frac{R1 + R2}{2}$ x √2 (the filter itself introduces a 3 dB gain) (R1 + R2 ≥ 10 kΩ)

2. Receive gain = $\frac{R4}{R3 + R4}$

(R3 + R4 ≥ 10 kΩ)

3. In the configuration shown, the receive filter power amplifiers will drive a 600 Ω T to R termination.

An alternative arrangement using a transformer winding ratio equivalent to 1.414.1 and 300 Ω resistor R level of 10 dBm across 600 Ω termination impedance.

FUNCTIONAL DESCRIPTION

The ETC5040FN-ETC5040FN/A monolithic filter contains four main sections ; Transmit Filter, Receive Filter, Receive Filter Power Amplifier, and Frequency Divider/Select Logic (figure 1). A brief description of the circuit operation for each section is provided below.

TRANSMIT FILTER

The input stage of the transmit filter is a CMOS operational amplifier which provides an input resistance greater than 10M, a voltage gain of greater than 5000, low power consumption (less than 3mW), high power supply rejection, and is capable of driving a 10k load parallel with up to 25pF. The inputs and output of the amplifier are accessible for added flexibility. Non-inverting mode, inverting mode, or differential amplifier mode operation can be implemented with external resistors. It can also be connected to provide a gain of up to 20dB without degrading the overall filter performance. The input stage is followed by a prefilter which is a two pole RC active low pass filter designed to attenuate high frequency noise before the input signal enters the switched-capacitor high pass and low pass filters.

A high pass filter is provided to reject 200Hz or lower noise which may exist in the signal path. The low pass portion of the switched-capacitor filter provides stopband attenuation which exceeds the D3 and D4 specifications as well as the CCITT G712 recommandations.

The output of the transmit filter, the postfilter, is also a two-pole RC active low pass filter which attenuates clock frequency noise by at least 40dB. The output of the transmit filter is capable of driving a 3.2V peak to peak signal into a 10kload in parallel with up to 25pF.

RECEIVE FILTER

The input stage of the receive filter is a prefilter which is similar to the transmit prefilter. The prefilter attenuates high frequency noise that may be present on the receive input signal. A switched capacitor low pass filter follows the prefilter to provide the necessary passband flatness, stopband rejection and sin x/x gain correction. A postfilter which is similar to the transmit postfilter follows the low pass stage. It attenuates clock frequency noise and provides a low output impedance capable of directly driving an electronic subscriber-line-interface circuit.

RECEIVE FILTER POWER AMPLIFIERS

Two power amplifiers are also provided to interface to transformer coupled line circuits. These two amplifiers are driven by the output of the receive postfilter through gain setting resistors, R3, R4 (figure 3). The power amplifiers can be deactivated, when not required, by connecting the power amplifier input (pin 5) to the negative power supply V_{BB}. This reduces the total filter power consumption by approximately 10mW to 20mW depending on output signal amplitude.

POWER DOWN CONTROL

A power down mode is also provided. A logic 1 power down command applied on the PDN pin (pin 17) will reduce the total filter power consumption to less than 1mW and turn the power amplifier outputs into high impedance state.

FREQUENCY DIVIDER AND SELECT LOGIC CIRCUIT

This circuit divides the external clock frequency down to the switching frequency of the low pass switched capacitor filters. The divider also contains a TTL-CMOS interface circuit which converts the external TTL clock level to the CMOS logic level required for the divider logic. This interface circuit can also be directly driven by CMOS logic.

A frequency select circuit is provided to allow the filter to operate with 2.048 MHz, 1544 MHz or 1.536 MHz clock frequencies. By connecting the frequency select pin CLKO (pin 18) to V_{CC}, a 2.048MHz clock input frequency is selected. Digital ground selects 1.544 MHz and V_{BB} selects 1.536 MHz.

APPLICATIONS INFORMATION

GAIN ADJUST

Figure 3 shows the signal path interconnections between the ETC5040FN-ETC5040FN/A and single-channel CODEC. The transmit RC coupling components have been chosen both for minimum passband droop and to present the correct impedance to the CODEC during sampling.

Optimum noise and distortion performance will be obtained from the ETC5040FN-ETC5040FN/A filter when operated with system peak overload voltages of 2.5 V to 3.2 V at VF_XO and VF_RO. When interfacing to a PCM CODEC with a peak overload voltage outside this range, further gain or attenuation may be required.

For example, the ETC5040FN-ETC5040FN/A filter can be used with CODEC which has a 5.5 V peak overload voltage. A gain stage following the transmit filter output and an attenuation stage following the CODEC output are required.

BOARD LAYOUT

Care must be taken in PCB layout to minimize power supply and ground noise. Analog ground (GNDA) of each filter shoult be connected to digital ground (GNDD) at a single point, which should be bypassed to both power supplies.

Further power supply decoupling adjacent to each filter and CODEC is recommended. Ground loops should be avoided, both between the GNDA traces of adjacent filters and CODECs.