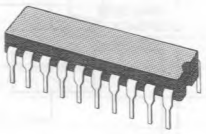
SGS-THOMSON MICROELECTRONICS

ETC5056

PARALLEL DATA INTERFACE CODEC/FILTER

- COMPLETE CODEC AND FILTERING SYSTEM INCLUDING :
  - TRANSMIT HIGH PASS AND LOW PASS FILTERING
  - RECEIVE LOW PASS FILTER WITH SIN x/x CORRECTION
  - RECEIVE POWER AMPLIFIER
  - ACTIVE RC NOISE FILTERS
  - A-LAW COder AND DECoder
  - INTERNAL PRECISION VOLTAGE REFERENCE
  - INTERNAL AUTO-ZERO CIRCUITRY
- MEETS OR EXCEEDS ALL D3/D4 AND CCITT SPECIFICATIONS
- ± 5 V OPERATION
- LOW OPERATING POWER - TYPICALLY 60mW
- POWER DOWN STANDBY MODE - TYPICALLY 3 mW
- HIGH SPEED TRI-STATE ® DATA BUS.
- 2 LOOPBACK TEST MODES
- SECOND SOURCE OF TP3056

The ETC5056 is especially designed to be used with a line interface controller providing local time and space switching in a distributed control switching system.



DIP20
(Ceramic)

ORDER CODES : ETC5056J

DESCRIPTION

The ETC5056 family is a A-law monolithic PCM CODEC/filters utilizing the A/D and D/A conversion architecture shown in figure 1, parallel I/O data bus interface. The device is fabricated using double-poly CMOS process.

The encode portion consists of an input gain adjust amplifier, an active RC pre-filter which eliminates very high frequency noise prior to entering a switched-capacitor band-pass filter that rejects signals below 200 Hz and above 3400 Hz. Also-included are auto-zero circuitry and a companding coder which samples the filtered signal and encodes it in the companded A-law PCM format..

The decode portion consists of an expanding decoder, which reconstructs the analog signal from the companded A-law code, a low-pass filter which corrects for the sin x/x response of the decoder output and rejects signals above 3400 Hz and is followed by a single-ended power amplifier capable of driving low impedance loads.

PIN CONNECTION

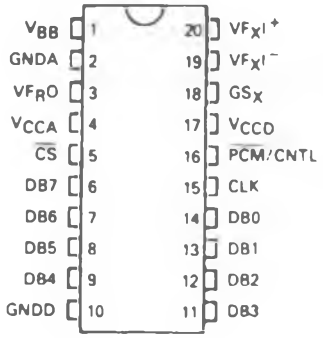
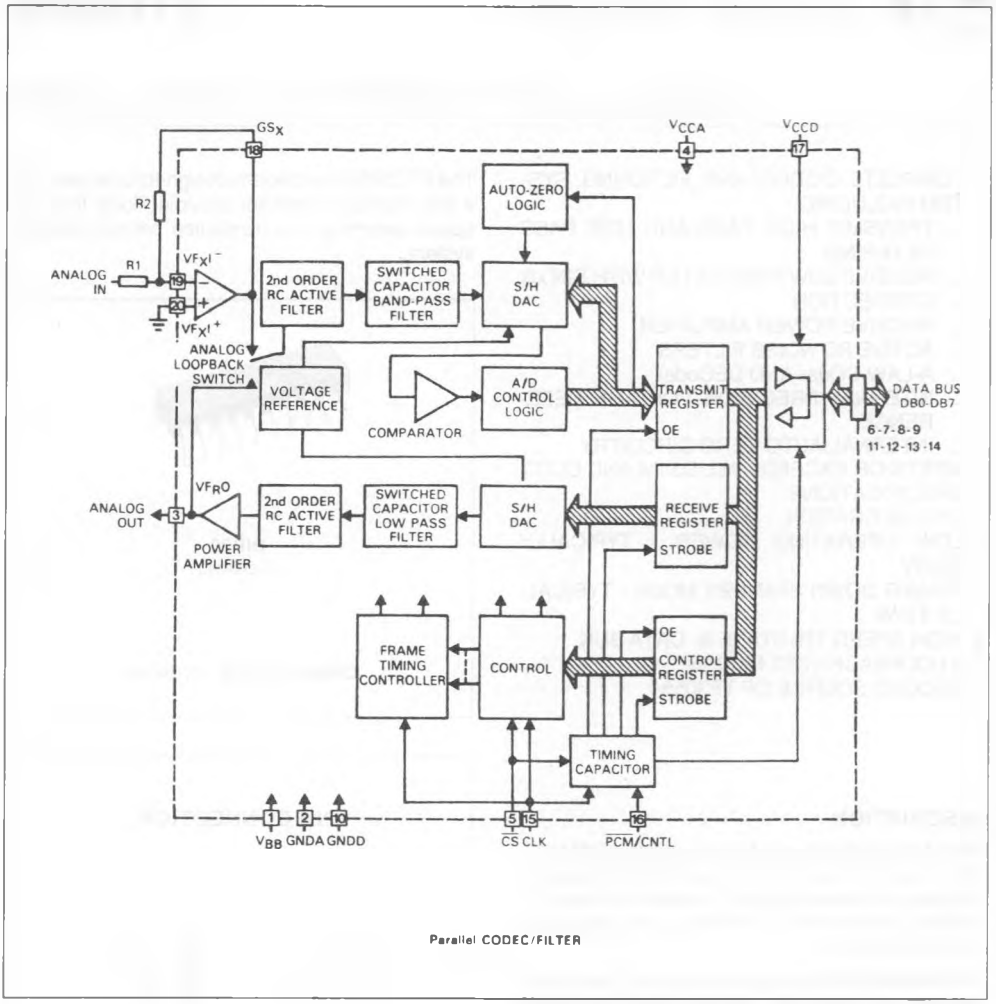


Figure 1 : Block Diagram.



Parallel CODEC/FILTER

PIN DESCRIPTION

Name	Pin Type*	N	Description
V_{BB}	S	1	Negative power supply pin. $V_{BB} = -5$ V ± 5 %
GNDA	GND	2	Analog ground. All analog signals are referenced to this pin.
VF_RO	0	3	Analog output of the receive power amplifier. This output can drive a 600 Ω load to ± 2.5 V.
V_{CCA}	S	4	Positive power supply voltage pin for the analog circuitry. $V_{CCA} = 5$ V ± 5 %. Must be connected to V_{CCD}.
$\overline{CS}$	I	5	Device chip select input which controls READ write and TRI-STATE® operations on the data bus. $\overline{CS}$ does not control the state of any analog functions.
DB7	I/O	6	Bit 7 I/O on the data bus. The PCM LSB.
DB6	I/O	7	Bit 6 I/O on the data bus.
DB5	I/O	8	Bit 5 I/O on the data bus.
DB4	I/O	9	Bit 4 I/O on the data bus.
GNDD	GND	10	Digital ground. All digital signals are referenced to this pin.
DB3	I/O	11	Bit 3 I/O on the data bus.
DB2	I/O	12	Bit 2 I/O on the data bus.
DB1	I/O	13	Bit 1 I/O on the data bus.
DB0	I/O	14	Bit 0 I/O on the data bus. This is the PCM sign bit.
CLK	I	15	The clock input for switched-capacitor filter and CODEC. Clock frequency must be 768 kHz, 772 kHz, 1.024 MHz or 1.28 MHz and must be synchronous with the system clock input.
$\overline{PCM}/CNTL$	I	16	This control input determines whether the information on the data bus is PCM data or control data.
V_{CCD}	S	17	Positive power supply pin for the bus drivers. $V_{CCD} = 5$ V ± 5 %. Must be connected to V_{CCA}.
GS_X	O	18	Analog output of the transmit input amplifier. Used to externally set gain.
VF_XI^-	I	19	Inverting input of the transmit input amplifier.
VF_XI^+	I	20	Non-inverting input of the transmit input amplifier.

* I : Input, O : Output, S : Power Supply.

FUNCTIONAL DESCRIPTION

CLOCK AND DATA BUS CONTROL

The CLK input signal provides timing for the encode and decode logic and the switched-capacitor filters. It must be one of the frequencies listed in Table 1 and must be correctly selected by control bits C0 and C1.

CLK also functions as a READ/$\overline{\text{WRITE}}$ control signal, with the device reading the data bus on a positive half-clock cycle and writing the bus on a negative half-clock cycle, as shown in figure 4.

POWER-UP

When power is first applied, power-on reset circuitry initializes the CODEC/filter and sets it in the power-down mode. All non-essential circuits are deactivated and the data bus outputs, DB0-DB7, and receive power amplifier output, VF_RO, are in high impedance states.

The ETC5056 is powered-up via a command to the control register (see Control Register Functions). This sets the device in the standby mode with all circuitry activated, but encoding and decoding do not begin until PCM READ and PCM WRITE chip selects occur.

Table 1 : Control Bit Functions.

Control Bits	Function		
C0, C1	Select Clock Frequency		
	C0	**C1**	**Frequency**
	0	X	1.024 MHz
	1	0	0.768 MHz or 0.772 MHz
	1	1	1.28 MHz
C2, C3	Digital and Analog Loopback		
	C2	**C3**	**Mode**
	1	X	Digital Loopback
	0	1	Analog Loopback
	0	0	Normal
C4	Power-down/power-up		
	1 = Power-down 0 = Power-up		
C5	ETC5056 0 = A-law without Even Bit Inversion 1 = A-law with Even Bit Inversion		
C6, C7	Don't Care		

DATA BUS ASSIGNEMENT

The parallel I/O data bus is defined as follows :

Data Type	DB0	DB7
PCM	Sign Bit	LSB
Control Data	C0	C7

READING THE BUS

If CLK is low when $\overline{\text{CS}}$ goes low, bus data is gated in during the next positive half-clock cycle of CLK and latched on the negative-going transition. If PCM/CNTL is low during the falling $\overline{\text{CS}}$ transition, then the bus data is defined as PCM voice data, which is latched into the receive register. This also functions as an internal receive frame synchronization pulse to start a decode cycle and must occur once per receive frame ; i.e., at an 8 KHz rate.

If PCM/CNTL is high during the falling $\overline{\text{CS}}$ transition, the bus data is latched into the control register. This does not effect frame synchronization.

WRITING THE BUS

If CLK is high when $\overline{\text{CS}}$ goes low, at the next falling transition of CLK, the bus drivers are enabled and either the PCM transmit data or the contents of the control register are gated into the bus, depending on the level of PCM/CNTL at the $\overline{\text{CS}}$ transition. If PCM/CNTL is low during the $\overline{\text{CS}}$ falling transition, the transmit register data is written to the bus. An internal transmit frame synchronization pulse is also generated to start an encode cycle, and this must occur once per transmit frame ; i.e., at an 8 KHz rate.

If PCM/CNTL is high during the $\overline{\text{CS}}$ falling transition, the control register data is written to the bus. This does not affect frame synchronization.

The receive register contents may also be written back to the bus, as described in the Digital Loopback section.

Except during a WRITE cycle, the bus drivers are in TRI-STATE mode.

CONTROL REGISTER FUNCTIONS

Writing to the control register allows the user to set the various operating states of the ETC5056. The control register can also be read back via the data bus to verify the current operating mode of the device.

1. CLK Select.
   Since one of three distinct clock frequencies may be used, the actual frequency must be known by

the device for proper operation of the switched-capacitor filters. This is achieved by writting control register bits C0 and C1, normally in the same WRITE cycle that powers-up the device, and before any PCM data transfers take place.

2. Digital Loopback.
   In order to establish that a valid path has been selected through a network, it is sometimes desirable to be able to send data through the network to its destination, then loop it back through the network return path to the originating source where the data can be verified. This loopback function can be performed in ETC5056 by setting control register bit C2 to 1. With C2 set, the PCM data in the receive register will be written back into the data bus during the next PCM WRITE cycle. In the digital loopback mode, the receive section is set to an idle channel condition in order to maintain a low impedance termination at VF_RO.
3. Analog Loopback.
   In the analog loopback mode, the transmit filter input is switched from the gain adjust amplifier to the receive power amplifier output, forming a unity-gain loop from the receive register back to the transmit register. This mode is enterred by setting control register bits C2 to 0 and C3 to 1. The receive power amplifier continues to drive the load in this mode.
4. Power-Down/Power-Up.
   The ETC5056 may be put in the power-down mode by setting control register bit C4 to 1. Conversely, setting bit C4 to 0 power up the device.

TRANSMIT FILTER AND ENCODE SECTION

The transmit section input is an operational amplifier with provision for gain adjustment using two external resistors, see figure 2. The low noise and wide bandwidth allow gains in excess of 20 dB across the audio passband to be realized. The op amp drives a unity-gain filter consisting of a 2 nd order RC active pre-filter, followed by an 8 th order switched-capacitor bandpass filter clocked at 256 KHz.

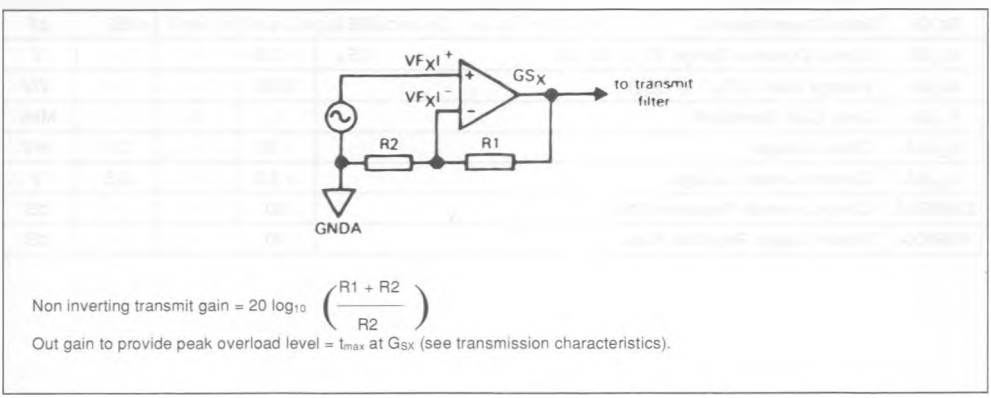
The output of this filter directly drives the encoder sample-and-hold circuit. The A/D is of companding type according to A-law (ETC5056) coding schemes. A precision voltage reference is trimmed in manufacturing to provide an input overload (t_{max}) of nominally 2.5 V peak (see table of Transmission Characteristics). Any offset voltage due to the filters or comparator is cancelled by sign bit integration in the auto-zero circuit.

The total encoding delay referenced to a PCM WRITE chip select will be approximately 165 µs (due to the transmit filter) plus 125 µs (due to endoding delay), which totals 290 µs.

DECODER AND RECEIVE FILTER SECTION

The receive section consists of an expanding DAC which drives a 5 th order switched-capacitor low pass filter clocked at 256 KHz. The decoder is of A-law (ETC5056) coding law and the 5 th order low pass filter corrects for the sin x/x attenuation due to the 8 KHz sample/hold. The filter is then followed by a 2 nd order RC active post-filter. The power amplifier output stage is capable of driving a 600 Ω load to a level of 7.2 dBm. The receive section has unity-gain. Following a PCM READ chip select, the decoding cycle begins, and 10 µs later the decoder DAC output is updated. The total decoder delay is – 10 µs (decoder update) plus 110 µs (filter delay) plus 62.5 µs (1/2 frame), which gives approximately 180 µs.

Figure 2 : Transmit Gain Adjustement.



$$\text{Non inverting transmit gain} = 20 \log_{10} \left(\frac{R1 + R2}{R2} \right)$$

Out gain to provide peak overload level = t_{max} at G_{SX} (see transmission characteristics).

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
	GNDD to GNDA	± 0.3	V
V_{CC}	V_{CCA} or V_{CCD} to GNDD or GNDA	± 7.0	V
V_{IN}, V_{OUT}	Voltage at Any Input or Output	V_{CC} + 0.3 to V_{BB} – 0.3	V
	Voltage at Any Digital Input or Output	V_{CC} + 0.3 to GNDD – 0.3	V
T_{oper}	Operating Temperature Range	– 25 to + 125	°C
T_{stg}	Storage Temperature Range	– 60 to + 150	°C
	Lead Temperature (soldering, 10 seconds)	300	°C

ELECTRICAL OPERATING CHARACTERSITICS

V_{CC} = 5.0 V ± 5 %, V_{BB} = – 5 V ± 5 %, GNDA = 0 V, T_A = 0 °C to 70 °C (unless otherwise noted) ; Typical characteristics specified at V_{CC} = 5.0 V, V_{BB} = – 5.0 V, T_A = 25 °C, all signals are referenced to GNDA.

DIGITAL INTERFACE

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{IL}	Input Low Voltage	–	–	0.6	V
V_{IH}	Input High Voltage	2.2	–	–	V
V_{OL}	Output Low Voltage IL = 2.5 mA, DB0-DB7	–	–	0.4	V
V_{OH}	Output High Voltage IH = – 2.5 mA, DB0-DB7	2.4	–	–	V
I_{IL}	Input Low Current (GNDA ≤ V_{IN} ≤ V_{IL}, all digital inputs)	– 10	–	10	µA
I_{IH}	Input High Current (V_{IH} ≤ V_{IN} ≤ V_{CC})	– 10	–	10	µA
I_{OZ}	Output Current in High impedance State (TRI-STATE) (GNDD ≤ V_O ≤ V_{CC}), DB0-DB7	– 10	–	10	µA

ANALOG INTERFACE WITH TRANSMIT INPUT AMPLIFIER (all devices)

Symbol	Parameter	Min.	Typ.	Max.	Unit
I_IXA	Input Leakage Current (– 2.5 V ≤ V ≤ + 2.5 V) VF_XI^+ or VF_XI^-	– 200	–	200	nA
R_IXA	Input Resistance (– 2.5 V ≤ V ≤ + 2.5 V) VF_XI^+ or VF_XI^-	10	–	–	MΩ
R_OXA	Output Resistance (closed loop, unity gain)	–	1	3	Ω
R_LXA	Load Resistance GS_X	10	–	–	kΩ
C_LXA	Load Capacitance GS_X	–	–	50	pF
V_OXA	Output Dynamic Range (R_L ≥ 10 kΩ) GS_X	± 2.8	–	–	V
A_VXA	Voltage Gain (VF_XI^+ to GS_X)	5000	–	–	V/V
F_UXA	Unity Gain Bandwidth	1	2	–	MHz
$V_{OS}XA$	Offset Voltage	– 20	–	20	mV
$V_{CM}XA$	Common-mode Voltage	– 2.5	–	2.5	V
CMRRXA	Common-mode Rejection Ratio	60	–	–	dB
PSRRXA	Power Supply Rejection Ratio	60	–	–	dB

ELECTRICAL OPERATING CHARACTERSITICS (continued)

ANALOG INTERFACE WITH RECEIVE FILTER (all devices)

Symbol	Parameter	Min.	Typ.	Max.	Unit
R_ORF	Output Resistance VF_RO	–	1	3	Ω
R_LRF	Load Resistance (VF_RO = ± 2.5 V)	600	–	–	Ω
C_LRF	Load Capacitance	–	–	500	pF
VOS_RO	Output DC Offset Voltage	– 200	–	200	mV

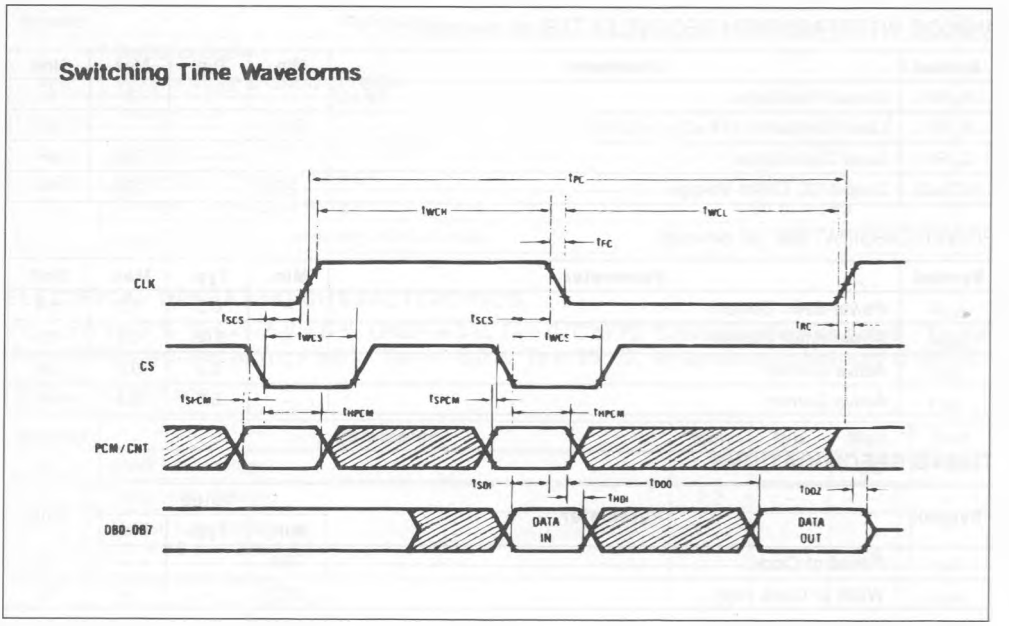
POWER DISSIPATION (all devices)

Symbol	Parameter	Min.	Typ.	Max.	Unit
$I_{CC}0$	Power-down Current	–	0.5	1.5	mA
$I_{BB}0$	Power-down Current	–	0.05	0.3	mA
$I_{CC}1$	Active Current	–	6.0	9.0	mA
$I_{BB}1$	Active Current	–	6.0	9.0	mA

TIMING SPECIFICATIONS

Symbol	Parameter	Value			Unit
		Min.	Typ.	Max.	
t_{PC}	Period of Clock	760	–	–	ns
t_{WCH}	Width of Clock High	330	–	–	ns
t_{WCL}	Width of Clock Low	330	–	–	ns
t_{RC}	Rise Time of Clock	–	–	50	ns
t_{FC}	Fall Time of Clock	–	–	50	ns
t_{SCS}	Set-up Time of CLK High or Low	100	–	–	ns
t_{HCS}	Hold Time from $\overline{CS}$ Low to CLK	100	–	–	ns
t_{WCS}	Width of Chip Select	100	–	–	ns
t_{SPCM}	Set-up Time of PCM/$\overline{CNTL}$	0	–	–	ns
t_{HPCM}	Hold Time of PCM/$\overline{CNTL}$	100	–	–	ns
t_{SDI}	Set-up Time of Data in	50	–	–	ns
t_{HDI}	Hold Time of Data in	20	–	–	ns
t_{DDO}	Delay Time of Data Out Valid (C_L = 0 pF to 200 pF)	90	–	260	ns
t_{DDZ}	Delay Time to Data Output Disabled (C_L = 0 pF to 200 pF)	20	–	80	ns

Figure 4 : Timing Waveforms for ETC5056.



TRANSMISSION CHARACTERSITICS

(all devices) T_A = 0 °C to 70 °C, V_{CC} = 5 V ± 5 %, V_{BB} = − 5 V ± 5 %, GNDA = 0 v, f = 1.02 kHz, V_{IN} = 0 dBm0 transmit input amplifier connected for unity-gain non-inverting (unless otherwise specified).

AMPLITUDE RESPONSE

Symbol	Parameter	Min.	Typ.	Max.	Unit
	Absolute Levels – Nominal 0 dBm0 level is 4 dBm (600 Ω). 0 dBm0 ETC5056	–	1.2276	–	V_{rms}
t_{MAX}	Max Overload Level 3.17 dBm0	–	2.501	–	V_{PK}
G_{XA}	Transmit Gain, Absolute (T_A = 25 °C, V_{CC} = 5 V, V_{BB} = − 5 V) Input at GS_X = 0 dBm0 at 1020 Hz	− 0.15	–	0.15	dB
G_{XR}	Transmit Gain, Relative to G_{XA}				dB
	f = 16 Hz	–	–	− 40	
	f = 50 Hz	–	–	− 30	
	f = 60 Hz	–	–	− 26	
	f = 180 Hz	− 2.8	–	− 0.2	
	f = 200 Hz	− 1.8	–	− 0.1	
	f = 300 Hz − 3000 Hz	− 0.15	–	− 0.15	
	f = 3300 Hz	− 0.35	–	+ 0.05	
	f = 3400 Hz	− 0.7	–	0	
	f = 4000 Hz	–	–	− 14	
	f = 4600 Hz and up, measure response from O Hz to 4000 Hz	–	–	− 32	
G_{XAT}	Absolute Transmit Gain Variation with Temperature (T_A = 0 °C to + 80 °C)	− 0.1	–	+ 0.1	dB
G_{XAV}	Absolute Transmit Gain Variation with Supply Voltage (V_{CC} = 5 V ± 5 %, V_{BB} = − 5 V ± 5 %)	− 0.05	–	+ 0.05	dB
G_{XRL}	Transmit Gain Variations with Level Sinusoidal Test Method Reference Level = − 10 dBm0				dB
	VF_XI^+ = − 40 dBm0 to + 3 dBm0	− 0.2	–	0.2	
	VF_XI^+ = − 50 dBm0 to − 40 dBm0	− 0.4	–	0.4	
	VF_XI^+ = − 55 dBm0 to − 50 dBm0	− 1.2	–	1.2	
G_{RA}	Receive Gain, Absolute (T_A = 25 °C, V_{CC} = 5 V, V_{BB} = − 5 V) Input = Digital Code Sequence for 0 dBm0 Signal at 1020 Hz	− 0.15	–	0.15	dB
G_{RR}	Receive Gain, Relative to G_{RA}				dB
	f= 0 Hz to 3000 Hz	− 0.15	–	0.15	
	f = 3300 Hz	− 0.35	–	0.05	
	f = 3400 Hz	− 0.7	–	0	
	f = 4000 Hz	–	–	− 14	
G_{RAT}	Absolute Receive Gain Variation with Temperature (T_A = 0 °C to + 70 °C)	− 0.1	–	+ 0.1	dB
G_{RAV}	Absolute Receive Gain Variation with Supply Voltage (V_{CC} = 5 V ± 5 %, V_{BB} = − 5 V ± 5 %)	− 0.05	–	+ 0.05	dB
G_{RRL}	Receive Gain Variations with Level Sinusoidal Test Method ; Reference input PCM code corresponds to an ideally encoded − 10 dBm0 signal				dB
	PCM level = − 40 dBm0 to + 3 dBm0	− 0.2	–	0.2	
	PCM level = − 50 dBm0 to − 40 dBm0	− 0.4	–	0.4	
	PCM level = − 55 dBm0 to − 50 dBm0	− 1.2	–	1.2	
V_{RO}	Receive Output Drive Level (R_L = 600 kΩ)	− 2.5	–	2.5	V

TRANSMISSION CHARACTERSITICS (continued)

ENVELOPE DELAY DISTORTION WITH FREQUENCY

Symbol	Parameter	Min.	Typ.	Max.	Unit
D_{XA}	Transmit Delay, Absolute (f = 1600 Hz)	–	290	315	µs
D_{XR}	Transmit Delay, Relative to D_{XA}				µs
	f = 500 Hz – 600 Hz	–	195	220	
	f = 600 Hz – 800 Hz	–	120	145	
	f = 800 Hz – 1000 Hz	–	50	75	
	f = 1000 Hz – 1600 Hz	–	20	40	
	f = 1600 Hz – 2600 Hz	–	55	75	
	f = 2600 Hz – 2800 Hz	–	80	105	
	f = 2800 Hz – 3000 Hz	–	130	155	
D_{RA}	Receive Delay, Absolute (f = 1600 Hz)	–	180	200	µs
D_{RR}	Receive Delay, Relative to D_{RA}				µs
	f = 500 Hz – 1000 Hz	– 40	– 25	–	
	f = 1000 Hz – 1600 Hz	– 30	– 20	–	
	f = 1600 Hz – 2600 Hz	–	70	90	
	f = 2600 Hz – 2800 Hz	–	100	125	
	f = 2800 Hz – 3000 Hz	–	145	175	

NOISE

Symbol	Parameter	Min.	Typ.	Max.	Unit
N_{XP}	Transmit Noise, P Message Weighted ($VF_XI^+ = 0$ V)	–	– 74	– 69 (note 1)	dBM0p
N_{RP}	Receive Noise, P Message Weighted (PCM Code Equals Positive Zero)	–	– 82	– 79	dBm0p
N_{RS}	Noise, Single Frequency f = 0 kHz to 100 kHz, Loop Around Measurement, $VF_XI^+ = 0$ Vrms	–	–	– 53	dBm0
$PPSR_X$	Positive Power Supply Rejection, Transmit $VF_XI^+ = 0$ Vrms, V_{CC} = 5.0 V_{DC} + 100 mVrms, f = 0 kHz – 50 kHz	40	–	–	dBp
$NPSR_X$	Negative Power Supply Rejection, Transmit $VF_XI^+ = 0$ Vrms, V_{BB} = – 0.5 V_{DC} + 100 mVrms, f = 0 kHz – 50 kHz	40	–	–	dBp
$PPSR_R$	Positive Power Supply Rejection, Receive (PCM code equals positive zero, V_{CC} = 5.0 V_{DC} + 100 mVrms)				
	f = 0 Hz – 4000 Hz	40	–	–	dBp
	f = 4 kHz – 25 kHz	40	–	–	dB
	f = 25 kHz – 50 KHZ	36	–	–	dB
$NPSR_R$	Negative Power Supply Rejection, Receive (PCM code equals positive zero, V_{BB} = – 5.0 V_{DC} + 100 mVrms)				
	f = 0 Hz – 4000 Hz	40	–	–	dBp
	f = 4 kHz – 25 kHz	40	–	–	dB
	f = 25 kHz – 50 kHz	36	–	–	dB

TRANSMISSION CHARACTERISTICS (continued)

Symbol	Parameter	Min.	Typ.	Max.	Unit
SOS	Spurious out-of band signals at the channel output. Loop around measurement, 0 dBm0, 300 Hz – 3400 Hz input applied to VF_XI *, measure individual image signals at VF_RO				dB
	4600 Hz – 7600 Hz	–	–	– 32	
	7600 Hz – 8400 Hz	–	–	– 40	
	8400 Hz – 100,000 Hz	–	–	– 30	

DISTORTION

Symbol	Parameter		Min.	Typ.	Max.	Unit
STD_X or STD_R	Signal to Total Distortion (sinusoidal test method)					dBp
	Transmit or Receive Half-channel					
	Level = 3 dBm0		33	–	–	
	= 0 dBm0 to – 30 dBm0		36	–	–	
	= – 40 dBm0	XMT	29	–	–	
		RCV	30	–	–	
	= – 55 dBm0	XMT	14	–	–	
		RCV	15	–	–	
SFD_X	Single Frequency Distortion, Transmit		–	–	– 46	dB
SFD_R	Single Frequency Distortion, Receive		–	–	– 46	dB
IMD	Intermodulation Distortion Loop Around Measurement, VF_XI * = – 4 dBm0 to – 21 dBm0, Two Frequencies in the Range 300 Hz – 3400 Hz		–	–	– 41	dB

CROSSTALK

Symbol	Parameter	Min.	Typ.	Max.	Unit
CT_{X-R}	Transmit to Receive Crosstalk, 0 dBm0 Transmit Level f = 300 Hz – 3400 Hz, D_R = Steady PCM Mode	–	– 90	– 75	dB
CT_{R-X}	Receive to Transmit Crosstalk, 0 dBm0 Receive Level f = 300 Hz – 3400 Hz, VF_XI = 0 V	–	– 90	– 70 (note 2)	dB

Notes : 1. Measured by extrapolation of the S/N ratio result in the first segment of the encoder.
2. CT_{R-X} is measured with a – 40 dBm0 activating signal applied at VF_XI*.

ENCODING FORMAT AT DATA BUS OUTPUT

	TRUE A–Law, C5 = 0 (includes even bit inversion)							
	MSB							LSB
V_{IN} = + Full-scale	1	0	1	0	1	0	1	0
V_{IN} = 0 V	1	1	0	1	0	1	0	1
	0	1	0	1	0	1	0	1
V_{IN} = – Full-scale	0	0	1	0	1	0	1	0
	SIGN + MAGNITUDE A–LAW, C_5 = 1 (before even bit inversion)							
V_{IN} = + Full-scale	1	1	1	1	1	1	1	1
V_{IN} = 0 V	1	0	0	0	0	0	0	0
	0	0	0	0	0	0	0	0
V_{IN} = – Full-scale	0	1	1	1	1	1	1	1