ETC5054FN
ETC5057FN

SERIAL INTERFACE CODEC/FILTER

- COMPLETE CODEC AND FILTERING SYSTEM (combo) INCLUDING :
  - Transmit high-pass and low-pass filtering.
  - Receive low-pass filter with sin x/x correction.
  - Active RC noise filters.
  - μ-law or A-law compatible COder and DECoder.
  - Internal precision voltage reference.
  - Serial I/O interface.
  - Internal auto-zero circuitry.
- A-LAW 20 PINS ETC5057FN
- μ-LAW WITHOUT SIGNALING, 20 PINS ETC5054FN
- MEETS OR EXCEEDS ALL D3/D4 AND CCITT SPECIFICATIONS
- 5 V OPERATION
- LOW OPERATING POWER - TYPICALLY 60 mW
- POWER-DOWN STANDBY MODE - TYPICALLY 3 mW
- AUTOMATIC POWER-DOWN
- TTL OR CMOS COMPATIBLE DIGITAL INTERFACES
- MAXIMIZES LINE INTERFACE CARD CIRCUIT DENSITY
- SECOND SOURCE OF TP3057FN, TP3054FN

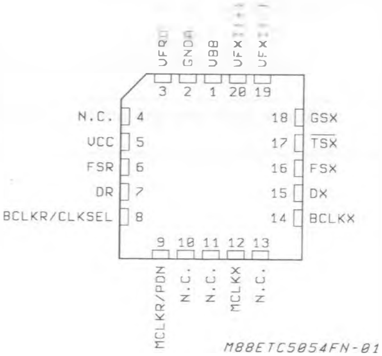
DESCRIPTION

The ETC5057/ETC5054 family consists of A-law and μ–law monolithic PCM CODEC/filters utilizing the A/D and D/A conversion architecture shown in the block diagram below, and a serial PCM interface. The devices are fabricated using double-poly CMOS process. The encode portion of each device consists of an input gain adjust amplifier, an active RC pre-filter which eliminates very high frequency noise prior to entering a switched-capacitor bandpass filter that rejects signals below 200 Hz and above 3400 Hz. Also included are auto-zero circuitry and a companding coder which samples the filtered signal and encodes it in the companded A-law or μ–law PCM format. The decode portion of each device consists of an expanding decoder, which reconstructs the analog signal from the companded A-law or μ–law code, a low-pass filter which corrects for the sin x/x response of the decoder output and rejects signals above 3400 Hz and is followed by a single-ended power amplifier capable of driving low impedance loads. The devices require 1.536 MHz, 1.544 MHz, or 2.048 MHz transmit and receive master clocks, which may be asynchronous, transmit and receive bit clocks which may vary from 64 kHz to 2.048 MHz, and transmit and receive frame sync pulses. The timing of the frame sync pulses and PCM data is compatible with both industry standard formats.

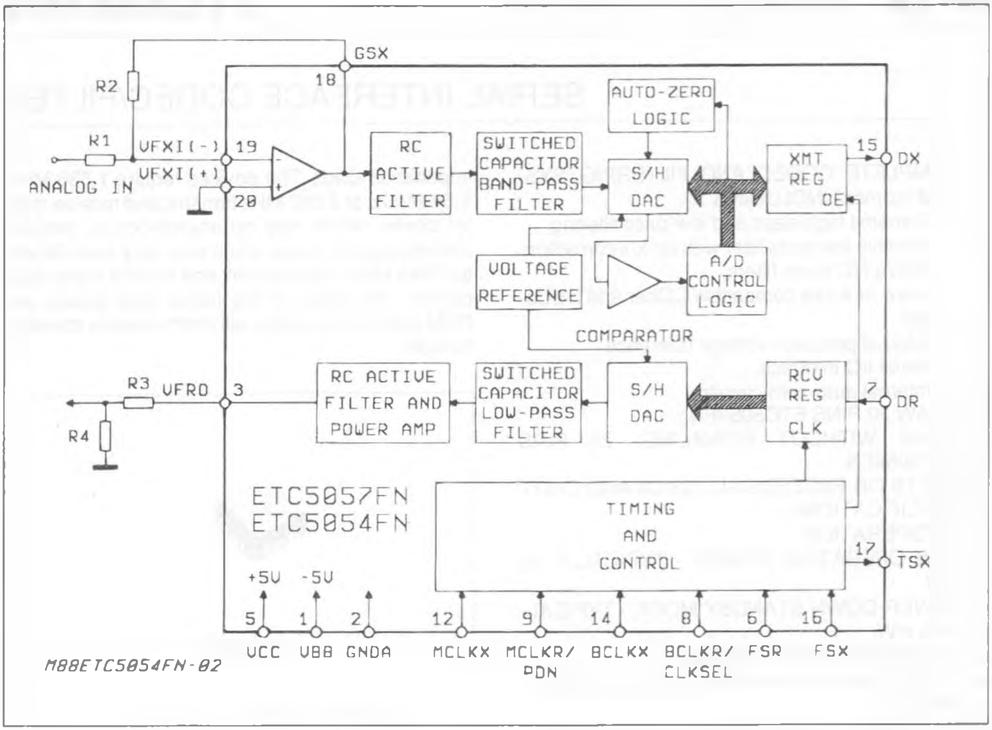
PLCC20

ORDER CODES : ETC5054FN
ETC5057FN

PIN CONNECTIONS



BLOCK DIAGRAM



PIN DESCRIPTION

Name	Pin Type *	N°	Function	Description
V_{BB}	S	1	Negative Power Supply	$V_{BB} = -5\ V \pm 5\ \%$.
GNDA	GND	2	Analog Ground	All signals are referenced to this pin.
VF_RO	O	3	Receive Filter Output	Analog Output of the Receive Filter
V_{CC}	S	5	Positive Power Supply	$V_{CC} = +5\ V \pm 5\ \%$.
FS_R	I	6	Receive Frame Sync Pulse	Enables $BCLK_R$ to shift PCM data into D_R. FS_R is an 8 kHz pulse train. See figures 1, 2 and 3 for timing details.
D_R	I	7	Receive Data Input	PCM data is shifted into D_R following the FS_R leading edge.
$BCLK_R$/CLKSEL	I	8	Shift-in Clock	Shifts data into D_R after the FS_R leading edge. May vary from 64 kHz to 2.048 MHz. Alternatively, may be a logic input which selects either 1.536 MHz/1.544 MHz or 2.048 MHz for master clock in synchronous mode and $BCLK_X$ is used for both transmit and receive directions (see table 1). This input has an internal pull-up.
$MCLK_R$/PDN	I	9	Receive	Must be 1.536 MHz, 1.544 MHz or 2.048 MHz. May be asynchronous with $MCLK_X$, but should be synchronous with $MCLK_X$ for best performance. When $MCLK_R$ is connected continuously low, $MCLK_X$ is selected for all internal timing. When $MCLK_R$ is connected continuously high, the device is powered down.
$MCLK_X$	I	12	Transmit Master Clock	Must be 1.536 MHz, 1.544 MHz or 2.048 MHz. May be asynchronous with $MCLK_R$.
$BCLK_X$	I	14	Shift-out Clock	Shifts out the PCM data on D_X. May vary from 64 kHz to 2.048 MHz, but must be synchronous with $MCLK_X$.
D_X	O	15	Transmit Data Output	The TRI-STATE® PCM data output which is enabled by FS_X.
FS_X	I	16	Transmit Frame Sync Pulse	Enables $BCLK_X$ to shift out the PCM data on D_X. FS_X is an 8 kHz pulse train. See figures 1, 2 and 3 for timing details.
$\overline{TS}_X$	O	17	Transmit Time Slot	Open drain output which pulses low during the encoder time slot. Recommended to be grounded if not used.
GS_X	O	18	Gain Set	Analog output of the transmit input amplifier. Used to set gain externally.
VF_XI^-	I	19	Inverting Amplifier Input	Inverting Input of the Transmit Input Amplifier.
VF_XI^+	I	20	Non-inverting Amplifier Input	Non-inverting Input of the Transmit Input Amplifier.

* I : Input, O : Output, S : Power Supply.

FUNCTIONAL DESCRIPTION

POWER-UP

When power is first applied, power-on reset circuitry initializes the COMBO and places it into the power-down mode. All non-essential circuits are deactivated and the D$_X$ and VF$_R$O outputs are put in high impedance states. To power-up the device, a logical low level or clock must be applied to the MCLK$_R$/PDN pin and FS$_X$ and/or FS$_R$ pulses must be present. Thus, 2 power-down control modes are available. The first is to pull the MCLK$_R$/PDN pin high ; the alternative is to hold both FS$_X$ and FS$_R$ inputs continuously low. The device will power-down approximately 2 ms after the last FS$_X$ or FS$_R$ pulse. Power-up will occur on the first FS$_X$ or FS$_R$ pulse. The TRI-STATE PCM data output, D$_X$, will remain in the high impedance state until the second FS$_X$ pulse.

SYNCHRONOUS OPERATION

For synchronous operation, the same master clock and bit clock should be used for both the transmit and receive directions. In this mode, a clock must be applied to MCLK$_X$ and the MCLK$_R$/PDN pin can be used as a power-down control. A low level on MCLK$_R$/PDN powers up the device and a high level powers down the device. In either case, MCLK$_X$ will be selected as the master clock for both the transmit and receive circuits. A bit clock must also be applied to BCLK$_X$ and the VCLK$_R$/CKSEL can be used to select the proper internal divider for a master clock of 1.536 MHz, 1.544 MHz or 2.048 MHz. For 1.544 MHz operation, the device automatically compensates for the 193rd clock pulse each frame. With a fixed level on the BCLK$_R$/CLKSEL pin, BCLK$_X$ will be selected as the bit clock for both the transmit and receive directions. Table 1 indicates the frequencies of operation which can be selected, depending on the state of BCLK$_R$/CLKSEL. In this synchronous mode, the bit clock, BCLK$_X$, may be from 64 kHz to 2.048 MHz, but must be synchronous with MCLK$_X$.

Table 1 : Selection of Master Clock Frequencies.

BCLK$_R$/CLKSEL	**Master Clock Frequency Selected**	
	ETC5057	**ETC5054**
Clocked	2.048 MHz	1.536 MHz or 1.544 MHz
0	1.536 MHz or 1.544 MHz	2.048 MHz
1 (or open circuit)	2.048 MHz	1.536 MHz or 1.544 MHz

Each FS$_X$ pulse begins the encoding cycle and the PCM data from the previous encode cycle is shifted out of the enabled D$_X$ output on the positive edge of BCLK$_X$. After 8 bit clock periods, the TRI-STATE D$_X$ output is returned to a high impedance state. With and FS$_R$ pulse, PCM data is latched via the D$_R$ input on the negative edge of BCLK$_X$ (or BCLK$_R$ if running). FS$_X$ and FS$_R$ must be synchronous with MCLK$_{X/R}$.

ASYNCHRONOUS OPERATION

For asynchronous operation, separate transmit and receive clocks may be applied. MCLK$_X$ and MCLK$_R$ must be 2.048 MHz for the ETC5057, or 1.536 MHz, 1.544 MHz for the ETC5054, and need not be synchronous. For best transmission performance, however, MCLK$_R$ should be synchronous with MCLK$_X$, which is easily achieved by applying only static logic levels to the MCLK$_R$/PDN pin. This will automatically connect MCLK$_X$ to all internal MCLK$_R$ functions (see pin description). For 1.544 MHz operation, the device automatically compensates for the 193rd clock pulse each frame. FS$_X$ starts each encoding cycle and must be synchronous with MCLK$_X$ and BCLK$_X$. FS$_R$ starts each decoding cycle and must be synchronous with BCLK$_R$. BCLK$_R$ must be a clock, the logic levels shown in table 1 are not valid in asynchronous mode. BCLK$_X$ and BCLK$_R$ may operate from 64 kHz to 2.048 MHz.

SHORT FRAME SYNC OPERATION

The COMBO can utilize either a short frame sync pulse or a long frame sync pulse. Upon power initialization, the device assumes a short frame mode. In this mode, both frame sync pulses, FS$_X$ and FS$_R$, must be one bit clock period long, with timing relationships specified in figure 2. With FS$_X$ high during a falling edge of BCLK$_X$ the next rising edge of BCLK$_X$ enables the D$_X$ TRI-STATE output buffer, which will output the sign bit. The following seven rising edges clock out the remaining seven bits, and the next falling edge disables the D$_X$ output. With FS$_R$ high during a falling edge of BCLK$_R$ (BCLK$_X$ in synchronous mode), the next falling edge of BCLK$_R$ latches in the sign bit. The following seven falling edges latch in the seven remaining bits. Both devices may utilize the short frame sync pulse in synchronous or asynchronous operating mode.

LONG FRAME SYNC OPERATION

To use the long frame mode, both the frame sync pulses, FS$_X$ and FS$_R$, must be three or more bit clock periods long, with timing relationships specified in figure 3. Based on the transmit frame sync, FS$_X$, the

COMBO will sense whether short or long frame sync pulses are being used. For 64 kHz operation, the frame sync pulse must be kept low for a minimum of 160 ns (see fig. 1). The D_X TRI-STATE output buffer is enabled with the rising edge of FS_X or the rising edge of $BCLK_X$, whichever comes later, and the first bit clocked out is the sign bit. The following seven $BCLK_X$ rising edges clock out the remaining seven bits. The D_X output is disabled by the falling $BCLK_X$ edge following the eighth rising edge, or by FS_X going low, which-ever comes later. A rising edge on the receive frame sync pulse, FS_R, will cause the PCM data at D_R to be latched in on the next eight falling edges of $BCLK_R$ ($BCLK_X$ in synchronous mode).

Both devices may utilize the long frame sync pulse in synchronous or asynchronous mode.

TRANSMIT SECTION

The transmit section input is an operational amplifier with provision for gain adjustment using two external resistors, see figure 6. The low noise and wide bandwidth allow gains in excess of 20 dB across the audio passband to be realized. The op amp drives a unitygain filter consisting of RD active pre-filter, followed by an eighth order switched-capacitor bandpass filter clocked at 256 kHz. The output of this filter directly drives the encoder sample-and-hold circuit. The A/D is of companding type according to A-law (ETC5057) or µ–law (ETC5054) coding conventions. A precision voltage reference is trimmed in manufacturing to provide an input overload (t_{MAX}) of nominally 2.5 V peak (see table of transmission charcteristics). The FS_X frame sync pulse controls the sampling of the filter output, and then the successive-approximation encoding cycle begins. The 8-bit code is then loaded into a buffer and shifted out through D_X at the next FS_X pulse. The total encoding delay will be approximately 165 µs (due to the transmit filter) plus 125µs (due to encoding delay), which totals 290µs. Any offset voltage due to the filters or comparator is cancelled by sign bit integration.

RECEIVER SECTION

The receive section consists of an expanding DAC which drives a fifth order switched-capacitor low pass filter clocked at 256 kHz. The decoder is A-law (ETC5057) or µ–law (ETC5054) and the 5th order low pass filter corrects for the sin x/x attenuation due to the 8 kHz sample and hold. The filter is then followed by a 2nd order RC active post-filter and power amplifier capable of driving a 600Ω load to a level of 7.2 dBm. The receive section is unity-gain. Upon the occurence of FS_R, the data at the D_R input is clocked in on the falling edge of the next eight $BCLK_R$ ($BCLK_X$) periods. At the end of the decoder time slot, the decoding cycle begins, and 10µs later the decoder DAC output is updated. The total decoder delay is ~ 10µs (decoder update) plus 110µs (filter delay) plus 62.5µs (1/2 frame), which gives approximately 180µs.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	V_{CC} to GNDA	7	V
V_{BB}	V_{BB} to GNDA	– 7	V
V_{IN}, V_{OUT}	Voltage at any Analog Input or Output	V_{CC} + 0.3 to V_{BB} – 0.3	V
	Voltage at Any Digital Input or Output	V_{CC} + 0.3 to GNDA – 0.3	V
T_{oper}	Operating Temperature Range	– 25 to + 125	°C
T_{stg}	Storage Temperature Range	– 65 to + 150	°C
	Lead Temperature (soldering, 10 seconds)	300	°C

ELECTRICAL OPERATING CHARACTERISTICS V_{CC} = 5.0 V ± 5 %, V_{BB} = – 5.0 V ± 5% GNDA = 0 V, T_A = 0 °C to 70 °C (unless otherwise noted) ; Typical Characteristics Specified at T_A = 25 °C ; all signals are referenced to GNDA.

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{IL}	Input Low Voltage			0.6	V
V_{IH}	Input High Voltage	2.2			V
V_{OL}	Output Low Voltage I_L = 3.2 mA D_X I_L = 3.2 mA, Open Drain $\overline{TS_X}$			0.4 0.4	V
V_{OH}	Output High Voltage I_H = 3.2 mA D_X	2.4			V
I_{IL}	Input Low Current (GNDA ≤ V_{IN} ≤ all digital inputs)	– 10		10	µA
I_{IH}	Input High Current (V_{IH} ≤ V_{IN} ≤ V_{CC}) Except $BCLK_R$/CLKSEL	– 10		10	µA
I_{OZ}	Output Current in High Impedance State (TRI-STATE) (GNDA ≤ V_O ≤ V_{CC}) D_X	– 10		10	µA

ANALOG INTERFACE WITH TRANSMIT INPUT AMPLIFIER (all devices)

Symbol	Parameter	Min.	Typ.	Max.	Unit
I_IXA	Input Leakage Current (– 2.5 V ≤ V ≤ + 2.5 V) VF_XI^+ or VF_XI^-	– 200		200	nA
R_IXA	Input Resistance (– 2.5 V ≤ V ≤ + 2.5 V) VF_XI^+ or VF_XI^-	10			MΩ
R_OXA	Output Resistance (closed loop, unity gain)		1	3	Ω
R_LXA	Load Resistance GS_X	10			kΩ
C_LXA	Load Capacitance GS_X			50	pF
V_OXA	Output Dynamic Range (R_L ≥ 10 kΩ) GS_X	± 2.8			V
A_VXA	Voltage Gain (VF_XI^+ to GS_X)	5000			V/V
F_UXA	Unity Gain Bandwidth	1	2		MHz
$V_{OS}XA$	Offset Voltage	– 20		20	mV
$V_{CM}XA$	Common-mode Voltage	– 2.5		2.5	V
CMRRXA	Common-mode Rejection Ratio	60			dB
PSRRXA	Power Supply Rejection Ratio	60			dB

ANALOG INTERFACE WITH RECEIVE FILTER (all devices)

Symbol	Parameter	Min.	Typ.	Max.	Unit
R_ORF	Output Resistance VF_RO		1	3	Ω
R_LRF	Load Resistance (VF_RO = ± 2.5 V)	600			Ω
C_LRF	Load Capacitance			500	pF
VOS_RO	Output DC Offset Voltage	– 200		200	mV

POWER DISSIPATION (all devices)

Symbol	Parameter	Min.	Typ.	Max.	Unit
$I_{CC}0$	Power-down Current		0.5	1.5	mA
$I_{BB}0$	Power-down Current		0.05	0.3	mA
$I_{CC}1$	Active Current		6.0	9.0	mA
$I_{BB}1$	Active Current		6.0	9.0	mA

TIMING SPECIFICATIONS All timing parameters are measured at V_{OH} = 2.0 V and V_{OL} = 0.7 V. See "definitions" and "timing convertions" sections for that method information.

Symbol	Parameter	Min.	Typ.	Max.	Unit
$1/t_{PM}$	Frequency of master clocks Depends on the device used and the $BCLK_R$/CLKSEL Pin $MCLK_X$ and $MCLK_R$		1.536 1.544 2.048		MHz
t_{WMH}	Width of Master Clock High $MCLK_X$ and $MCLK_R$	160			ns
t_{WML}	Width of Master Clock Low $MCLK_X$ and $MCLK_R$	160			ns
t_{RM}	Rise Time of Master Clock $MCLK_X$ and $MCLK_R$			50	ns
t_{FM}	Fall Time of Master Clock $MCLK_X$ and $MCLK_R$			50	ns
t_{PB}	Period of Bit Clock	485	488	15.725	ns
t_{WBH}	Width of Bit Clock High (V_{IH} = 2.2 V)	160			ns
t_{WBL}	Width of Bit Clock Low (V_{IL} = 0.6 V)	160			ns
t_{RB}	Rise Time of Bit Clock (t_{PB} = 488 ns)			50	ns
t_{FB}	Fall Time of Bit Clock (t_{PB} = 488 ns)			50	ns
t_{SBFM}	set-up time from $BCLK_X$ high to $MCLK_X$ falling edge. (first bit clock after the leading edge of FS_X)	100			ns
t_{HBF}	Holding Time from Bit Clock Low to the Frame Sync (long frame only)	0			ns
t_{SFB}	Set-up Time from Frame Sync to Bit Clock (long frame only)	80			ns
t_{HBFI}	Hold Time from 3rd Period of Bit Clock Low to Frame Sync (long frame only). FS_X or FS_R	100			ns
t_{DZF}	Delay time to valid data from FS_X or $BCLK_X$, whichever comes later and delay time from FS_X to data output disabled. (C_L = 0 pF to 150 pF)	20		165	ns
t_{DBD}	Delay time from $BCLK_X$ high to data valid. (load = 150 pF plus 2 LSTTL loads)	0		180	ns
t_{DZC}	Delay time from $BCLK_X$ low to data output disabled.	50		165	ns
t_{SDB}	Set-up time from D_R valid to $BCLK_{R/X}$ low.	50			ns
t_{HBD}	Hold time from $BCLK_{R/X}$ low to D_R invalid.	50			ns
t_{HOLD}	Holding Time from Bit Clock High to Frame Sync (short frame only)	0			ns
t_{SF}	Set-up Time from $FS_{X/R}$ to $BCLK_{X/R}$ Low (short frame sync pulse) - Note 1	80			ns
t_{HF}	Hold Time from $BCLK_{X/R}$ Low to $FS_{X/R}$ Low (short frame sync pulse) - Note 1	100			ns
t_{XDP}	Delay Time to TS_Xlow (load = 150 pF plus 2 LSTTL loads)			140	ns
t_{WFL}	Minimum Width of the Frame Sync Pulse (low level) (64 k bit/s operating mode)	160			ns

Note : 1. For short frame sync timing. FS_X and FS_R must go high while their respective bit clocks are high.

Figure 1 : 64 k bits/s TIMING DIAGRAM.

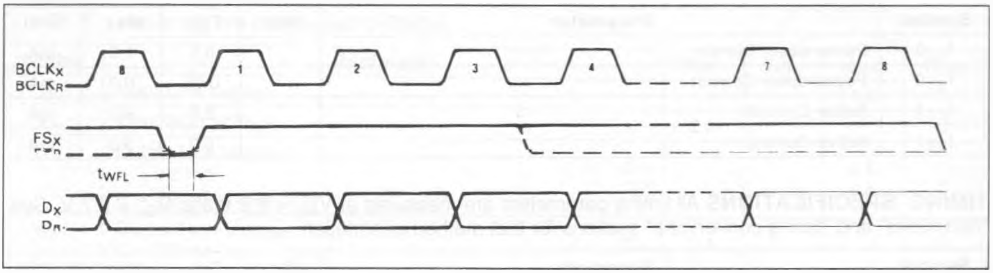


Figure 2 : Short Frame Sync Timing.

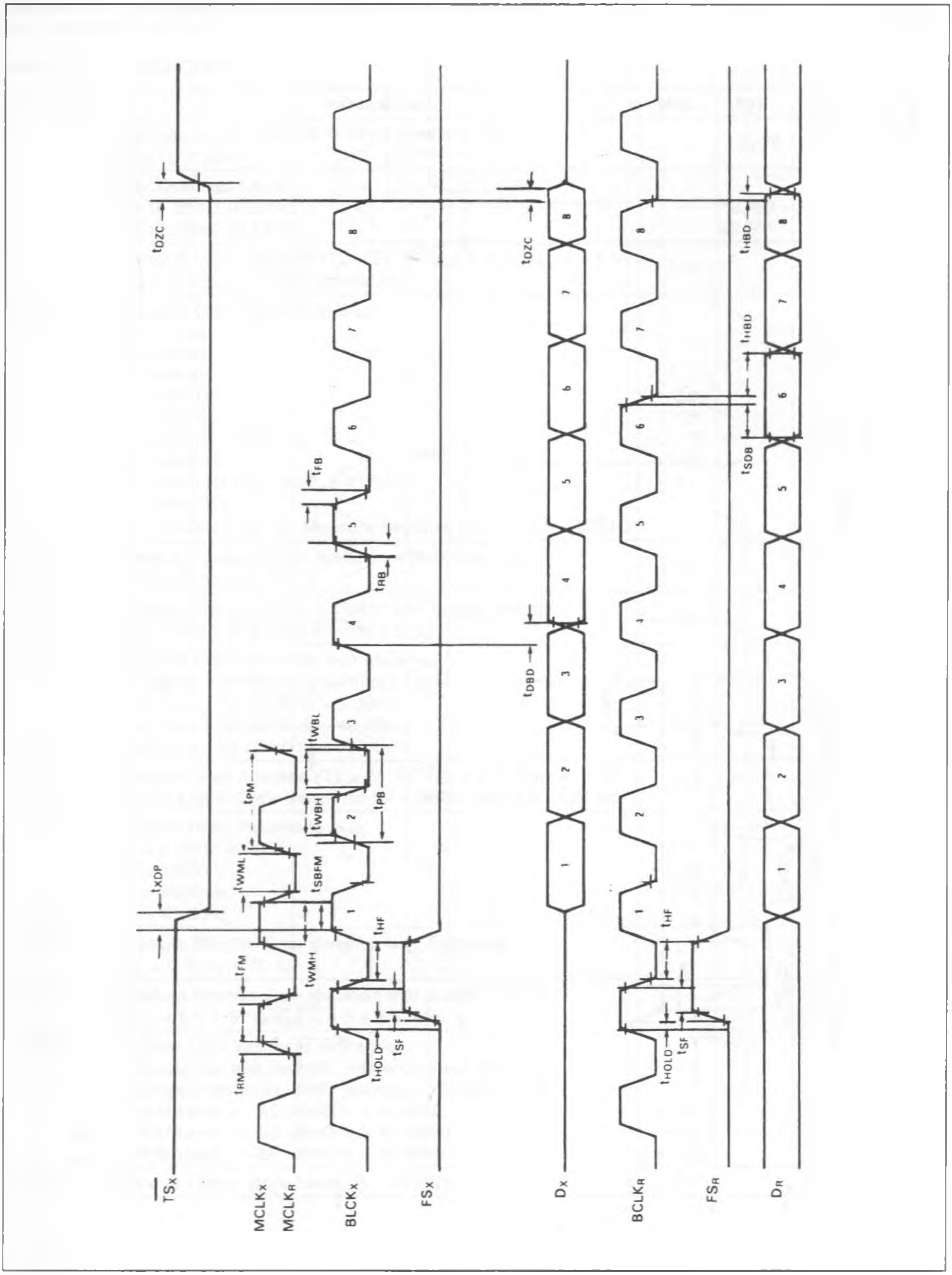
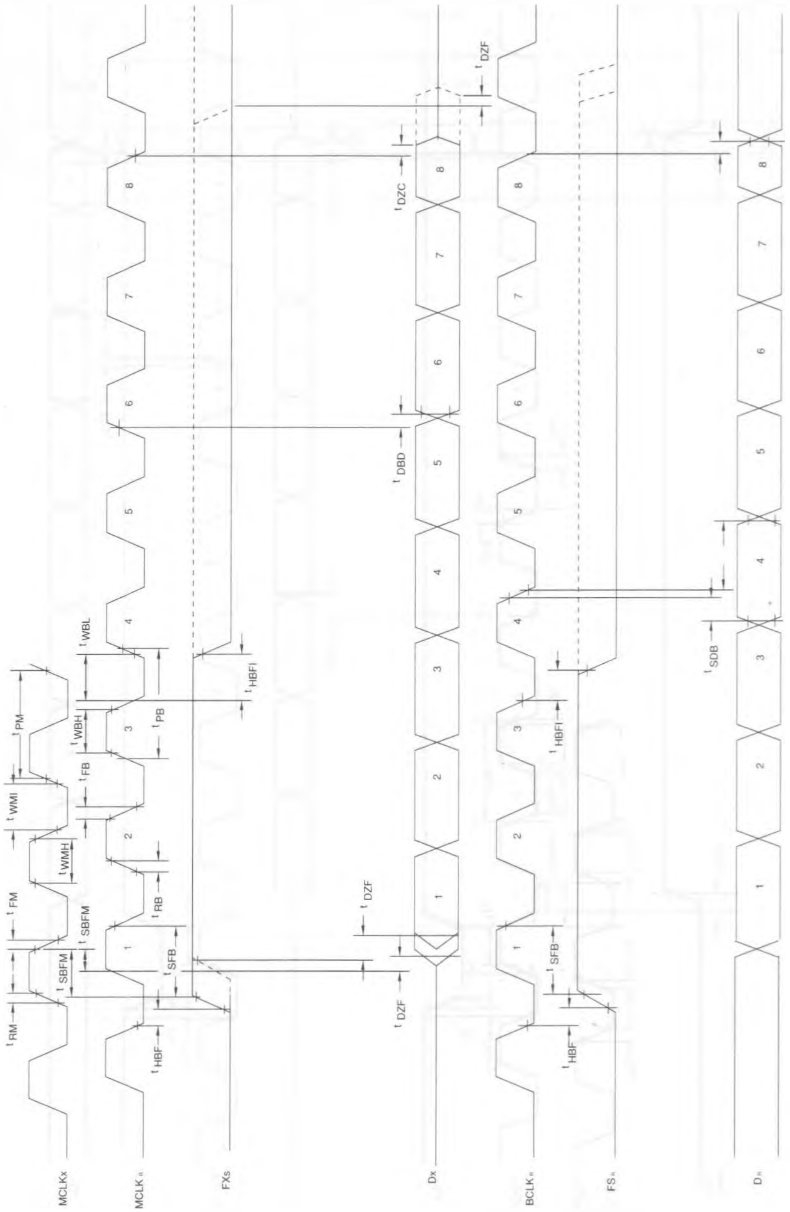


Figure 3 : Long Frame Sync Timing.



TRANSMISSION CHARACTERISTICS (all devices) T_A = 0°C to 70°C, V_{CC} = 5V ± 5%, V_{BB} = – 5V ± 5%, GNDA = 0V, f = 1.02kHz, V_{IN} = 0dBm0 transmit input amplifier connected for unity–gain non–inverting. (unless otherwise specified).

AMPLITUDE RESPONSE

Symbol	Parameter	Min.	Typ.	Max.	Unit
	Absolute levels - nominal 0 dBm0 level is 4 dBm (600 Ω) 0 dBm0		1.2276		Vrms
t_{MAX}	Max Overload Level				V_{PK}
	3.14 dBm0 (A LAW)		2.492		
	3.17 dBm0 (U LAW)		2.501		
G_{XA}	Transmit Gain, Absolute (T_A = 25 °C, V_{CC} = 5 V, V_{BB} = – 5 V) Input at GS_X = 0 dBm0 at 1020 Hz	– 0.15		0.15	dB
G_{XR}	Transmit Gain, Relative to G_{XA}				dB
	f = 16 Hz			– 40	
	f = 50 Hz			– 30	
	f = 60 Hz			– 26	
	f = 180 Hz	– 2.8		– 0.2	
	f = 200 Hz	– 1.8		– 0.1	
	f = 300 Hz - 3000 Hz	– 0.15		0.15	
	f = 3300 Hz	– 0.35		0.05	
	f = 3400 Hz ETC 5057, ETC 5054	– 0.7		0	
	f = 4000 Hz			– 14	
	f = 4600 Hz and up, Measure Reponse from 0 Hz to 4000 Hz			– 32	
G_{XAT}	Absolute Transmit Gain Variation with Temperature (T_A = 0 °C to + 70 °C)	– 0.1		0.1	dB
G_{XAV}	Absolute Transmit Gain Variation with Supply Voltage (V_{CC} = 5 V ± 5 %, V_{BB} = – 5 V ± 5 %)	– 0.05		0.05	dB
G_{XRL}	Transmit Gain Variations with Level Sinusoidal Test Method Reference Level = – 10 dBm0				dB
	VF_XI+ = – 40 dBm0 to + 3 dBm0	– 0.2		0.2	
	VF_XI+ = – 50 dBm0 to – 40 dBm0	– 0.4		0.4	
	VF_XI+ = – 55 dBm0 to – 50 dBm0	– 1.2		1.2	
G_{RA}	Receive Gain, Absolute (T_A = 25 °C, V_{CC} = 5 V, V_{BB} = – 5 V) Input = Digital Code Sequence for 0 dBM0 Signal at 1020 Hz	– 0.15		0.15	dB
G_{RR}	Receive Gain, Relative to G_{RA}				dB
	f = 0 Hz to 3000 Hz	– 0.15		0.15	
	f = 3300 Hz	– 0.35		0.05	
	f = 3400 Hz	– 0.7		0	
	f = 4000 Hz			– 14	
G_{RAT}	Absolute Receive Gain Variation with Temperature (T_A = 0 °C to + 70 °C)			± 0.1	dB
G_{RAV}	Absolute Receive Gain Variation with Supply Voltage (V_{CC} = 5 V ± 5 %, V_{BB} = – 5 v ± 5 %)			± 0.05	dB
G_{RRL}	Receive Gain Variations with Level Sinusuoidal test method ; reference input PCM code corresponds to an ideally encoded – 10 dBm0 signal				dB
	PCM Level = – 40 dBm0 to + 3 dBm0	– 0.2		0.2	
	PCM Level = – 50 dBm0 to – 40 dBm0	– 0.4		0.4	
	PCM Level = – 55 dBm0 to – 50 dBm0	– 1.2		1.2	
V_{RO}	Receive Output Drive Level (R_L = 600 Ω)	– 2.5		2.5	V

TRANSMISSION CHARACTERISTICS (continued).

ENVELOPE DELAY DISTORTION WITH FREQUENCY

Symbol	Parameter	Min.	Typ.	Max.	Unit
D_{XA}	Transmit Delay, Absolute (f = 1600 Hz)		290	315	µs
D_{XR}	Transmit Delay, Relative to D_{XA}				µs
	f = 500 Hz-600 Hz		195	220	
	f = 600 Hz-800 Hz		120	145	
	f = 800 Hz-1000 Hz		50	75	
	f = 1000 Hz-1600 Hz		20	40	
	f = 1600 Hz-2600Hz		55	75	
	f = 2600 Hz-2800 Hz		80	105	
	f = 2800 Hz-3000 Hz		130	155	
D_{RA}	Receive Delay, Absolute (f = 1600 Hz)		180	200	µs
D_{RR}	Receive Delay, Relative to D_{RA}				µs
	f = 500 Hz-1000 Hz	– 40	– 25		
	f = 1000 Hz-1600 Hz	– 30	– 20		
	f = 1600 Hz-2600 Hz		70	90	
	f = 2600 Hz-2800 Hz		100	125	
	f = 2800 Hz-3000 Hz		145	175	

NOISE

Symbol	Parameter	Min.	Typ.	Max.	Unit
N_{XP}	Transmit Noise, P Message Weighted (ETC5057, VF_XI^+ = 0 V)		– 74	– 69 (note 1)	dBm0p
N_{RP}	Receive Noise, P Message Weighted (ETC5057, PCM code equals positive zero)		– 82	– 79	dBm0p
N_{XC}	Transmit Noise, C Message Weighted (ETC5054, VF_XI^+ = 0 V)		12	15	dBrnC0
N_{RC}	Receive Noise, C Message Weighted ETC5054, PCM Code Equals Alternating Positive and Negative Zero		8	11	dBrnC0
N_{RS}	Noise, Single Frequency f = 0 kHz to 100 kHz, Loop around Measurement, VF_XI^+ = 0 Vrms			– 53	dBm0
$PPSR_X$	Positive Power Supply Rejection, Transmit (note 2) – 50 dBm0VF_{XI}^+ V_{CC} = 5.0 V_{DC} + 100 mVrms, f = 0 kHz-50 kHz	40			dBp
$NPSR_X$	Negative Power Supply Rejection, Transmit (note 2) – 50 dBm0VF_{XI}^+ V_{BB} = – 5.0 V_{DC} + 100 mVrms, f = 0 kHz-50 kHz	40			dBp
$PPSR_R$	Positive Power Supply Rejection, Receive (PCM code equals positive zero, V_{CC} = 5.0 V_{DC} + 100 mVrms)				
	f = 0 Hz-4000Hz	40			dBp
	f = 4 kHz-25 kHz	40			dB
	f = 25 kHz-50 kHz	36			dB
$NPSR_R$	Negative Power Supply Rejection, Receive (PCM code equals positive zero, V_{BB} = – 5.0 V_{DC} + 100 mVrms)				
	f = 0 Hz-4000Hz	40			dBp
	f = 4 kHz-25 kHz	40			dB
	f = 25 kHz-50 kHz	36			dB

TRANSMISSION CHARACTERISTICS (continued).

NOISE (continued)

Symbol	Parameter	Min.	Typ.	Max.	Unit
SOS	Spurious out-of-band Signals at the Channel Output Loop around measurement, 0 dBm0, 300 Hz-3400 Hz input applied to DR, measure individual image signals at DX				
	4600 Hz-7600 Hz			– 32	dB
	7600 Hz-8400 Hz			– 40	dB
	8400 Hz-100,000 Hz			– 32	dB

DISTORTION

Symbol	Parameter	Min.	Typ.	Max.	Unit
STD_X or STD_R	Signal to Total Distortion (sinusoidal test method) Transmit or Receive Half-channel				
	Level = 3.0 dBm0	33			dBp
	= 0 dBm0 to – 30 dBm0	36			
	= – 40 dBm0 XMT	29			
	RCV	30			
	= – 55 dBm0 XMT	14			
	RCV	15			
SFD_X	Single Frequency Distortion, transmit			– 46	dB
SFD_R	Single Frequency Distortion, receive			– 46	dB
IMD	Intermodulation Distortion Loop Around Measurement, VF_XI^+ = – 4 dBm0 to – 21 dBm0, two Frequencies in the Range 300 Hz-3400 Hz			– 41	dB

CROSSTALK

Symbol	Parameter	Min.	Typ.	Max.	Unit
CT_{X-R}	Transmit to Receive Crosstalk, 0dBm0 Transmit Level f = 300 Hz-3400 Hz, D_R = Steady PCM Code		– 90	– 75	dB
CT_{R-X}	Receive to Transmit Crosstalk, 0dBm0 Receive Level f = 300 Hz-3400 Hz, VF_XI = 0 V		– 90	– 70 (note 2)	dB

Notes : 1. Measured by extrapolation from the distortion test results.
2. PPSRX, NPSRX, CTR–X are measured with a –50dBm0 activating signal applied at VF_XI+

ENCODING FORMAT AT D_X OUTPUT

	A-Law (including even bit inversion)	μLaw
V_{IN} (at GS_X) = + Full-scale	1 0 1 0 1 0 1 0	1 0 0 0 0 0 0 0
V_{IN} (at GS_X) = 0 V	1 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1	1 1 1 1 1 1 1 1 0 1 1 1 1 1 1 1
V_{IN} (at GS_X) = – Full-scale	0 0 1 0 1 0 1 0	0 0 0 0 0 0 0 0

APPLICATION INFORMATION

POWER SUPPLIES

While the pins at the ETC5050 family are well protected against electrical misuse, it is recommended that the standard CMOS practice be followed, ensuring that ground is connected to the device before any-other connections are made. In applications where the printed circuit board may be plugged into a "hot" socket with power and clocks already present, an extra long ground pin in the connector should be used.

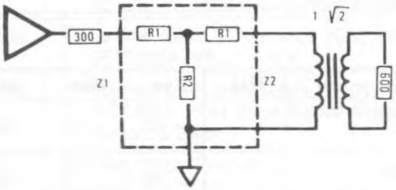
All ground connections to each device should meet at a common point as close as possible to the GNDA pin. This minimizes the interaction of ground return currents flowing through a common bus impedance. 0.1 F supply decoupling capacitors should be connected from this common ground point to V_{CC} and V_{BB} as close to the device as possible.

For best performance, the ground point of each CODEC/FILTER on a card should be connected to a common card ground in star formation, rather than via a ground bus. This common ground point should be decoupled to V_{CC} and V_{BB} with 10µF capacitors.

RECEIVE GAIN ADJUSTMENT

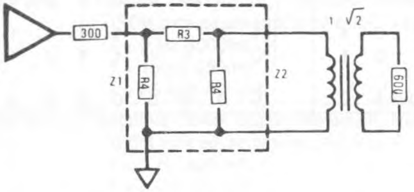
For applications where a ETC5050 family CODEC/filter receive output must drive a 600Ω load, but a peak swing lower then ± 2.5V is required, the receive gain can be easily adjusted by inserting a matched T-pad or π –pad at the output. Table II lists the required resistor values for 600Ω terminations. As these are generally non-standard values, the equations can be used to compute the attenuation of the closest pratical set of resistors. It may be necessary to use unequal values for the R1 or R4 arms of the attenuators to achieve a precise attenuation. Generally it is tolerable to allow a small deviation of the input impedance from nominal while still maintaining a good return loss. For example a 30dB return loss against 600Ω is obtained if the output impedance of the attenuator is in the range 282Ω to 319Ω (assuming a perfect transformer).

Figure 4 : T–PAD Attenuator.



Note 1 : XMIT gain = 20 x log $\left(\frac{R1 + R2}{R2}\right)$ (R1 + R2) > 10kΩ

Figure 5 : π–PAD Attenuator.

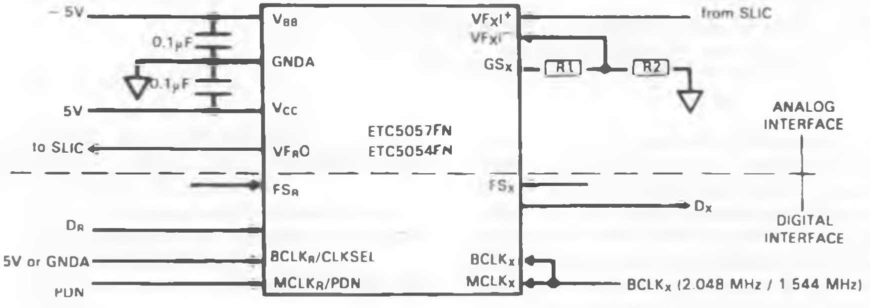


Note 1 : XMIT gain = 20 x log $\left(\frac{R1 + R2}{R2}\right)$ (R1 + R2) > 10kΩ

Table 2 : Attenuator Tables For
Z1 = Z2 = 300 Ω (all values in Ω).

dB	R1	R2	R3	R4
0.1	1.7	26k	3.5	52k
0.2	3.5	13k	6.9	26k
0.3	5.2	8.7k	10.4	17.4k
0.4	6.9	6.5k	13.8	13k
0.5	8.5	5.2k	17.3	10.5k
0.6	10.4	4.4k	21.3	8.7k
0.7	12.1	3.7k	24.2	7.5k
0.8	13.8	3.3k	27.7	6.5k
0.9	15.5	2.9k	31.1	5.8k
1.0	17.3	2.6k	34.6	5.2k
2	34.4	1.3k	70	2.6k
3	51.3	850	107	1.8k
4	68	650	144	1.3k
5	84	494	183	1.1k
6	100	402	224	900
7	115	380	269	785
8	129	284	317	698
9	143	244	370	630
10	156	211	427	527
11	168	184	490	535
12	180	161	550	500
13	190	142	635	473
14	200	125	720	450
15	210	110	816	430
16	218	98	924	413
18	233	77	1.17k	386
20	246	61	1.5k	366

Figure 6 : Typical Synchronous Application.



Note 1 : XMIT gain = $20 \times \log\left(\frac{R1 + R2}{R2}\right)$ (R1 + R2) > 10kΩ