

**SERIAL INTERFACE CODEC/FILTER WITH RECEIVE
POWER AMPLIFIER**

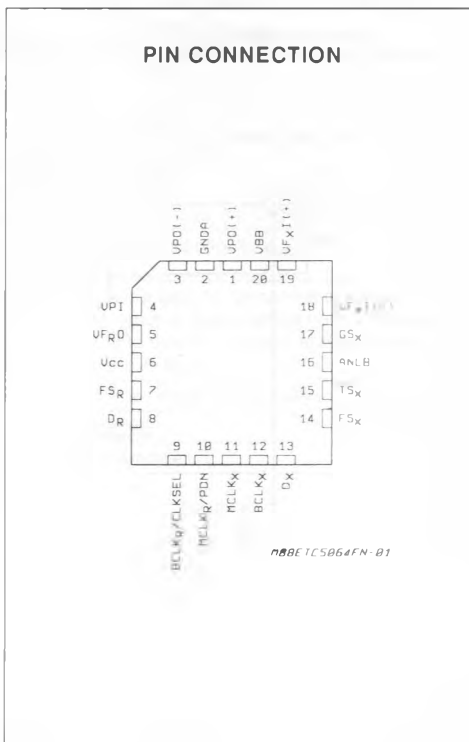
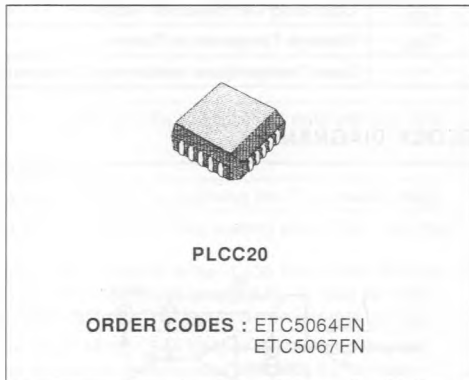
- COMPLETE CODEC AND FILTERING SYSTEM INCLUDING :
 - TRANSMIT HIGH-PASS AND LOW-PASS FILTERING
 - RECEIVE LOW-PASS FILTER WITH SIN X/X CORRECTION
 - ACTIVE RC NOISE FILTER
 - μ -LAW OR A-LAW COMPATIBLE CODER AND DECODER
 - INTERNAL PRECISION VOLTAGE REFERENCE
 - SERIAL I/O INTERFACE
 - INTERNAL AUTO-ZERO CIRCUITRY
 - RECEIVE PUSH-PULL POWER AMPLIFIERS
- μ -LAW 20 PINS ETC5064FN
- A-LAW 20 PINS ETC5067FN
- MEETS OR EXCEEDS ALL D3/D4 AND CCITT SPECIFICATIONS
- $\pm 5V$ OPERATION
- LOW OPERATING POWER-TYPICALLY 70mW
- POWER-DOWN STANDBY MODE-TYPICALLY 3mW
- AUTOMATIC POWER-DOWN
- TTL OR CMOS COMPATIBLE DIGITAL INTERFACES
- MAXIMIZES LINE INTERFACE CARD CIRCUIT DENSITY

DESCRIPTION

The ETC5064 (μ -law) and ETC5067 (A-law) are monolithic PCM CODEC/FILTERS utilizing the A/D and D/A conversion architecture shown in the block diagram below and a serial PCM interface. The devices are fabricated using double-poly CMOS process.

Similar to the ETC5050 family, these devices feature and additional Receive Power Amplifier to provide push-pull balanced output drive capability. The receive gain can be adjusted by means of two external resistors for an output level of up to $\pm 6.6V$ across a balanced 600Ω load.

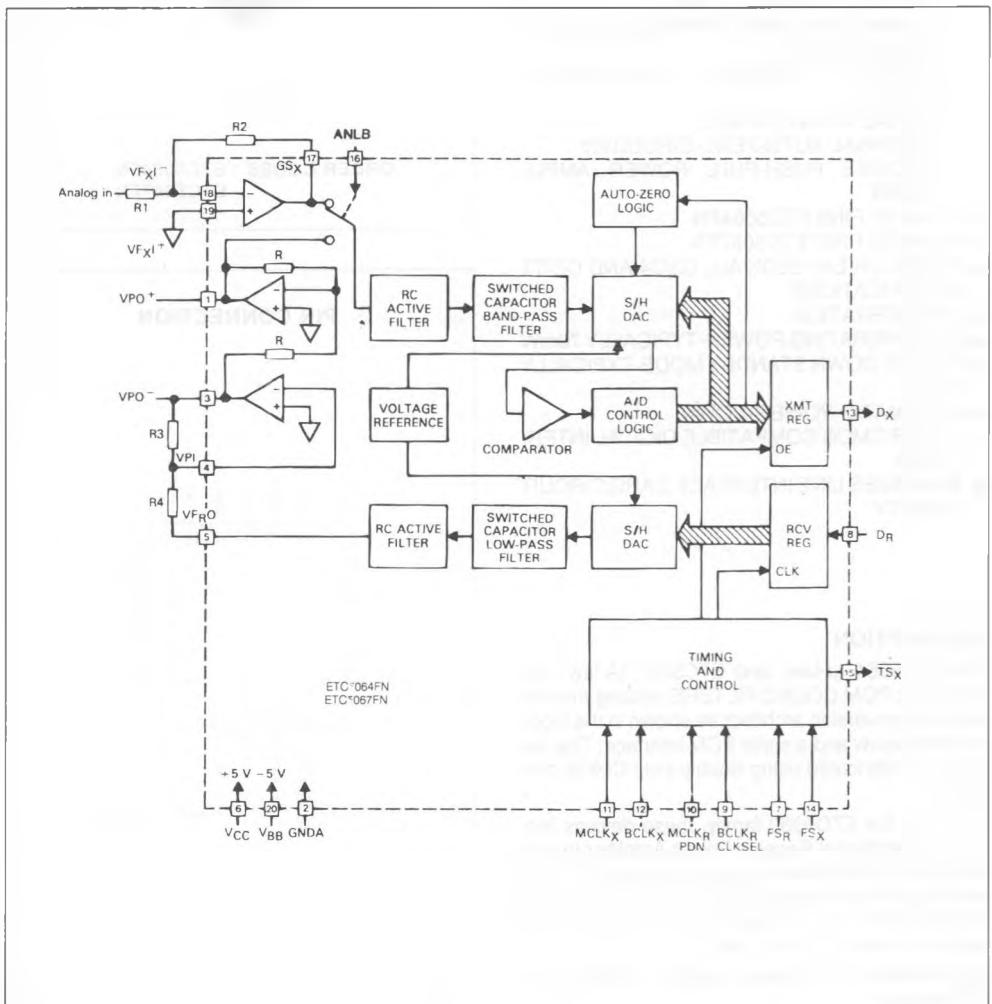
Also included is an Analog Loopback switch and a TS_x output.



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	V_{CC} to GNDA	7	V
V_{BB}	V_{BB} to GNDA	-7	V
V_{IN}, V_{OUT}	Voltage at any Analog Input or Output	$V_{CC} + 0.3$ to $V_{BB} - 0.3$	V
	Voltage at Any Digital Input or Output	$V_{CC} + 0.3$ to $GNDA - 0.3$	V
T_{oper}	Operating Temperature Range	-25 to +125	°C
T_{stg}	Storage Temperature Range	-65 to +150	°C
	Lead Temperature (soldering 10 seconds)	300	°C

BLOCK DIAGRAM



PIN DESCRIPTION

Name	Pin Type	N°	Description
VPO+	O	1	The non-inverted Output of the receive power amplifier.
GND	GND	2	Analog Ground. All signal are referenced to this pin.
VPO-	O	3	The inverted output to the receive power amplifier.
VPI	I	4	Inverting input to the receive power amplifier. Also powers down both amplifiers when connected to V _{BB} .
VF _{RO}	O	5	Analog Output of the Receive Filter
V _{CC}	S	6	Positive Power Supply Pin. V _{CC} = + 5 V ± 5 %
FS _R	I	7	Receive frame sync pulse which enables BCLK _R to shift PCM data into D _R . FS _R is an 8 kHz pulse train. See figures 1 and 2 for timing details.
D _R	I	8	Receive Data Input. PCM data is shifted into D _R following the FS _R leading edge.
BCLK _R /CLKSEL	I	9	The bit clock which shifts data into D _R after the FS _R leading edge. May vary from 64 kHz to 2.048 MHz. Alternatively, may be a logic input which selects either 1.536 MHz/1.544 MHz or 2.048 MHz for master clock in synchronous mode and BCLK _X is used for both transmit and receive directions (see table I). This input has an internal pull-up.
MCLK _R /PDN	I	10	Receive Master Clock. Must be 1.536 MHz, 1.544 MHz or 2.048 MHz. May be asynchronous with MCLK _X , but should be synchronous with MCLK _X for best performance. When MCLK _R is connected continuously low, MCLK _X is selected for all internal timing. When MCLK _R is connected continuously high, the device is powered down.
MCLK _X	I	11	Transmit Master Clock. Must be 1.536 MHz, 1.544 MHz or 2.048 MHz. May be asynchronous with MCLK _R .
BCLK _X	I	12	The bit clock which shifts out the PCM data on D _X . May vary from 64 kHz to 2.048 MHz, but must be synchronous with MCLK _X .
D _X	O	13	The tri-state PCM data output which is enabled by FS _X .
FS _X	I	14	Transmit frame sync pulse input which enables BCLK _X to shift out the PCM data on D _X . FS _X is an 8 kHz pulse train, see figures 1 and 2 timing details.
TS _X	O	15	Open drain output which pulses low during the encoder time slot. Must to be grounded if not used.
ANLB	I	16	Analog Loopback Control Input. Must be set a logic '0' for normal operation. When pulled to logic '1', the transmit filter input is disconnected from the output of the transmit preamplifier and connected to the VPO + output of the receive power amplifier. This input has an internal pull-down.
GS _X	O	17	Analog Output of the Transmit Input Amplifier. Used to externally set gain.
VF _{XI} ⁻	I	18	Inverting Input of the Transmit Input Amplifier.
VF _{XI} ⁺	I	19	Non-inverting Input of the Transmit Input Amplifier.
V _{BB}	S	20	Negative Power Supply Pin. V _{BB} = - 5 V ± 5

* I : Input, O : Output, S : Power Supply

FUNCTIONAL DESCRIPTION

POWER-UP

When power is first applied, power-on reset circuitry initializes the COMBO and places it into the power-down mode. All non-essential circuits are deactivated and the D_X and V_{FRO} outputs are put in high impedance states. To power-up the device, a logical low level or clock must be applied to the $MCLK_R/PDN$ pin and FS_X and/or FS_R pulses must be present. Thus, 2 power-down control modes are available. The first is to pull the $MCLK_R/PDN$ pin high ; the alternative is to hold both FS_X and FS_R inputs continuously low. The device will power-down approximately 2ms after the last FS_X pulse. The TRI-STATE PCM data output, D_X , will remain in the high impedance state until the second FS_X pulse.

SYNCHRONOUS OPERATION

For synchronous operation, the same master clock and bit clock should be used for both the transmit and receive directions. In this mode, a clock must be applied to $MCLK_X$ and the $MCLK_R/PDN$ pin can be used as a power-down control. A low level on $MCLK_R/PDN$ powers up the device and a high level powers down the device. In either case, $MCLK_X$ will be selected as the master clock for both the transmit and receive circuits. A bit clock must also be applied to $BCLK_X$ and the $BCLR/CLKSEL$ can be used to select the proper internal divider for a master clock of 1.536MHz, 1.544MHz or 2.048MHz. For 1.544MHz operation, the device automatically compensates for the 193 rd clock pulse each frame.

With a fixed level on the $BCLK_R/CKSEL$ pin, $BCLK_X$ will be selected as the bit clock for both the transmit and receive directions. Table 1 indicates the frequencies of operation which can be selected, depending on the state of $BCLK_R/CLKSEL$. In this synchronous mode, the bit clock, $BCLK_X$, may be from 64kHz to 2.048MHz, but must be synchronous with $MCLK_X$.

Table 1 : Selection of Master Clock Frequencies.

$BCLK_R/CLKSEL$	Master Clock Frequency Selected	
	ETC5067	ETC5064
Clocked	2.048 MHz	1.536 MHz or 1.544 MHz
0	1.536 MHz or 1.544 MHz	2.048 MHz
1 (or open circuit)	2.048 MHz	1.536 MHz or 1.544 MHz

Each FS_X pulse begins the encode cycle and the PCM data from the previous encode cycle is shift out of the enabled D_X output on the positive edge of $BCLK_X$. After 8 bit clock periods, the TRI-STATE D_X output is returned to a high impedance state. With an FS_R pulse, PCM data is latched via the D_R input the negative edge of $BCLK_X$ (or on $BCLK_R$ if running). FS_X and FS_R must be synchronized with $MCLK_X$.

ASYNCHRONOUS OPERATION

For asynchronous operation, separate transmit and receive clocks may be applied. $MCLK_X$ and $MCLK_R$ must be 2.048MHz for the ETC5067, or 1.536MHz, 1.544MHz for the ETC5064, and need not be synchronous. For best transmission performance, however, $MCLK_R$ should be synchronous with $MCLK_X$, which is easily achieved by applying only static logic levels to the $MCLK_R/PDN$ pin. This will automatically connect $MCLK_X$ to all internal $MCLK_R$ functions (see pin description). For 1.544MHz operation, the device automatically compensates for the 193 rd clock pulse each frame. FS_X starts each encoding cycle and must be synchronous with $MCLK_X$ and $BCLK_X$. FS_R starts each decoding cycle and must be synchronous with $BCLK_R$. $BCLK_R$ must be a clock, the logic levels shown in Table 1 are not valid in asynchronous mode. $BCLK_X$ and $BCLK_R$ may operate from 64kHz to 2.048MHz.

SHORT FRAME SYNC OPERATION

The COMBO can utilize either a short frame sync pulse or a long frame sync pulse. Upon power initialization, the device assumes a short frame mode. In this mode, both frame sync pulses, FS_X and FS_R , must be one bit clock period long, with timing relationships specified in figure 3 with FS_R high during a falling edge of $BCLK_R$, the next rising edge of $BCLK_X$ enables the D_X TRI-STATE output buffer, which will output the sign bit. The following seven rising edges clock out the remaining seven bits, and the next falling edge disables the D_X output. With FS_R high during a falling edge of $BCLK_R$ ($BCLK_X$ in synchronous mode), the next falling edge of $BCLK_R$ latches in the sign bit. The following seven falling edges latch in the seven remaining bits. Both devices may utilize the short frame sync pulse in synchronous or asynchronous operating mode.

LONG FRAME SYNC OPERATION

To use the long frame mode, both the frame sync pulses, FS_X and FS_R , must be three or more bit clock periods long, with timing relationships specified in

figure 3. Based on the transmit frame sync FS_x , the COMBO will sense whether short or long frame sync pulses are being used. For 64kHz operation, the frame sync pulse must be kept low for a minimum of 160ns (see fig. 1). The D_x TRI-STATE output buffer is enabled with the rising edge of FS_x or the rising edge of $BCLK_x$, whichever comes later, and the first bit clocked out is the sign bit. The following seven $BCLK_x$ rising edges clock out the remaining seven bits. The D_x output is disabled by the falling $BCLK_x$ edge following the eighth rising edge, or by FS_x going low, whichever comes later. A rising edge on the receive frame sync pulse, FS_R , will cause the PCM data at D_R to be latched in on the next eight falling edges of $BCLK_R$ ($BCLK_x$ in synchronous mode). Both devices may utilize the long frame sync pulse in synchronous or asynchronous mode.

TRANSMIT SECTION

The transmit section input is an operational amplifier with provision for gain adjustment using two external resistors, see figure 4. The low noise and wide bandwidth allow gains in excess of 20dB across the audio passband to be realized. The op amp drives a unity gain filter consisting of RC active pre-filter, followed by an eighth order switched-capacitor bandpass filter clocked at 256kHz. The output of this filter directly drives the encoder sample-and-hold circuit. The A/D is of companding type according to A-law (ETC5067) or μ -law (ETC5064) coding conventions. A precision voltage reference is trimmed in manufacturing to provide an input overload (I_{MAX}) of nominally 2.5V peak (see table of Transmission Characteristics). The FS_x frame sync pulse controls the sampling of the filter output, and then the successive-approximation encoding cycle begins. The 8-bit code is then loaded into a buffer and shifted out through D_x at the next FS_x pulse. The total encoding delay will be approximately 165 μ s (due to the transmit filter) plus 125 μ s (due to encoding delay), which totals 290 μ s. Any offset voltage

due to the filters or comparator is cancelled by sign bit integration.

RECEIVE SECTION

The receive section consist of an expanding DAC which drives a fifth order switched-capacitor low pass filter clocked at 256kHz. The decoder is A-law (ETC5067) or μ -law (ETC5064) and the 5th order low pass filter corrects for the $\sin x/x$ attenuation due to the 8kHz sample and hold. The filter is then followed by a 2nd order RC active post-filter and power amplifier capable of driving a 600 Ω load to a level of 7.2dBm. The receive section is unity-gain. Upon the occurrence of FS_R , the data at the DR input is clocked in on the falling edge of the next eight $BCLK_R$ ($BCLK_x$) periods. At the end of the decoder time slot, the decoding cycle begins, and 10 μ s later the decoder DAC output is updated. The total decoder delay is \sim 10 μ s (decoder up-date) plus 110 μ s (filter delay) plus 62.5 μ s (1/2 frame), which gives approximately 180 μ s.

RECEIVE POWER AMPLIFIERS

Two inverting mode power amplifiers are provided for directly driving a matched line interface transformer. The gain of the first power amplifier can be adjusted to boost the \pm 2.5V peak output signal from the receive filter up \pm 3.3V peak into an unbalanced 300 Ω load, or \pm 4.0V into an unbalanced 15k Ω load. The second power amplifier is internally connected in unity-gain inverting mode to give 6dB of signal gain for balanced loads. Maximum power transfer to a 600 Ω subscriber line termination is obtained by differentially driving a balanced transformer with a $\sqrt{2} : 1$ turns ratio, as shown in figure 4. A total peak power of 15.6dBm can be delivered to the load plus termination. Both power amplifier can be powered down independently from the PDN input by connecting the VPI input to V_{BB} saving approximately 12mW of power.

ELECTRICAL OPERATING CHARACTERISTICS $V_{CC} = 5.0 \text{ V} \pm 5\%$, $V_{BB} = -5\%$, $G_NDA = 0 \text{ V}$, $T_A = 0 \text{ }^\circ\text{C}$ to $70 \text{ }^\circ\text{C}$ (unless otherwise noted) ; typical characteristics specified at $V_{CC} = 5.0\text{V}$, $V_{BB} = -5.0\text{V}$, $T_A = 25 \text{ }^\circ\text{C}$; all signals are referenced to G_NDA .

DIGITAL INTERFACE (all devices)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{IL}	Input Low Voltage			0.6	V
V_{IH}	Input High Voltage	2.2			V
V_{OL}	Output Low Voltage $I_L = 3.2 \text{ mA}$ $I_L = 3.2 \text{ mA}$, Open Drain	$\frac{D_x}{TS_x}$		0.4 0.4	V
V_{OH}	Output High Voltage $I_H = 3.2 \text{ mA}$	D_x	2.4		V
I_{IL}	Input Low Current ($G_NDA \leq V_{IN} \leq V_{IL}$) all Digital Inputs Except $BCLK_R$	- 10		10	μA
I_{IH}	Input High Current ($V_{IH} \leq V_{IN} \leq V_{CC}$) Except ANLB	- 10		10	μA
I_{OZ}	Output Current in High Impedance State (TRI-STATE) ($G_NDA \leq V_O \leq V_{CC}$)	D_x	- 10	10	μA

ANALOG INTERFACE WITH TRANSMIT INPUT AMPLIFIER (all devices)

Symbol	Parameter	Min.	Typ.	Max.	Unit
I_{XA}	Input Leakage Current ($-2.5 \text{ V} \leq V \leq +2.5 \text{ V}$)	VF_{xI}^+ or VF_{xI}^-	- 200	200	nA
R_{IXA}	Input Resistance ($-2.5 \text{ V} \leq V \leq +2.5 \text{ V}$)	VF_{xI}^+ or VF_{xI}^-	10		$\text{M}\Omega$
R_{OXA}	Output Resistance (closed loop, unity gain)		1	3	Ω
R_{LXA}	Load Resistance	GS_x	10		$\text{k}\Omega$
C_{LXA}	Load Capacitance	GS_x		50	pF
V_{OXA}	Output Dynamic Range ($R_L \geq 10 \text{ k}\Omega$)	GS_x	- 2.8	+ 2.8	V
A_{VXA}	Voltage Gain (VF_{xI}^+ to GS_x)		5000		V/V
F_{UXA}	Unity Gain Bandwidth		1	2	MHz
V_{OSXA}	Offset Voltage		- 20	20	mV
V_{CMXA}	Common-mode Voltage		- 2.5	2.5	V
CMRRXA	Common-mode Rejection Ratio		60		dB
PSRRXA	Power Supply Rejection Ratio		60		dB

ANALOG INTERFACE WITH RECEIVE FILTER (all devices)

Symbol	Parameter	Min.	Typ.	Max.	Unit
R_{ORF}	Output Resistance	VF_{RO}	1	3	Ω
R_{LRF}	Load Resistance ($VF_{RO} = \pm 2.5 \text{ V}$)	10			$\text{k}\Omega$
C_{LRF}	Load Capacitance			25	pF
V_{OSRO}	Output DC Offset Voltage	- 200		200	mV

ANALOG INTERFACE WITH POWER AMPLIFIERS (all devices)

Symbol	Parameter	Min.	Typ.	Max.	Unit
IPI	Input Leakage Current ($-1.0\text{ V} \leq V_{PI} \leq 1.0\text{ V}$)	- 100		100	nA
RIPI	Input Resistance ($-1.0 \leq V_{PI} \leq 1.0\text{ V}$)	10			M Ω
VIOS	Input Offset Voltage	- 25		25	mV
ROP	Output Resistance (inverting unity-gain at VPO ⁻ or VPO ⁻)		1		Ω
F _C	Unity-gain Bandwidth, Open Loop (VPO ⁻)		400		kHz
C _L P	Load Capacitance (VPO ⁺ or VPO ⁻ to GNDA) R _L \geq 1500 Ω R _L = 600 Ω R _L = 300 Ω			100 500 1000	pF
GAp ⁺	Gain VPO ⁻ to VPO ⁺ to GNDA, Level at VPO ⁻ = 1.77 Vrms (+ 3 dBm0)		- 1		V/V
PSRRp	Power Supply Rejection of V _{CC} or V _{BB} (VPO ⁻ connected to VPI) 0 kHz - 4 kHz 0 kHz - 50 kHz	60 36			dB

POWER DISSIPATION (all devices)

Symbol	Parameter	Min.	Typ.	Max.	Unit
I _{CC0}	Power-down Current		0.5	1.5	mA
I _{BB0}	Power-down Current		0.05	0.3	mA
I _{CC1}	Active Current		7.0	10.0	mA
I _{BB1}	Active Current		7.0	10.0	mA

TIMING SPECIFICATIONS All timings parameters are measured at $V_{OH} = 2.0$ V and $V_{OL} = 0.7$ V.

Symbol	Parameter	Min.	Typ.	Max.	Unit	
$1/t_{PM}$	Frequency of master clocks Depends on the device used and the BCLK _R /CLKSEL Pin	MCLK _X and MCLK _R	1.536 1.544 2.048		MHz	
t_{WMH}	Width of Master Clock High	MCLK _X and MCLK _R	160		ns	
t_{WML}	Width of Master Clock Low	MCLK _X and MCLK _R	160		ns	
t_{RM}	Rise Time of Master Clock	MCLK _X and MCLK _R		50	ns	
t_{FM}	Fall Time of Master Clock	MCLK _X and MCLK _R		50	ns	
t_{PB}	Period of Bit Clock		485	488	15.725	ns
t_{WBH}	Width of Bit Clock High ($V_{IH} = 2.2$ V)		160		ns	
t_{WBL}	Width of Bit Clock Low ($V_{IL} = 0.6$ V)		160		ns	
t_{RB}	Rise Time of Bit Clock ($t_{PB} = 488$ ns)			50	ns	
t_{FB}	Fall Time of Bit Clock ($t_{PB} = 488$ ns)			50	ns	
t_{SBFM}	Set-up time from BCLK _X high to MCLK _X falling edge (first bit clock after the leading edge of FS _X)		100		ns	
t_{HBF}	Holding Time from Bit Clock Low to the Frame Sync (long frame only)		0		ns	
t_{SFB}	Set-up Time from Frame Sync to Bit Clock (long frame only)		80		ns	
t_{HBF1}	Hold Time from 3rd Period of Bit Clock Low to Frame Sync (long frame only)	FS _X or FS _R	100		ns	
t_{DZF}	Delay Time to valid data from FS _X or BCLK _X , whichever comes later and delay time from FS _X to data output disabled ($C_L = 0$ pF to 150 pF)		20	165	ns	
t_{DBD}	Delay Time from BCLK _X high to data valid (load = 150 pF plus 2 LSTTL loads)		0	180	ns	
t_{DZC}	Delay Time from BCLK _X low to data output disabled		50	165	ns	
t_{SDB}	Set-up Time from D _R valid to BCLK _{R/X} low		50		ns	
t_{HBD}	Hold Time from BCLK _{R/X} low to D _R invalid		50		ns	
t_{HOLD}	Holding Time from Bit Clock High to Frame Sync (short frame only)		0		ns	
t_{SF}	Set-up Time from FS _{X/R} to BCLK _{X/R} Low (short frame sync pulse) - Note 1		80		ns	
t_{HF}	Hold Time from BCLK _{X/R} Low to FS _{X/R} Low (short frame sync pulse) - Note 1		100		ns	
t_{XDp}	Delay Time to TS _X low (load = 150 pF plus 2 LSTTI loads)			140	ns	
t_{WFL}	Minimum Width of the Frame Sync Pulse (low level) (64 bit/s operating mode)		160		ns	

Note : 1. For short frame sync timing, FS_X and FS_R must go high while their respective bit clocks are high.

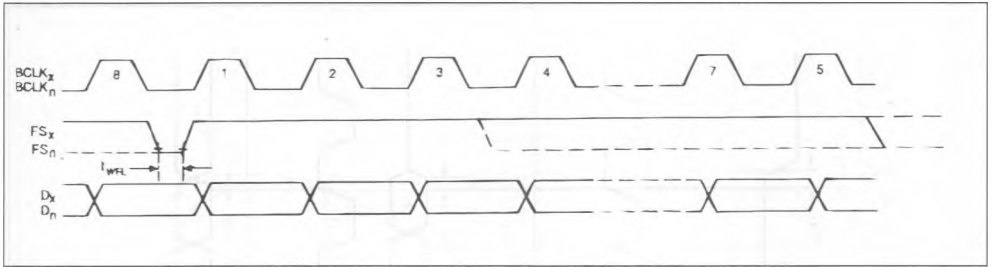
Figure 1 : 64 k bits/s TIMING DIAGRAM. (see next page for complete timing)

Figure 2 : Short Frame Sync Timing.

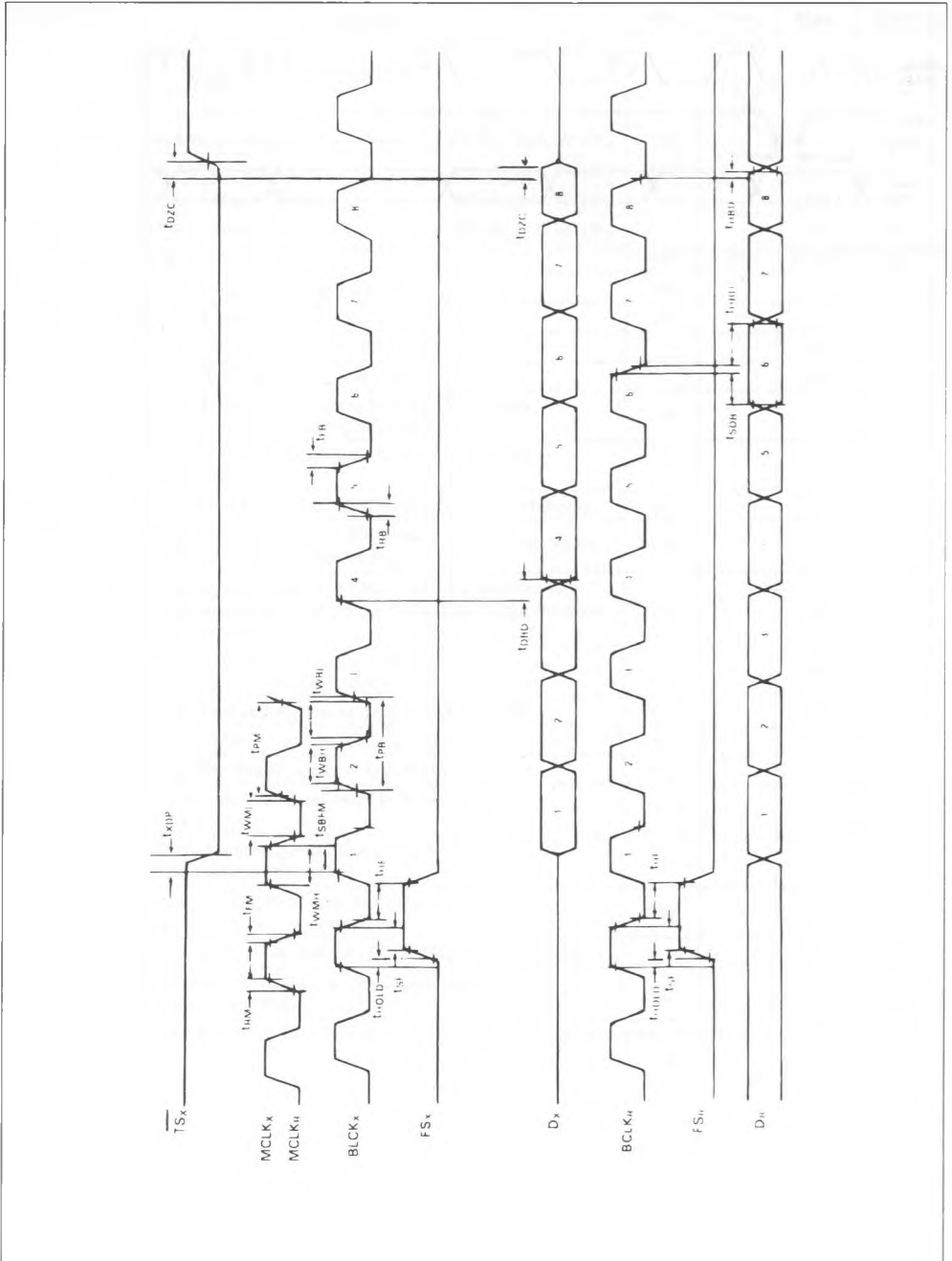
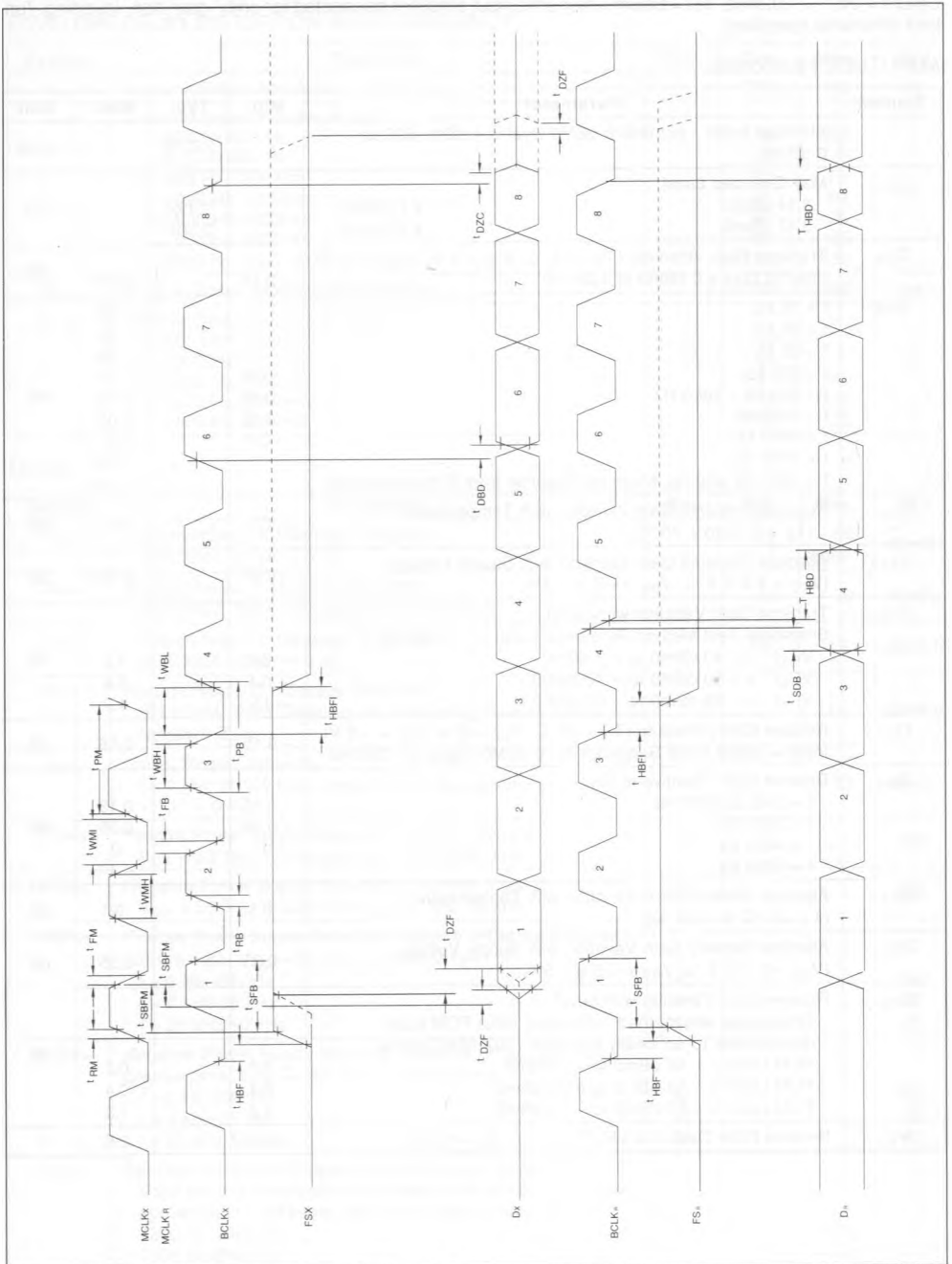


Figure 3 : Long Frame Sync Timing.



TRANSMISSION CHARACTERISTICS (all devices) $T_A = 0^\circ\text{C}$ to 70°C , $V_{CC} = 5\text{V} \pm 5\%$, $V_{BB} = -5\text{V} \pm 5\%$, $G_{NDA} = 0\text{V}$, $f = 1.02\text{kHz}$, $V_{IN} = 0\text{dBm0}$, transmit input amplifier connected for unity-gain non-inverting. (unless otherwise specified).

AMPLITUDE RESPONSE

Symbol	Parameter	Min.	Typ.	Max.	Unit
	Absolute levels - nominal 0 dBm0 level is 4 dBm (600 Ω) 0 dBm0		1.2276		Vrms
t_{MAX}	Max Overload Level 3.14 dBm0 ETC5067 3.17 dBm0 ETC5064		2.492 2.501		V_{PK}
G_{XA}	Transmit Gain, Absolute ($T_A = 25^\circ\text{C}$, $V_{CC} = 5\text{V}$, $V_{BB} = -5\text{V}$) Input at $G_{SX} = 0\text{dBm0}$ at 1020 Hz	- 0.15		0.15	dB
G_{XR}	$f = 16\text{ Hz}$ $f = 50\text{ Hz}$ $f = 60\text{ Hz}$ $f = 200\text{ Hz}$ $f = 300\text{ Hz} - 3000\text{ Hz}$ $f = 3300\text{ Hz}$ $f = 3400\text{ Hz}$ $f = 4000\text{ Hz}$ $f = 4600\text{ Hz}$ and up, Measure Reponse from 0 Hz to 4000 Hz	- 1.8 - 0.15 - 0.35 - 0.7		- 40 - 30 - 26 - 0.1 0.15 0.05 0 - 14 - 32	dB
G_{XAT}	Absolute Transmit Gain Variation with Temperature ($T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$)	- 0.1		0.1	dB
G_{XAV}	Absolute Transmit Gain Variation with Supply Voltage ($V_{CC} = 5\text{V} \pm 5\%$, $V_{BB} = -5\text{V} \pm 5\%$)	- 0.05		0.05	dB
G_{XRL}	Transmit Gain Variation with Level Sinusoidal Test Method Reference Level = - 10 dBm0 $V_{FXL}^+ = -40\text{ dBm0}$ to $+3\text{ dBm0}$ $V_{FXL}^- = -50\text{ dBm0}$ to -40 dBm0 $V_{FXL}^+ = -55\text{ dBm0}$ to -50 dBm0	- 0.2 - 0.4 - 1.2		0.2 0.4 1.2	dB
G_{RA}	Receive Gain, Absolute ($T_A = 25^\circ\text{C}$, $V_{CC} = 5\text{V}$, $V_{BB} = -5\text{V}$) Input = Digital Code Sequence for 0 dBm0 Signal at 1020 Hz	- 0.15		0.15	dB
G_{RR}	Receive Gain, Relative to G_{RA} $f = 0\text{ Hz}$ to 3000 Hz $f = 3300\text{ Hz}$ $f = 3400\text{ Hz}$ $f = 4000\text{ Hz}$	- 0.15 - 0.35 - 0.7		0.15 0.05 0 - 14	dB
G_{RAT}	Absolute Receive Gain Variation with Temperature ($T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$)	- 0.1		0.1	dB
G_{RAV}	Absolute Receive Gain Variation with Supply Voltage ($V_{CC} = 5\text{V} \pm 5\%$, $V_{BB} = -5\text{V} \pm 5\%$)	- 0.05		0.05	dB
G_{RRL}	Receive Gain Variation with Level Sinusoidal test method ; reference input PCM code corresponds to an ideally encoded - 10 dBm0 signal PCM Level = - 40 dBm0 to $+3\text{ dBm0}$ PCM Level = - 50 dBm0 to -40 dBm0 PCM Level = - 55 dBm0 to -50 dBm0	- 0.2 - 0.4 - 1.2		0.2 0.4 1.2	dB
V_{RO}	Receive Filter Output at VR_{FO} $R_L = 10\text{ k}\Omega$	- 2.5		2.5	V

TRANSMISSION CHARACTERISTICS (continued).

ENVELOPE DELAY DISTORTION WITH FREQUENCY

Symbol	Parameter	Min.	Typ.	Max.	Unit
D_{XA}	Transmit Delay, Absolute ($f = 1600$ Hz)		290	315	μ s
D_{XR}	Transmit Delay, Relative to D_{XA} $f = 500$ Hz-600 Hz $f = 600$ Hz-800 Hz $f = 800$ Hz-1000 Hz $f = 1000$ Hz-1600 Hz $f = 1600$ Hz-2600Hz $f = 2600$ Hz-2800 Hz $f = 2800$ Hz-3000 Hz		195 120 50 20 55 80 130	220 145 75 40 75 105 155	μ s
D_{RA}	Receive Delay, Absolute ($f = 1600$ Hz)		180	200	μ s
D_{RR}	Receive Delay, Relative to D_{RA} $f = 500$ Hz-1000 Hz $f = 1000$ Hz-1600 Hz $f = 1600$ Hz-2600 Hz $f = 2600$ Hz-2800 Hz $f = 2800$ Hz-3000 Hz	- 40 - 30	- 25 - 20 70 100 145	90 125 175	μ s

NOISE

Symbol	Parameter	Min.	Typ.	Max.	Unit
N_{XP}	Transmit Noise, P Message Weighted (ETC5067, $V_{Fxl}^* = 0$ V)		- 74	- 69 (note 1)	dBm0p
N_{RP}	Receive Noise, P Message Weighted (ETC5067, PCM code equals positive zero)		- 82	- 79	dBm0p
N_{XC}	Transmit Noise, C Message Weighted (ETC5064, $V_{Fxl}^* = 0$ V)		12	15	dBmC0
N_{PC}	Receive Noise, C Message Weighted (ETC5064, PCM Code Equals Alternating Positive and Negative Zero)		8	11	dBmC0
N_{RS}	Noise, Single Frequency $f = 0$ kHz to 100 kHz, Loop around Measurement. $V_{Fxl}^* = 0$ V			- 53	dBm0
$PPSR_X$	Positive Power Supply Rejection, Transmit (note 2) $V_{CC} = 5.0$ V _{DC} + 100 mVrms, $f = 0$ kHz-50 kHz	40			dBp
$NPSR_X$	Negative Power Supply Rejection, Transmit (note 2) $V_{BB} = 5.0$ V _{DC} + 100 mVrms, $f = 0$ kHz-50 kHz	40			dBp
$PPSR_R$	Positive Power Supply Rejection, Receive (PCM code equals positive zero, $V_{CC} = 5.0$ V _{DC} + 100 mVrms) $f = 0$ Hz-4000Hz $f = 4$ kHz-25 kHz $f = 25$ kHz-50 kHz	5067 40 40 36			dBp dB dB
$NPSR_R$	Negative Power Supply Rejection, Receive (PCM code equals positive zero, $V_{BB} = - 5.0$ V _{DC} + 100 mVrms) $f = 0$ Hz-4000Hz $f = 4$ kHz-25 kHz $f = 25$ kHz-50 kHz	5067 40 40 36			dBp dB dB
SOS	Spurious out-of-band Signals at the Channel Output Loop around measurement, 0 dBm0, 300 Hz-3400 Hz input applied to D_R , measure individual image signals at D_X 4600 Hz-7600 Hz 7600 Hz-8400 Hz 8400 Hz-100,000 Hz			- 32 - 40 - 32	

TRANSMISSION CHARACTERISTICS (continued).

DISTORTION

Symbol	Parameter	Min.	Typ.	Max.	Unit
STD _X or STD _R	Signal to Total Distortion (sinusoidal test method)				
	Transmit or Receive Half-channel Level = 3.0 dBm0	33			dBp
	= 0 dBm0 to - 30 dBm0	36			
	= - 40 dBm0	XMT 29			
		RCV 30			
= - 55 dBm0	XMT 14 RCV 15				
SFD _X	Single Frequency Distortion, Transmit			- 46	dB
SFD _R	Single Frequency Distortion, Receive			- 46	dB
IMD	Intermodulation Distortion Loop Around Measurement, VF _{XI} * = - 4 dBm0 to - 21 dBm0, two Frequencies in the Range 300 Hz-3400 Hz			- 41	dB

CROSSTALK

Symbol	Parameter	Min.	Typ.	Max.	Unit
CT _{X-R}	Transmit to Receive Crosstalk, 0dBm0 Transmit f = 300 Hz-3400 Hz, D _R = Steady PCM Code		- 90	- 75	dB
CT _{R-X}	Receive to Transmit Crosstalk, 0dBm0 Receive Level f = 300 Hz-3400 Hz, VF _{XI} = 0 V		- 90	- 70 (note 2)	dB

POWER AMPLIFIERS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V _{OL}	Maximum 0 dBm0 Level for Better than ± 0.1 dB Linearity Over the Range 10 dBm0 to + 3 dBm0 (balanced load, R _L connected between VPO ⁺ and VPO ⁻) R _L = 600 Ω R _L = 1200 Ω R _L = 30 kΩ	3.3 3.5 4.0			V _{rms}
S/D _P	Signal/Distortion R _L = 600 Ω, 0 dBm0	50			dB

- Notes :** 1. Measured by extrapolation from the distortion test results
2. PPSRX, NPSRX, CTR-X measured with a -50dBm0 activating signal applied at VF_{XI}*

ENCODING FORMAT AT D_X OUTPUT

	A-Law (including even bit inversion)	μLaw
V _{IN} (at GS _X) = + Full-scale	1 0 1 0 1 0 1 0	1 0 0 0 0 0 0 0
V _{IN} (at GS _X) = 0 V	1 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1	1 1 1 1 1 1 1 1 0 1 1 1 1 1 1 1
V _{IN} (at GS _X) = - Full-scale	0 0 1 0 1 0 1 0	0 0 0 0 0 0 0 0

APPLICATION INFORMATION

POWER SUPPLIES

While the pins at the ETC5060 family are well protected against electrical misure, it is recommended that the standard CMOS practice be followed, ensuring that ground is connected to the device before any other connections are made. In applications where the printed circuit board may be plugged into a "hot" socket with power and clocks already present, an extra long ground pin in the connector should be used.

All ground connections to each device should meet at a common point as close as possible to the GNDA

pin. This minimizes the interaction of ground return currents flowing through a common bus impedance. 0.1µF supply decoupling capacitors should be connected from this common ground point to V_{CC} and V_{BB} as close to the device as possible.

For best performance, the ground point of each CODEC/FILTER on a card should be connected to a common card ground in star formation, rather than via a ground bus. This common ground point should be decoupled to V_{CC} and V_{BB} with 10µF capacitors.

For best performance, TSX should be grounded if not used.

Figure 4 : Typical Asynchronous Application.

