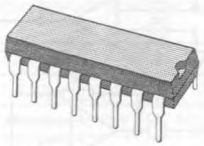
SGS-THOMSON MICROELECTRONICS

ETC50S64
ETC50S67

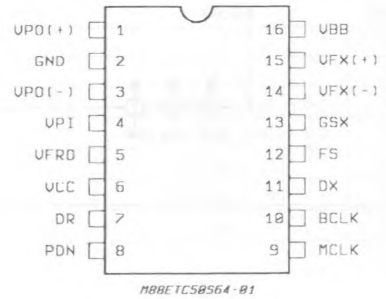
SYNCHRONOUS SERIAL INTERFACE CODEC/FILTER WITH RECEIVE POWER AMPLIFIER

- COMPLETE CODEC AND FILTERING SYSTEM (combo) INCLUDING :
  - TRANSMIT HIGH-PASS AND LOW-PASS FILTERING
  - RECEIVE LOW-PASS FILTER WITH SIN X/X CORRECTION
  - ACTIVE RC NOISE FILTERS
  - μ-LAW OR A-LAW COMPATIBLE CODER AND DECODER
  - INTERNAL PRECISION VOLTAGE REFERENCE
  - SERIAL I/O INTERFACE
  - INTERNAL AUTO-ZERO CIRCUITRY
  - RECEIVE PUSH-PULL POWER AMPLIFIERS
- μ-LAW ETC50S64
- A-LAW ETC50S67
- MEETS OR EXCEEDS ALL D3/D4 AND CCITT SPECIFICATIONS
- ± 5 V OPERATION
- LOW OPERATING POWER - TYPICALLY 70 mW
- POWER-DOWN STANDBY MODE - TYPICALLY 3 mW
- AUTOMATIC POWER-DOWN
- TTL OR CMOS COMPATIBLE DIGITAL INTERFACE
- MAXIMIZES LINE INTERFACE CARD CIRCUIT DENSITY
- IDEAL FOR DIGITAL TELEPHONE SET APPLICATION



DIP16
(Plastic)
ORDER CODES : ETC50S67N
ETC50S64N

PIN CONNECTION

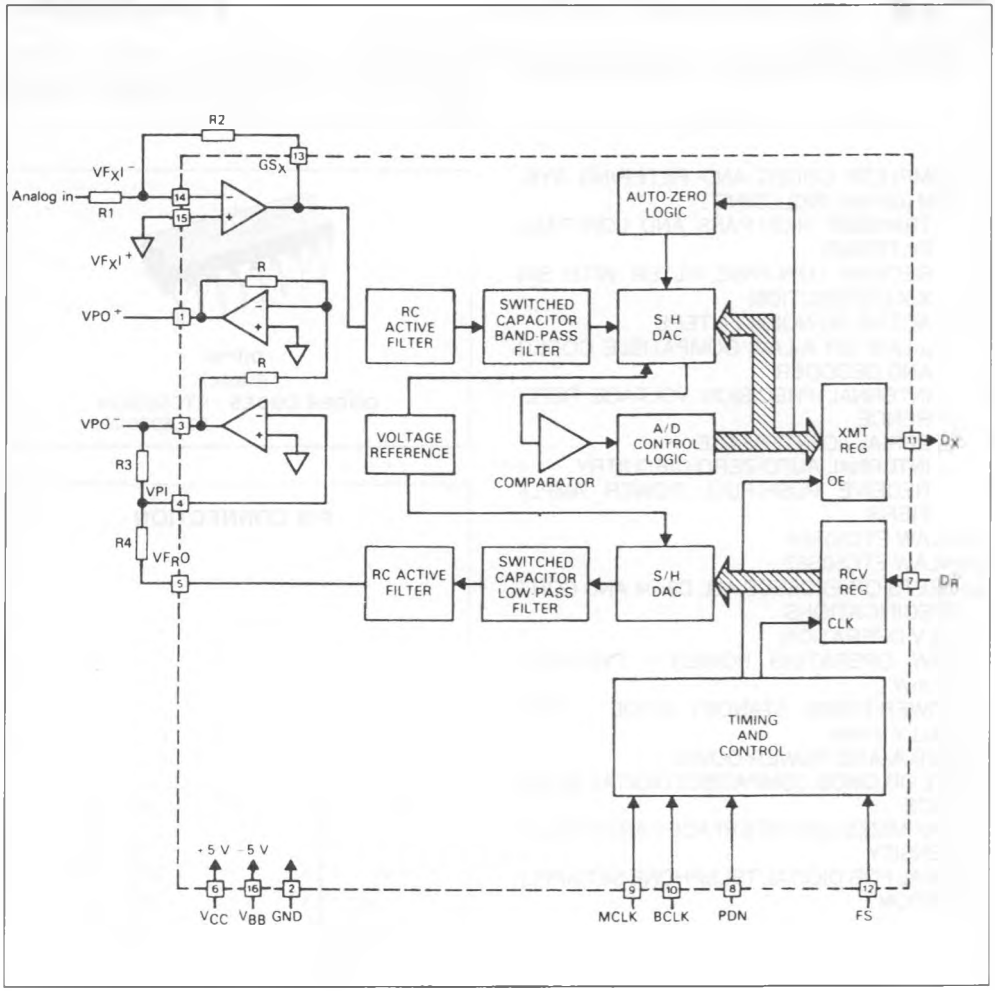


MBBETC50S64-B1

DESCRIPTION

The ETC50S64 (μ-law) and ETC50S67 (A-Law) are synchronous monolithic PCM CODEC/FILTERS utilizing the A/D and D/A conversion architecture shown in the block diagram below, and a serial PCM interface. The devices are fabricated using double-poly CMOS process. Similar to ETC505X - family, these devices feature an additional Receive Power Amplifier to provide push-pull balanced output drive capability. The receive gain can be adjusted by means of two external resistors for an output level of up to ± 6.6 V across a balanced 600 Ω load.

BLOCK DIAGRAM



PIN DESCRIPTION

Name	Pin Type (*)	N°	Description
VPO+	O	1	The Non-inverted Output to the Receive Power Amplifier.
GND	GND	2	Ground. All signals are referenced to this pin.
VPO–	O	3	The Inverted Output of the Receive Power Amplifier.
VPI	I	4	Inverting input to the receive power amplifier. Also powers down both amplifiers when connected to V_{BB}.
VF_RO	O	5	Analog Output of the Receive Filter.
V_{CC}	S	6	Positive Power Supply Pin. V_{CC} = + 5 V ± 5 %.
D_R	I	7	Receive Data Input. PCM data is shifted into D_R following the FS_R leading edge.
PDN	I	8	Power Down Selection. Must be connected continuously low in operation. When PDN is connected continuously high, the device is powered down.
MCLK	I	9	Master Clock. Must be 2.048 MHz for ETC50S67 and 1.536 or 1.544 MHz for ETC50S64.
BCLK	I	10	Bit clock which shifts out the PCM data on D_X and shifts PCM data into DR. May vary from 64 kHz to 2.048 MHz, but must be synchronous with MCLK.
D_X	O	11	The tri-state PCM data output which is enabled by FS.
FS	I	12	Frame sync. pulse, which enables BCLK to shift out the PCM data on DX, and to shift PCM data into DR. FS is a 8KHz pulse train.
GS_X	O	13	Analog Output of the Transmit Input Amplifier. Used to externally set gain.
$VF_XI–$	I	14	Inverting Input of the Transmit Input Amplifier.
VF_XI+	I	15	Non-inverting Input of the Transmit Input Amplifier.
V_{BB}	S	16	Negative Power Supply Pin. V_{BB} = – 5 V ± 5 %.

(*) I : Input, O : Outputs. S : Power supply

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	V_{CC} to GND	7	V
V_{BB}	V_{BB} to GND	– 7	V
V_{IN}, V_{OUT}	Voltage at any Analog Input or Output	V_{CC} + 0.3 to V_{BB} – 0.3	V
	Voltage at any Digital Input or Output	V_{CC} + 0.3 to GND – 0.3	V
T_{oper}	Operating Temperature Range	– 25 to + 125	°C
T_{stg}	Storage Temperature Range	– 65 to + 150	°C
	Lead Temperature (soldering, 10 seconds)	300	°C

FUNCTIONAL DESCRIPTION

POWER-UP

When power is first applied, power-on reset circuitry initializes the COMBO and places it into the power-down mode. All non-essential circuits are deactivated and the D_X and VF_RO outputs are put in high impedance states. To power-up the device, a logical low level or clock must be applied to the PDN pin and FS pulses must be present. Thus, 2 power-down control modes are available. The first is to pull the PDN pin high ; the alternative is to hold FS input continuously low. The device will power-down approximately 2 ms after the last FS pulse. Power-up will occur on the first FS pulse. The TRI-STATE PCM data output, DX, will remain in the high impedance state until the second FS pulse.

OPERATION

A clock must be applied to MCLK (2.048 MHz for ETC50S67, 1.544 or 1.536 for ETC50S64) and the PDN pin can be used as a power-down control. A low level on PDN powers up the device and a high level powers down the device. A bit clock must also be applied to BCLK. For 1.544 MHz operation, the device automatically compensates for the 193rd clock pulse each frame. The bit clock, BCLK may be from 64 kHz to 2.048 MHz, but must be synchronous with MCLK. Each FS pulse begins the encoding cycle and the PCM data from the previous encode cycle is shifted out of the enabled DX output on the positive edge of BCLK. After 8 bit clock periods, the TRI-STATE D_X output is returned to a high impedance state. With an FS pulse. PCM data is latched via the D_R input on the negative edge of BCLK. FS must be synchronous with MCLK.

SHORT FRAME SYNC OPERATION

The COMBO can utilize either a short frame sync pulse or a long frame sync pulse. Upon power initialization, the device assumes a short frame mode. In this mode FS sync pulse must be one bit period long, with timing relationships specified in figure 2. With FS high during a falling edge of BCLK, the next rising edge of BCLK enables the DX TRI-STATE output buffer, which will output the sign bit. The following seven rising edges clock out the remaining seven bits, and the next falling edge disables the DX output. With FS high during a falling edge of BCLK, the next falling edge of BCLK latches in the sign bit. The following seven falling edges latch in the seven remaining bits.

LONG FRAME SYNC OPERATION

To use the long frame mode, FS must be three or more bit clock periods long, with timing relationships specified in figure 3. Based on FS the COMBO will sense whether short or long frame sync pulses are being used. For 64 kHz operation, the frame sync pulse must be kept low for a minimum of 160 ns (see fig. 1). The D_X TRI-STATE output buffer is enabled with the rising edge of FS or the rising edge of BCLK, whichever comes later, and the first bit clocked out is the sign bit. The following seven BCLK rising edges clock out the remaining seven bits. The D_X output is disabled by the falling BCLK edge following the eighth rising edge or by FS going low, whichever comes later. A rising edge on the receive frame sync pulse, FS, will cause the PCM data at D_R to be latched in on the next eight falling edges of BCLK.

TRANSMIT SECTION

The transmit section input is an operational amplifier with provision for gain adjustment using two external resistor, see figure 5. The low noise and wide band-width allow gains in excess of 20 dB across the audio passband to be realized. The op amp drives a unity-gain filter consisting of RC active prefilter, followed by an eighth order switched-capacitor bandpass filter clocked at 256 kHz. The output of this filter directly drives the encoder sample-and-hold circuit. The A/D is of companding type according to A-law (ETC50S67) or μ-law (ETC50S64) coding conventions. A precision voltage reference is trimmed in manufacturing to provide on input overload (t_{MAX}) of nominally 2.5 V peak (see table of Transmission Characteristics). The FS frame sync pulse controls the sampling of the filter output, and then the successive-approximation encoding cycle begins. The 8-bit code is then loaded into a buffer and shifted out through D_X at the next FS pulse. The total encoding delay will be approximately 165 μs (due to the transmit filter) plus 125 μs (due to encoding delay), which totals 290 μs. Any offset voltage due to the filters or comparator is cancelled by sign bit integration.

RECEIVE SECTION

The receive section consists of an expanding DAC which drives a fifth order switched-capacitor low pass filter clocked at 256 kHz. The decoder is A-law (ETC50S67) or μ-law (ETC50S64) and the 5 th order low pass filter corrects for the sin x/x attenuation due to the 8 kHz sample and hold. The filter is then followed by a 2 nd order RC active post-filter and power amplifier capable of driving a 600 Ω load to a level of 7.2 dBm. The receive section is unity-gain. Upon the occurence of FS, the data at the D_R input is clocked in on the falling edge of the next eight BCLK periods. At the end of the decoder time slot, the decoding cycle begins, and 10 μlater the decoder DAC output is updated. The total decoder delay is ~ 10 μs (decoder update) plus 110 μs (filter delay) plus 62.5 μs (1/2 frame), which gives approximately 180 μs.

RECEIVE POWER AMPLIFIERS

Two inverting mode power amplifiers are provided for directly driving a matched line interface transformer. The gain of the first power amplifier can be adjusted to boost the ± 2.5 V peak output signal from the receive filter up ± 3.3 V peak into an unbalanced 300 Ω load, or ± 4.0 V into an unbalanced 15 kΩ

load. The second power amplifier is internally connected in unity-gain inverting mode to give 6 dB of signal gain for balanced loads. Maximum power transfer to a 600 Ω subscriber line termination is obtained by differentially driving a balanced transformer with a $\sqrt{2}$: 1 turns ratio. A total peak power of 15.6 dBm can be delivered to the load plus termination. Both power amplifiers can be powered down independently form the PDN input by connecting the VPI input to V_{BB} saving approximately 12 mW of power.

ELECTRICAL OPERATING CHARACTERISTICS V_{CC} = 5.0 V ± 5 %, V_{BB} = − 5 V ± 5 %, GND = 0 V, T_A = 0 °C to 70 °C (unless otherwise noted) ; typical characteristics specified at V_{CC} = 5.0 V, V_{BB} = − 5.0 V, T_A = 25 °C ; all signals are referenced to GND.

DIGITAL INTERFACE

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{IL}	Input Low Voltage	–	–	0.6	V
V_{IH}	Input High Voltage	2.2	–	–	V
V_{OL}	Output Low Voltage I_{IL} = 3.2 mA D_X	–	–	0.4	V
V_{OH}	Output High Voltage I_H = − 3.2 mA D_X	2.4	–	–	V
I_{IL}	Input Low Current (GND ≤ V_{IN} ≤ V_{IL} all digital inputs except BCLK)	− 10	–	10	µA
I_{IH}	Input High Current (V_{IH} ≤ V_{IN} ≤ V_{CC})	− 10	–	10	µA
I_{OZ}	Output Current in High Impedance State (TRI-STATE) (GND ≤ V_O ≤ V_{CC}) D_X	− 10	–	10	µA

ANALOG INTERFACE WITH TRANSMIT INPUT AMPLIFIER (all devices)

Symbol	Parameter	Min.	Typ.	Max.	Unit
I_IXA	Input Leakage Current (− 2.5 V ≤ V ≤ + 2.5 V) VF_XI^+ or VF_XI^-	− 200	–	200	nA
R_IXA	Input Resistance (− 2.5 V ≤ V ≤ + 2.5 V) VF_XI^+ or VF_XI^-	10	–	–	MΩ
R_OXA	Output Resistance (closed loop, unity gain)	–	1	3	Ω
R_LXA	Load Resistance GS_X	10	–	–	kΩ
C_LXA	Load Capacitance GS_X	–	–	50	pF
V_OXA	Output Dynamic Range (R_L ≥ 10 kΩ) GS_X	± 2.8	–	–	V
A_VXA	Voltage Gain (VF_XI^+ to GS_X)	5000	–	–	V/V
F_UXA	Unity Gain Bandwidth	1	2	–	MHz
$V_{OS}XA$	Offset Voltage	− 20	–	20	mV
$V_{CM}XA$	Common-mode Voltage	− 2.5	–	2.5	V
CMRRXA	Common-mode Rejection ratio	60	–	–	dB
PSRRXA	Power Supply Rejection Ratio	60	–	–	dB

ANALOG INTERFACE WITH RECEIVE FILTER (all devices)

Symbol	Parameter	Min.	Typ.	Max.	Unit
R_ORF	Output Resistance VF_RO	–	1	3	Ω
R_LRF	Load Resistance (VF_RO = ± 2.5 V)	10	–	–	kΩ
C_LRF	Load Capacitance	–	–	25	pF
VOS_RO	Output DC Offset Voltage	− 200	–	200	mV

ELECTRICAL OPERATING CHARACTERISTICS (continued)

ANALOG INTERFACE WITH POWER AMPLIFIERS (all devices)

Symbol	Parameter	Min.	Typ.	Max.	Unit
IPI	Input Leakage Current (– 1.0 V ≤ VPI ≤ 1.0 V)	– 100	–	100	nA
RIPI	Input Resistance (– 1.0 V ≤ VPI ≤ 1.0 V)	10	–	–	MΩ
VIOS	Input Offset Voltage	– 25	–	25	mV
ROP	Output Resistance (inverting unity-gain at VPO^+ or VPO^-)	–	1	–	Ω
F_C	Unity-gain Bandwidth, open loop (VPO^-)	–	400	–	kHz
$C_L P$	Load Capacitance (VPO^+ or VPO^- to GND) $R_L \geq 1500\ \Omega$ $R_L = 600\ \Omega$ $R_L = 300\ \Omega$	 – – –	 – – –	 100 500 1000	pF
GAp+	Gain VPO– to VPO^+ to GND, Level at VPO^- = 1.77 Vrms (+ 3 dBmO)	–	– 1	–	V/V
PSRRp	Power Supply Rejection of V_{CC} or V_{BB} (VPO^- connected to VPI) 0 kHz - 4 kHz 0 kHz - 50 kHz	 60 36	 – –	 – –	dB

POWER DISSIPATION (all devices)

Symbol	Parameter	Min.	Typ.	Max.	Unit
$I_{CC}0$	Power-Down Current	–	0.5	2.0	mA
$-I_{BB}0$	Power-Down Current	–	0.05	0.5	mA
$-I_{CC}1$	Active Current	–	7.0	12.0	mA
$I_{BB}1$	Active Current	–	7.0	12.0	mA

TIMING SPECIFICATIONS. All timing parameters are measured at V_{OH} = 2.0 V and V_{OL} = 0.7 V. See "definitions" and "timing conventions" section for test method information.

Symbol	Parameter		Min.	Typ.	Max.	Unit
$1/t_{PM}$	Frequency of Master Clock ETC50S64 ETC50S67	MCLK	– – –	1.536 1.544 2.048	– – –	MHz
t_{WMH}	Width of Master Clock High	MCLK	160	–	–	ns
t_{WML}	Width of Master Clock Low	MCLK	160	–	–	ns
t_{RM}	Rise Time of Master Clock	MCLK	–	–	50	ns
t_{FM}	Fall Time of Master Clock	MCLK	–	–	50	ns
t_{PB}	Period of Bit Clock		485	488	15.725	ns
t_{WBH}	Width of Bit Clock High (V_{IH} = 2.2 V)		160	–	–	ns
t_{WBL}	Width of Bit Clock Low (V_{IL} = 0.6 V)		160	–	–	ns
t_{RB}	Rise Time of Bit Clock (t_{PB} = 488 ns)		–	–	50	ns
t_{FB}	Fall Time of Bit Clock (t_{PB} = 488 ns)		–	–	50	ns
t_{SBFM}	Set-up time from BCLK high to MCLK falling edge (first bit clock after the leading edge of FS)		100	–	–	ns
t_{HBF}	Holding Time from Bit Clock Low to the Frame Sync (long frame only)		0	–	–	ns
t_{SFB}	Set-up Time from Frame Sync to Bit Clock Low (long frame only)		80	–	–	ns
t_{HBFI}	Hold Time from 3rd Period of Bit Clock Low to Frame Sync (long frame only)	FS	100	–	–	ns
t_{DZF}	Delay Time to Valid Data from FS or BCLK Whichever Comes Later and Delay Time from FS to Data Output Disabled (C_L = 0 pF to 150 pF)		20	–	165	ns
t_{DBD}	Delay Time from BCLK High to Data Valid (load = 150 pF plus 2 LSTTL loads)		0	–	180	ns
t_{DZC}	Delay Time from BCLK Low to Data Output Disabled		50	–	165	ns
t_{SDB}	Set-up Time from D_R Valid to BCLK Low		50	–	–	ns
t_{HBD}	Hold Time from BCLK Low to D_R Invalid		50	–	–	ns
t_{HOLD}	Holding Time from Bit Clock High to Frame Sync (short frame only)		0	–	–	ns
t_{SF}	Set-up Time from FS to BCLK Low (short frame sync pulse) - Note 1		80	–	–	ns
t_{HF}	Hold Time from BCLK Low to FS Low (short frame sync pulse) Note 1		100	–	–	ns
t_{WFL}	Minimum Width of the Frame Sync Pulse (low level) (64k bit/s operating mode)		160	–	–	ns

Note : 1. For short frame sync timing FS must go high while bit clock is high.

Figure 1 : 64 k bits/s TIMING DIAGRAM.

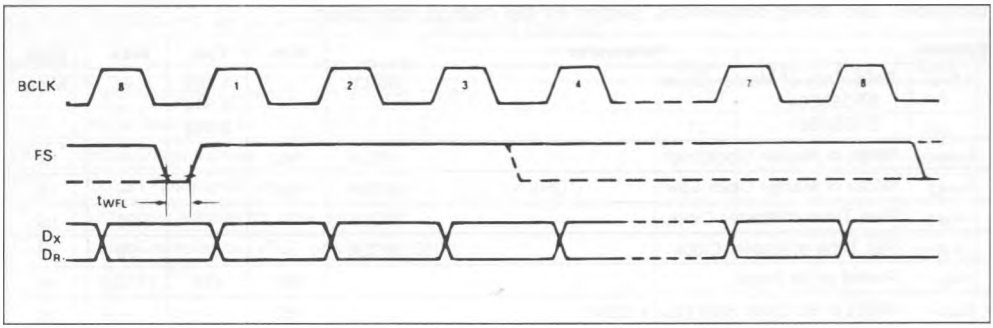


Figure 2 : Short Frame Sync Timing.

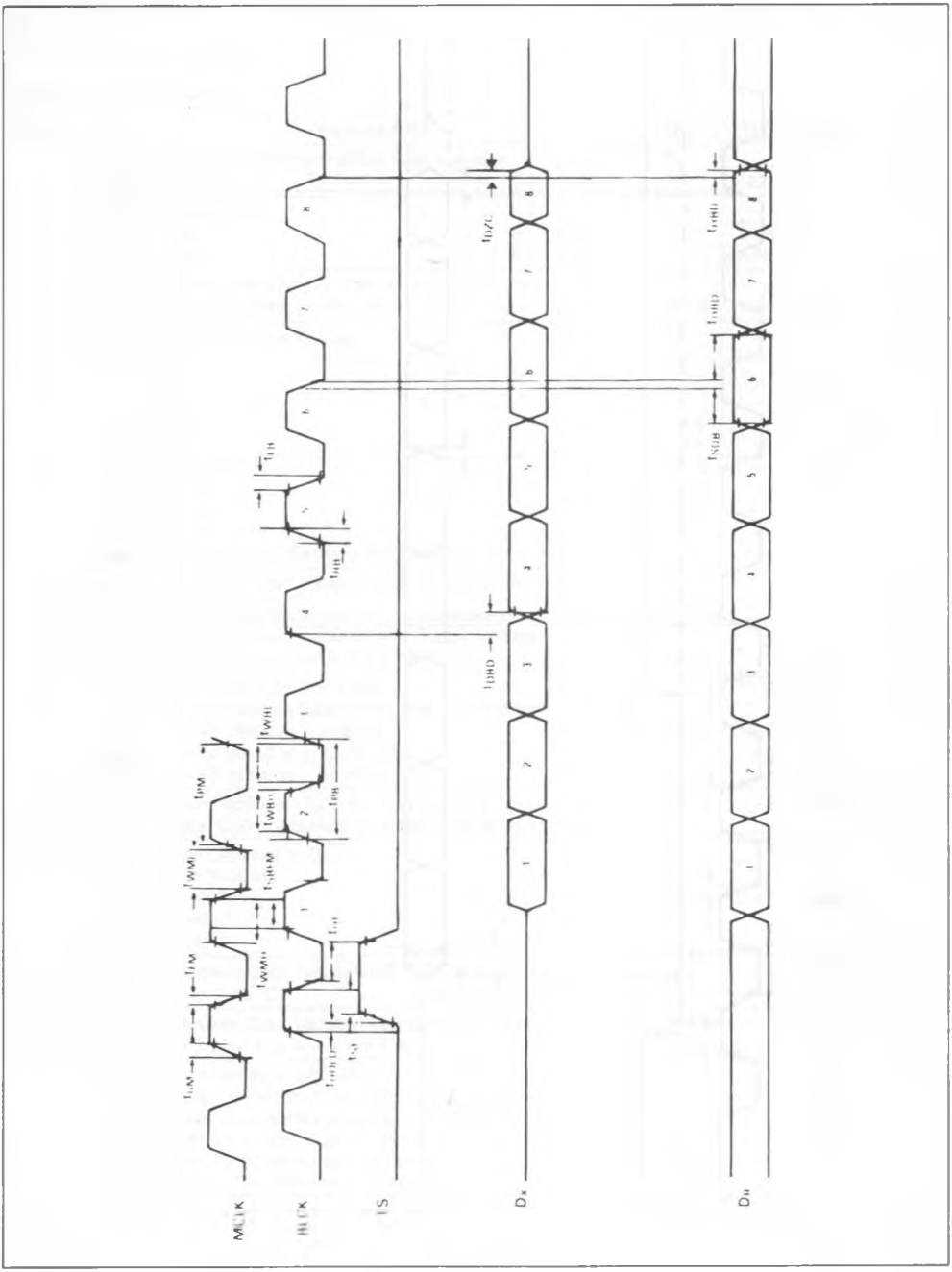
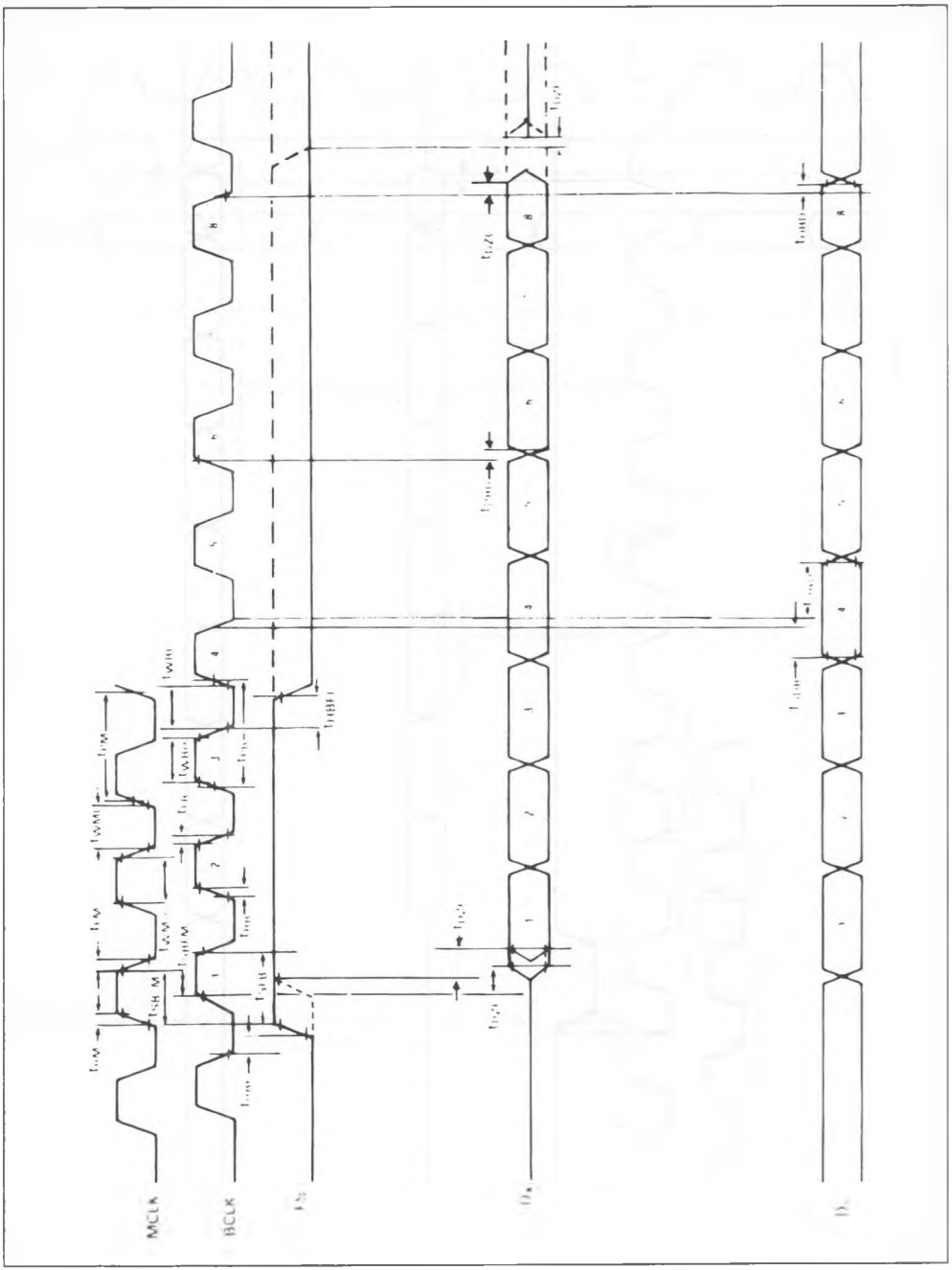


Figure 3 : Long Frame Sync Timing.



TRANSMISSION CHARACTERISTICS (all devices) T_A = 0 °C to 70 °C, V_{CC} = 5 V ± 5 %, V_{BB} = − 5 V ± 5 %, GND = 0 V, f = 1.02 kHz, V_{IN} = 0 dBm0 transmit input amplifier connected for unity-gain non-inverting.
(unless otherwise specified)

AMPLITUDE RESPONSE

Symbol	Parameter	Min.	Typ.	Max.	Unit
	Absolute Levels - Nominal 0 dBm0 level is 4 dBm (600 Ω) 0 dBm0	–	1.2276	–	Vrms
t_{MAX}	Max Overload Level				V_{PK}
	3.14 dBm0 ETC50S67	–	2.492	–	
	3.17 dBm0 ETC50S64	–	2.501	–	
G_{XA}	Transmit Gain, Absolute (T_A = 25 °C, V_{CC} = 5 V, V_{BB} = − 5 V) Input at GS_X = 0 dBm0 at 1020 Hz	− 0.15	–	0.15	dB
G_{XR}	Transmit Gain, Relative to G_{XA}				dB
	f = 16 Hz	–	–	− 40	
	f = 50Hz	–	–	− 30	
	f = 60 Hz	–	–	− 26	
	f = 180 Hz	− 2.8	–	− 0.2	
	f = 200 Hz	− 1.8	–	− 0.1	
	f = 300 Hz-3000Hz	− 0.15	–	0.15	
	f = 3300 Hz	− 0.35	–	0.05	
	f = 3400 Hz	− 0.7	–	0	
	f = 4000 Hz	–	–	− 14	
	f = 4600 Hz and up, measure reponse from 0Hz to 4000 Hz	–	–	− 32	
G_{XAT}	Absolute Transmit Gain Variation with Temperature (T_A = 0 °C to + 70 °C)	− 0.1	–	0.1	dB
G_{XAV}	Absolute Transmit Gain Variation with Supply Voltage (V_{CC} = 5 V ± 5 %, V_{BB} = − 5 V ± 5 %)	− 0.05	–	− 0.05	dB
G_{XRL}	Transmit Gain Variation with Level Sinusoidal Test Method Reference Level = − 10 dBm0				dB
	VF_XI^+ = − 40 dBm0 to + 3 dBm0	− 0.2	–	0.2	
	VF_XI^+ = − 50 dBm0 to − 40 dBm0	− 0.4	–	0.4	
	VF_XI^+ = − 55 dBm0 to − 50 dBmo	− 1.2	–	1.2	
G_{RA}	Receive Gain, Absolute (T_A = 25 °C, V_{CC} = 5 V, V_{BB} = − 5 V) Input = Digital Code Sequence for 0dBm0 Signal at 1020 Hz	− 0.15	–	0.15	dB
G_{RR}	Receive Gain, relative to G_{RA}				dB
	f = 0 Hz to 3000 Hz	− 0.15	–	0.15	
	f = 3300 Hz	− 0.35	–	0.05	
	f = 3400 Hz	− 0.7	–	0	
	f = 4000 Hz	–	–	− 14	
G_{RAT}	Absolute Receive Gain Variation with Temperature (T_A = 0 °C to + 70 °C)	− 0.1	–	0.1	dB
G_{RAV}	Absolute Receive Gain Variation with Supply Voltage (V_{CC} = 5 V ± 5 %, V_{BB} = − 5 V ± 5 %)	− 0.05	–	0.05	dB
G_{RRL}	Receive Gain Variation with Level Sinusuoidal Test Method ; reference input PCM code corresponds to an ideally encoded − 10 dBm0 signal				dB
	PCM Level = − 40 dBm0 to + 3 dBm0	− 0.2	–	0.2	
	PCM Level = − 50 dBm0 to − 40 dBm0	− 0.4	–	0.4	
	PCM Level = − 55 dBm0 to − 50 dBm0	− 1.2	–	1.2	
V_{RO}	Receive Filter Output at VF_RO, R_L = 10 kΩ	− 2.5	–	2.5	V

TRANSMISSION CHARACTERISTICS (continued)

ENVELOPE DELAY DISTORTION WITH FREQUENCY

Symbol	Parameter	Min.	Typ.	Max.	Unit
D_{XA}	Transmit Delay, Absolute (f = 1600 Hz)	–	290	315	µs
D_{XR}	Transmit Delay, Relative to D_{XA}				µs
	f = 500 Hz-600 Hz	–	195	220	
	f = 600 Hz-800 Hz	–	120	145	
	f = 800 Hz-1000 Hz	–	50	75	
	f = 1000 Hz-1600 Hz	–	20	40	
	f = 1600 Hz-2600Hz	–	55	75	
	f = 2600 Hz-2800 Hz	–	80	105	
	f = 2800 Hz-3000 Hz	–	130	155	
D_{RA}	Receive Delay, Absolute (f = 1600 Hz)	–	180	200	µs
D_{RR}	Receive Delay, Relative to D_{RA}				µs
	f = 500 Hz-1000 Hz	– 40	– 25	–	
	f = 1000 Hz-1600 Hz	– 30	– 20	–	
	f = 1600 Hz-2600 Hz	–	70	90	
	f = 2600 Hz-2800 Hz	–	100	125	
	f = 2800 Hz-3000 Hz	–	145	175	

NOISE

Symbol	Parameter	Min.	Typ.	Max.	Unit
N_{XP}	Transmit Noise, P Message Weighted (ETC50S67, VF_XI^+ = 0 V)	–	– 74	– 67 (note 1)	dBm0p
N_{RP}	Receive Noise, P Message Weighted (ETC50S67, PCM code equals positive zero)	–	– 82	– 79	dBm0p
N_{XC}	Transmit Noise, C Message Weighted (ETC50S64, VFXI+ = 0 v)	–	12	15	dBmCO
N_{RC}	Receive Noise, C Message Weighted (ETC50S64, PCM code equals alternating positive and negative zero)	–	8	11	dBmC0
N_{RS}	Noise, Single Frequency f = 0 kHz to 100 kHz, Loop around Measurement, VF_XI^+ = 0 V	–	–	– 53	dBm0
$PPSR_X$	Positive Power Supply Rejection, Transmit (note 2) V_{CC} = 5.0 V_{DC} + 100 mVrms, f = 0 kHz-50 kHz	40	–	–	dBp
$NPSR_X$	Negative Power Supply Rejection, Transmit (note 2) V_{BB} = – 5.0 V_{DC} + 100 mVrms, f = 0 kHz-50 kHz	40	–	–	dBp
$PPSR_R$	Positive Power Supply Rejection, receive (PCM code equals positive zero, V_{CC} = 5.0 V_{DC} + 100 mVrms)				
	f = 0 Hz-4000Hz	40	–	–	dBp
	f = 4 kHz-25 kHz	40	–	–	dB
	f = 25 kHz-50 kHz	36	–	–	dB
$NPSR_R$	Negative Power Supply Rejection, receive (PCM code equals positive zero, V_{BB} = – 5.0 V_{DC} + 100 mVrms) f = 0 Hz-4000Hz				
	f = 4 kHz-25 kHz	40	–	–	dBp
	f = 25 kHz-50 kHz	40	–	–	dB
		36	–	–	dB
SOS	Spurious out-of-band Signals at the Channel Output Loop around measurement, 0 dBm0, 300 Hz-3400 Hz input applied to DR, measure individual image signals at DX				
	4600 Hz-7600 Hz	–	–	– 32	dB
	7600 Hz-8400 Hz	–	–	– 40	dB
	8400 Hz-100,000 Hz	–	–	– 32	dB

TRANSMISSION CHARACTERISTICS (continued)

DISTORTION

Symbol	Parameter		Min.	Typ.	Max.	Unit
STD_X or STD_R	Signal to Total Distortion (sinusoidal test method)					dBp
	Transmit or Receive Half-channel					
	Level = 3.0 dBm0		33	–	–	
	= 0 dBm0 to – 30 dBm0		36	–	–	
	= – 40 dBm0	XMT	29	–	–	
		RCV	30	–	–	
	= – 55 dBm0	XMT	14	–	–	
		RCV	15	–	–	
SFD_X	Single Frequency Distortion, transmit		–	–	– 46	dB
SFD_R	Single Frequency Distortion, receive		–	–	– 46	dB
IMD	Intermodulation Distortion Loop Around Measurement, $VF_XI+ = -4$ dBm0 to – 21 dBm0, two Frequencies in the Range 300 Hz-3400 Hz		–	–	– 41	dB

CROSSTALK

Symbol	Parameter	Min.	Typ.	Max.	Unit
CT_{X-R}	Transmit to Receive Crosstalk, 0dBm0 Transmit f = 300 Hz-3400 Hz, D_R = Steady PCM Code	–	– 90	– 75	dB
CT_{R-X}	Receive to Transmit Crosstalk, 0dBm0 Receive Level f = 300 Hz-3400 Hz, VF_XI = 0 V	–	– 90	– 70 (note 2)	dB

POWER AMPLIFIERS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{OL}	Maximum 0 dBm0 Level for better than ± 0.1 dB Linearity over the Range 10 dBm0 to + 3 dBm0 (balanced load, R_L connected between VPO^+ and VPO)				Vrms
	R_L = 600 Ω	33	–	–	
	R_L = 1200 Ω	3.5	–	–	
	R_L = 30 kΩ	4.0	–	–	
S/D_P	Signal/Distortion R_L = 600 Ω, 0dBm0	50	–	–	dB

Notes : 1. Measured by extrapolation from the distortion test result.
2. PPSRX, NPSRX, CTR-X measured with a - 50 dBmO activating signal applied at VFxI+.

ENCODING FORMAT AT D_X OUTPUT

	A-Law (including even bit inversion)	μLaw
V_{IN} (at GS_X) = + Full-scale	1 0 1 0 1 0 1 0	1 0 0 0 0 0 0 0
V_{IN} (at GS_X) = 0 V	1 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1	1 1 1 1 1 1 1 1 0 1 1 1 1 1 1 1
V_{IN} (at GS_X) = – Full-scale	0 0 1 0 1 0 1 0	0 0 0 0 0 0 0 0

APPLICATION INFORMATION

POWER SUPPLIES

While the pins at the ETC5056 family are well protected against electrical misure, it is recommended that the standard CMOS practice be followed, ensuring that ground is connected to the device before any other connections are made. In applications where the printed circuit board may be plugged into a "hot" socket with power and clocks already present, an extra long ground pin in the connector should be used.

All ground connections to each device should meet at a common point as close as possible to the GND pin. This minimizes the interaction of ground return currents flowing through a common bus impedance. 0.1 µF supply decoupling capacitors should be connected from this common ground point to V_{CC} and V_{BB} as close to the device as possible.

For best performance, the ground point of each CODEC/FILTER on a card should be connected to a common card ground in star formation, rather than via a ground bus. This common ground point should be decoupled to V_{CC} and V_{BB} with 10 µF capacitors.