RSL10 SIP

Product Preview

Bluetooth® 5 System-in-Package (SiP)

Introduction

RSL10 System−In−Package (RSL10 SIP) is a complete solution that provides the easiest way to integrate the industry's lowest power Bluetooth low energy technology into a wireless application.

The RSL10 SIP features an on−board antenna, RSL10 radio SoC, and all necessary passive components in one package to help minimize overall system size. Already fully qualified to FCC, CE, and other regulatory standards; RSL10 SIP removes the need for additional antenna design considerations or RF certifications.

Key Features

- Fully Certified:
  - Bluetooth 5
  - QDID
  - Declaration ID
  - FCC, CE, IC, MIC, KC
- Industry's Lowest Power:
  - Peak Rx Current = 5.6 mA (1.25 V VBAT)
  - Peak Rx Current = 3.0 mA (3 V VBAT)
  - Peak Tx Current (0 dBm) = 8.9 mA (1.25 V VBAT)
  - Peak Tx Current (0 dBm) = 4.6 mA (3 V VBAT)
- Deep Sleep Current Consumption (1.25 V VBAT):
  - Deep Sleep, IO Wake−up: 50 nA
  - Deep Sleep, 8 kB RAM Retention: 300 nA
- Current Consumption (3 V VBAT):
  - Deep Sleep, IO Wake−up: 25 nA
  - Deep Sleep, 8 kB RAM Retention: 100 nA
- EEMBC ULPMark Core Profile (3 V): 1090
- EEMBC ULPMark Core Profile (2.1 V): 1360
- Advanced Wireless:
  - Supports Bluetooth Low Energy Technology and 2.4 GHz Custom Protocols
  - Supports FOTA (Firmware Over−The−Air) Updates
  - Rx Sensitivity (Bluetooth Low Energy Mode, 1 Mbps): −94 dB
  - Transmitting Power: −17 to +6 dBm

Other Key Features

- Arm Cortex−M3 Processor Clocked at up to 48 MHz
- Supply Voltage Range: 1.1 – 3.3 V
- 384 kB of Flash Memory
- 76 kB of Program Memory
- 88 kB of Data Memory

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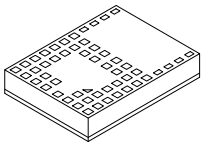


SIP51 8x6
CASE 127EY

(SIP51)

XXXXXX	= Specific Device Code
A	= Assembly Location
WL	= Wafer Lot
Y	= Year
WW	= Work Week
G or ▪	= Pb−Free Package

ORDERING INFORMATION

Device	Package	Shipping†
NCH−RSL10−101S51−ACG	SIP51 (Pb−Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

FEATURES

- **Arm Cortex−M3 Processor:** A 32−bit core for real−time applications, specifically developed to enable high−performance low−cost platforms for a broad range of low−power applications.
- **LPDSP32:** A 32−bit Dual Harvard DSP core that efficiently supports intensive signal processing applications. Various codecs are available to customers through libraries that are included in RSL10's development tools.
- **Radio Frequency Front−End:** Based on a 2.4 GHz RF transceiver, the RFFE implements the physical layer of the Bluetooth low energy technology standard and other proprietary or custom protocols.
- **Protocol Baseband Hardware:** Bluetooth 5 certified and includes support for a 2 Mbps RF link and custom protocol options. The RSL10 baseband stack is supplemented by support structures that enable implementation of ON Semiconductor and customer designed custom protocols.
- **Highly−Integrated SoC:** The dual−core architecture is complemented by high−efficiency power management units, oscillators, flash and RAM memories, a DMA controller, along with a full complement of peripherals and interfaces.
- **Deep Sleep Mode:** RSL10 can be put into a Deep Sleep Mode when no operations are required. Various Deep Sleep Mode configurations are available, including:
  - "IO wake−up" configuration. The power consumption in deep sleep mode is 50 nA (1.25 V VBAT).
  - Embedded 32 kHz oscillator running with interrupts from timer or external pin. The total current drain is 90 nA (1.25 V VBAT).
  - As above with 8 kB RAM data retention. The total current drain is 300 nA (1.25 V VBAT).
  - With the exception of IO wake up only configuration, the on−chip buck converter can also be enabled to reduce current consumption in Deep Sleep Mode (at higher VBAT voltages).
- **Standby Mode:** Can be used to reduce the average power consumption for off−duty cycle operation, ranging typically from a few ms to a few hundreds of ms. The typical chip power consumption is 30 μA in Standby Mode.
- **Multi−Protocol Support:** Using the flexibility provided by LPDSP32, the Arm Cortex−M3 processor, and the RF front−end; proprietary protocols and other custom protocols are supported.
- **Flexible Supply Voltage:** RSL10 integrates high−efficiency power regulators and has a VBAT range of 1.1 to 3.3 V.
- **Highly Configurable Interfaces:** , UART, two SPI interfaces, PCM interface, multiple GPIOs. It also supports a digital microphone interface (DMIC) and an output driver (OD).
- **Flexible Clocking Scheme:** RSL10 must be clocked from the XTAL/PLL of the radio front−end at 48 MHz when transmitting or receiving RF traffic. When RSL10 is not transmitting/receiving RF traffic, it can run off the 48 MHz XTAL, the internal RC oscillators, the 32 kHz oscillator, or an external clock. A low frequency RTC clock at 32 kHz can also be used in Deep Sleep Mode. It can be sourced from either the internal XTAL, the RC oscillator, or a digital input pad.
- **Diverse Memory Architecture:** 76 kB of SRAM program memory and 88 kB of SRAM data memory are available. A total of 384 kB of flash is available to store the Bluetooth stack and other applications. The Arm Cortex−M3 processor can execute from SRAM and/or flash.
- **IP Protection Feature:** Ensures that the customer's flash contents cannot be copied by a third party. It prevents any core or memory from being accessed externally after the chip has booted.
- **Ultra−Low Power Consumption Application Examples:**
  - Low Duty Cycle Advertising: IDD 1.1 μA for advertising at all three channels at 5 second intervals @ VBAT 3 V, DCDC converter enabled.
- **RoHS Compliant Device**

Notice

All specifications for the RSL10 System−in−Package are based on the RSL10 radio SoC. The RSL10 SIP data sheet only contains key parameters. For a full list of RSL10 parameters and specifications, refer to the RSL10 data sheet.

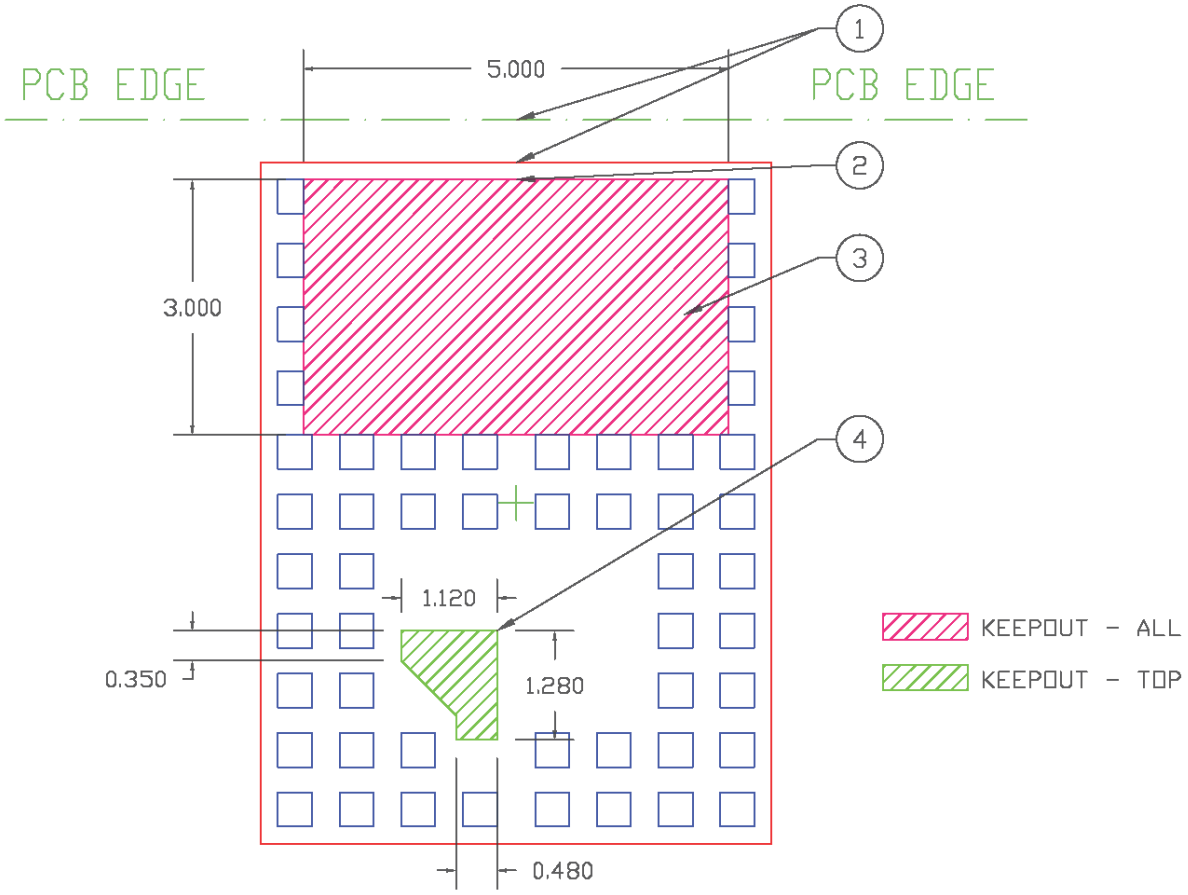
Application Board Connection

The RSL10 SIP is designed to be reflowed onto low−cost printed circuit boards. The RSL10 SIP connects to the application board via solder pads located on the bottom.

To properly operate the RSL10 SIP an external PCB connection between the RF and ANT pads is required. This connection connects the RF pin on RSL10 to the antenna inside the SiP. If an external antenna is used instead of the antenna internal to the SiP, this external antenna needs to be connected to PIN E1.

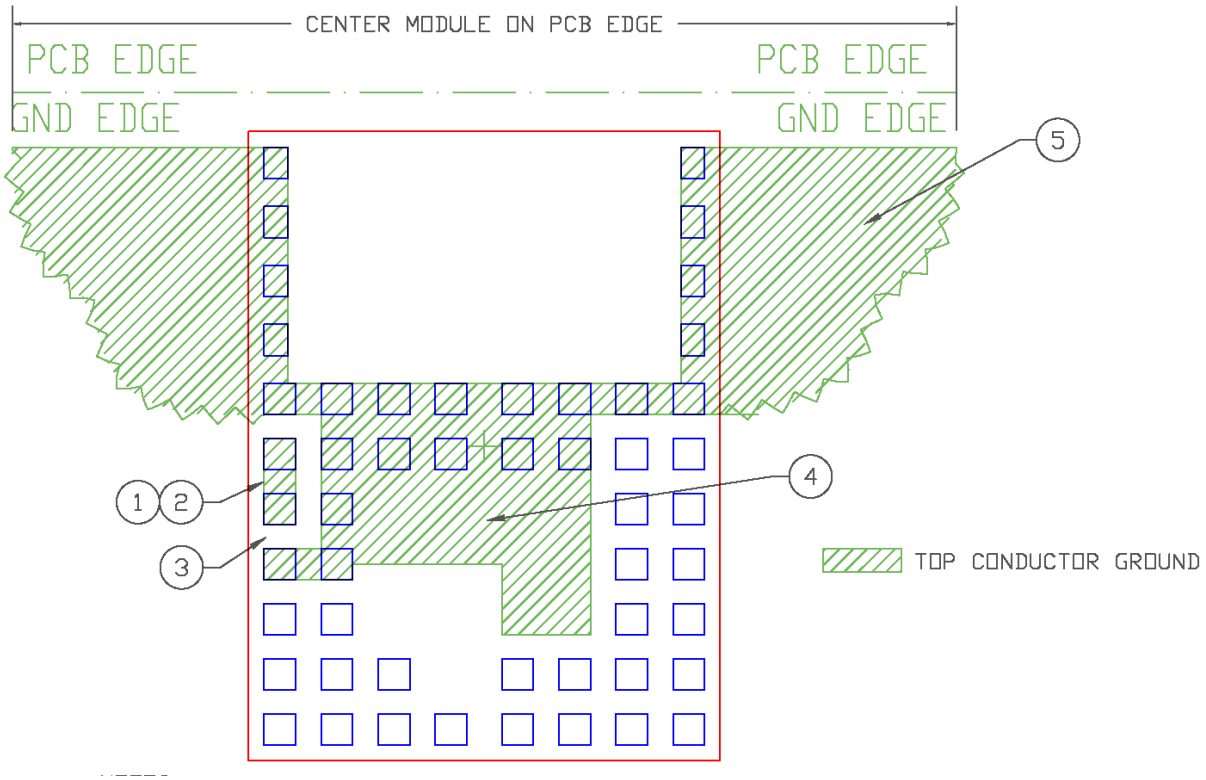
Additionally, an external PCB connection between the VDDO and VBAT pads is required. This connection ensures that the logic high level for the digital I/O (DIO) pads is equal to VBAT.

Figures 1 and 2 show proposed layout patterns for the RSL10 SIP. The specific layout pattern used in the application may have to be adjusted to meet certain needs of the PCB manufacturer or assembly house. PCB design files for the RSL10 SIP are available at www.onsemi.com.



Notes:
1. Align component edge to PCB edge if possible.
2. Extend keepout area to PCB edge.
3. Keepout area− All layers.
4. Keepout area− Top layer only.
5. Units = MM.

Figure 1. RSL10 SIP Keepout Area Requirements



Notes:
1. When incorporating internal antenna, join landing pads using 0.40 x 1.10 shape.
2. Establish 50 (Ohm symbol) impedance to underlying reference plane.
3. Maintain minimum 300 (uM symbol) distance from ground plane.
4. Area for several vias.
5. Refer to radiation efficiency data for applicable ground plane sizing,
6. Units = MM.

Figure 2. Minimum Top Layer Ground Structure

RSL10 SiP Schematic

The schematic for the RSL10 SIP is shown in Figure 3.

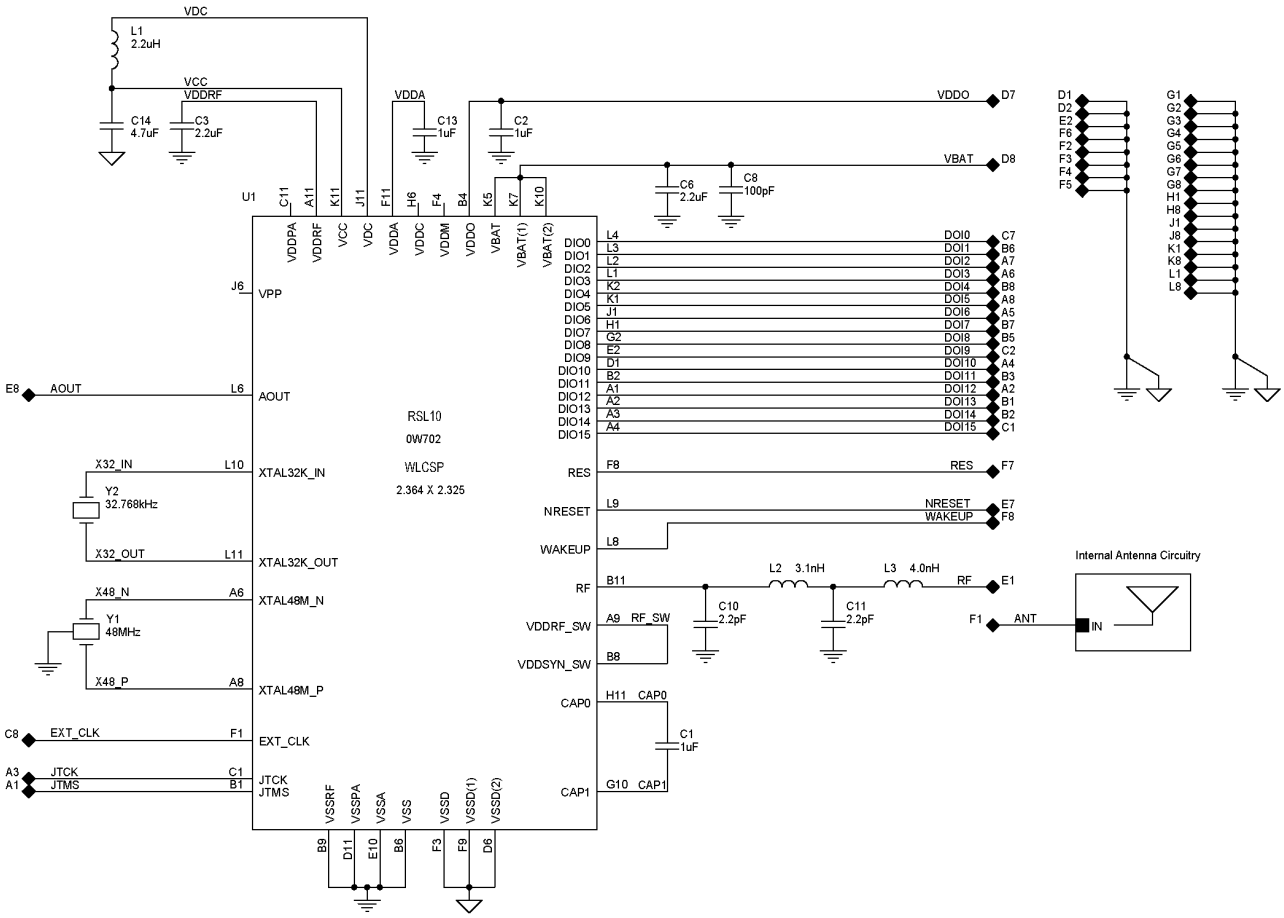


Figure 3. RSL10 SIP Schematic

PAD FUNCTION DESCRIPTION

For detailed pad function information see the RSL10 data sheet.

Table 1. PAD LIST

Pad Identifier	Pad Name	I/O	A/D	Pull	Description
A1	JTMS	I/O	D	U	CM3−JTAG Test Mode State
A2	DOI12	I/O	D	U/D	Digital input output 12
A3	JTCK	I/O	D	U	CM3−JTAG Test Clock
A4	DOI10	I/O	D	U/D	Digital input output 10
A5	DOI6	I/O	D	U/D	Digital input output 6
A6	DOI3	I/O	A/D	U/D	Digital input output 3 / ADC 3
A7	DOI2	I/O	A/D	U/D	Digital input output 2 / ADC 2
A8	DOI5	I/O	D	U/D	Digital input output 5
B1	DOI13	I/O	D	U/D	Digital input output/CM3−JTAG Test Reset
B2	DOI14	I/O	D	U/D	Digital input output/CM3−JTAG Test Data In
B3	DOI11	I/O	D	U/D	Digital input output 11
B5	DOI8	I/O	D	U/D	Digital input output 8
B6	DOI1	I/O	A/D	U/D	Digital input output 1 / ADC 1
B7	DOI7	I/O	D	U/D	Digital input output 7
B8	DOI4	I/O	D	U/D	Digital input output 4
C1	DOI15	I/O	D	U/D	Digital input output/CM3−JTAG Test Data Out
C2	DOI9	I/O	D	U/D	Digital input output 9
C7	DOI0	I/O	A/D	U/D	Digital input output 0 / ADC 0
C8	EXT_CLK	I	D	U	External clock input
D1	DGND	I/O	P		Ground
D2	DGND	I/O	P		Ground
D7	VDDO	I	P		Digital O/I voltage supply
D8	VBAT	I	P		Battery input voltage
E1	RF	I/O	A		RF signal input/output
E2	DGND	I/O	P		Ground
E7	NRESET	I	D	U	Reset pin
E8	AOUT	O	A		Analog test pin
F1	ANT	I/O	A		Antenna
F2	DGND	I/O	P		Ground
F3	DGND	I/O	P		Ground
F4	DGND	I/O	P		Ground
F5	DGND	I/O	P		Ground
F6	DGND	I/O	P		Ground
F7	RES	I	D	D	RESERVED
F8	WAKEUP	I	A		Wake−up pin for power modes
G1	DGND	I/O	P		Ground
G2	DGND	I/O	P		Ground
G3	DGND	I/O	P		Ground
G4	DGND	I/O	P		Ground
G5	DGND	I/O	P		Ground

Table 1. PAD LIST

Pad Identifier	Pad Name	I/O	A/D	Pull	Description
G6	DGND	I/O	P		Ground
G7	DGND	I/O	P		Ground
G8	DGND	I/O	P		Ground
H1	DGND	I/O	P		Ground
H8	DGND	I/O	P		Ground
J1	DGND	I/O	P		Ground
J8	DGND	I/O	P		Ground
K1	DGND	I/O	P		Ground
K8	DGND	I/O	P		Ground
L1	DGND	I/O	P		Ground
L8	DGND	I/O	P		Ground

Table 2. ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Min	Max	Unit
VBAT	Power supply voltage	–	3.63	V
VDDO	I/O supply voltage	–	3.63	V
VSSRF	RF front−end ground	−0.3	–	V
VSSA	Analog ground	−0.3	–	V
VSSD	Digital core and I/O ground	−0.3	–	V
Vin	Voltage at any input pin	VSSD−0.3	VDDO + 0.3	V
T functional	Functional temperature range	−40	85	°C
T storage	Storage temperature range	−40	85	°C
Caution: Class 2 ESD Sensitivity, JESD22−A114−B (2000 V) The QFN package meets 450 V CDM level				

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

Table 3. RECOMMENDED OPERATING CONDITIONS

Description	Symbol	Conditions	Min	Typ	Max	Units
Supply voltage operating range	VBAT	Input supply voltage on VBAT pin (Note 1)	1.18	1.25	3.3	V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

1. In order to be able to use a VBAT Min of 1.1 V, the following reduced operating conditions should be observed:
   – Maximum Tx power 0 dBm.
   – SYSCLK ≤ 24 MHz.
   – Functional temperature range limited to 0−50 deg C
   The following trimming parameters should be used:
   – VCC = 1.10 V
   – VDDC = 0.92 V
   – VDDM = 1.05 V, will be limited by VCC at end of battery life
   – VDDRF = 1.05 V, will be limited by VCC at end of battery life. VDDPA should be disabled
   RSL10 should enter in end−of−battery−life operating mode if VCC falls below 1.03 V. VCC will remain above 1.03 V if VBAT ≥ 1.10 V under the restricted operating conditions described above.

Table 4. ELECTRICAL PERFORMANCE SPECIFICATIONS

Unless otherwise noted, the specifications mentioned in the table below are valid at 25°C at VBAT = VDDO = 1.25 V.

Description	Symbol	Conditions	Min	Typ	Max	Units
OVERALL						
Current consumption RX, V_{BAT} = 1.25 V, low latency	I_{VBAT}		–	1.8	–	mA
Current consumption TX, V_{BAT} = 1.25 V, low latency	I_{VBAT}		–	1.8	–	mA
Current consumption RX, V_{BAT} = 1.25 V	I_{VBAT}		–	1.15	–	mA
Deep sleep current, example 1, V_{BAT} = 1.25 V	Ids1	Wake up from wake up pin.	–	50	–	nA
Deep sleep current, example 2, V_{BAT} = 1.25 V	Ids2	Embedded 32 kHz oscillator running with interrupts from timer or external pin.	–	90	–	nA
Deep sleep current, example 3, V_{BAT} = 1.25 V	Ids3	As Ids2 but with 8 kB RAM data retention.	–	300	–	nA
Standby Mode current, V_{BAT} = 1.25 V	Istb	Digital blocks and memories are not clocked and are powered at a reduced voltage.	–	30	–	μA
Current consumption RX, V_{BAT} = 3 V	I_{VBAT}		–	0.9	–	mA
Current consumption TX, V_{BAT} = 3 V	I_{VBAT}		–	0.9	–	mA
Deep sleep current, example 1, V_{BAT} = 3 V	Ids1	Wake up from wake up pin.	–	25	–	nA
Deep sleep current, example 2, V_{BAT} = 3 V	Ids2	Embedded 32 kHz oscillator running with interrupts from timer or external pin.	–	40	–	nA
Deep sleep current, example 3, V_{BAT} = 3 V	Ids3	As Ids2 but with 8 kB RAM data retention.	–	100	–	nA
Standby Mode current, V_{BAT} = 3 V	Istb	Digital blocks and memories are not clocked and are powered at a reduced voltage.	–	17	–	μA
EEMBC ULPMark BENCHMARK, CORE PROFILE						
ULPMark CP 3.0 V		Arm Cortex−M3 processor running from RAM, VBAT= 3.0 V, IAR C/C++ Compiler for ARM 8.20.1.14183	–	1090	–	ULP Mark
ULPMark CP 2.1 V		Arm Cortex−M3 processor running from RAM, VBAT= 2.1 V, IAR C/C++ Compiler for ARM 8.20.1.14183	–	1260	–	ULP Mark
EEMBC CoreMark BENCHMARK for the Arm Cortex−M3 Processor and the LPDSP32 DSP						
Arm Cortex−M3 processor running from RAM		At 48 MHz SYSCLK. Using the IAR 8.10.1 C compiler, certified	–	159	–	Core Mark

Table 4. ELECTRICAL PERFORMANCE SPECIFICATIONS (continued)
Unless otherwise noted, the specifications mentioned in the table below are valid at 25°C at VBAT = VDDO = 1.25 V.

Description	Symbol	Conditions	Min	Typ	Max	Units
EEMBC CoreMark BENCHMARK for the Arm Cortex−M3 Processor and the LPDSP32 DSP						
LPDSP32 running from RAM		At 48 MHz SYSCLK Using the 2017.03−SP3−2 release of the Synopsys LPDSP32 C compiler	−	133	−	Core Mark
Arm Cortex−M3 processor and LPDSP32 running from RAM, VBAT = 1.25 V		At 48 MHz SYSCLK	−	108	−	Core Mark/ mA
Arm Cortex−M3 processor and LPDSP32 running from RAM, VBAT = 3 V		At 48 MHz SYSCLK	−	257	−	Core Mark/ mA
INTERNALLY GENERATED VDDC: Digital Block Supply Voltage						
Supply voltage: operating range	VDDC		0.92	1.15	1.32 (Note 2)	V
Supply voltage: trimming range	$VDDC_{RANGE}$		0.75	−	1.38	V
Supply voltage: trimming step	$VDDC_{STEP}$		−	10	−	mV
INTERNALLY GENERATED VDDM: Memories Supply Voltage						
Supply voltage: operating range	VDDM		1.05	1.15	1.32 (Note 3)	V
Supply voltage: trimming range	$VDDM_{RANGE}$		0.75	−	1.38	V
Supply voltage: trimming step	$VDDM_{STEP}$		−	10	−	mV
INTERNALLY GENERATED VDDRF: Radio Front end supply voltage						
Supply voltage: operating range	VDDRF		1.00	1.10	1.32 (Notes 4 and 5)	V
Supply voltage: trimming range	$VDDRF_{RANGE}$		0.75	−	1.38	V
Supply voltage: trimming step	$VDDRF_{STEP}$		−	10	−	mV
INTERNALLY GENERATED VDDPA: Optional Radio Power Amplifier Supply Voltage						
Supply voltage: operating range	VDDPA		1.05	1.3	1.68	V
Supply voltage: trimming range	$VDDPA_{RANGE}$		1.05	−	1.68	V
Supply voltage: trimming step	$VDDPA_{STEP}$		−	10	−	mV
Supply voltage: trimming step	$DCDC_{STEP}$		−	10	−	mV
VDDO PAD SUPPLY VOLTAGE: Digital Level High Voltage						
Digital I/O supply	VDDO		1.1	1.25	3.3	V
INDUCTIVE BUCK DC−DC CONVERTER						
VBAT range when the DC−DC converter is active (Note 6)	$DCDC_{IN\_RANGE}$		1.4	−	3.3	V
VBAT range when the LDO is active	LDO_{IN_RANGE}		1.1	−	3.3	V
Output voltage: trimming range	$DCDC_{OUT\_RANGE}$		1.1	1.2	1.32	V
Supply voltage: trimming step	$DCDC_{STEP}$		−	10	−	mV
POWER−ON RESET						
POR voltage	$VBAT_{POR}$		0.4	0.8	1.0	V
RADIO FRONT−END: General Specifications						
RF input impedance	Z_{in}	Single ended	−	50	−	Ω
Input reflection coefficient	S_{11}	All channels	−	−	−8	dB
Data rate FSK / MSK / GFSK	R_{FSK}	OQPSK as MSK	62.5	1000	3000	kbps
Data rate 4−FSK			−	−	4000	kbps
On−air data rate	bps	GFSK	250	−	2000	kbps

Table 4. ELECTRICAL PERFORMANCE SPECIFICATIONS (continued)
Unless otherwise noted, the specifications mentioned in the table below are valid at 25°C at VBAT = VDDO = 1.25 V.

Description	Symbol	Conditions	Min	Typ	Max	Units
RADIO FRONT−END: Crystal and Clock Specifications						
Xtal frequency	F_{XTAL}	Fundamental		48		MHz
Equiv. series Res.	ESR_{XTAL}	RSL10 has internal load capacitors, additional external capacitors are not required	20	–	80	Ω
Differential equivalent load capacitance	CL_{XTAL}	Internal load capacitors (NO EXTERNAL LOAD CAPACITORS REQUIRED)	6	8	10	pF
Settling time			–	0.5	1.5	ms
RADIO FRONT−END: Synthesizer Specifications						
Frequency range	F_{RF}	Supported carrier frequencies	2360	–	2500	MHz
RX frequency step		RX Mode frequency synthesizer resolution	–	–	100	Hz
TX frequency step		TX Mode frequency synthesizer resolution	–	–	600	Hz
PLL Settling time, RX	t_{PLL_RX}	RX Mode	–	15	25	μs
PLL Settling time, TX	t_{PLL_TX}	TX mode, BLE modulation	–	5	10	μs
RADIO FRONT−END: Receive Mode Specifications						
Current consumption at 1 Mbps, V_{BAT} = 1.25 V	$IBAT_{RFRX}$	VDDRF = 1.1 V, 100% duty cycle	–	5.6	–	mA
Current consumption at 2 Mbps, V_{BAT} = 1.25 V	$IBAT_{RFRX}$	VDDRF = 1.1 V, 100% duty cycle	–	6.2	–	mA
Current consumption at 1 Mbps, V_{BAT} = 3 V, DC−DC	$IBAT_{RFRX}$	VDDRF = 1.1 V, 100% duty cycle	–	3.0	–	mA
Current consumption at 2 Mbps, V_{BAT} = 3 V, DC−DC	$IBAT_{RFRX}$	VDDRF = 1.1 V, 100% duty cycle	–	3.4	–	mA
RX Sensitivity, 0.25 Mbps		0.1% BER (Notes 7, 8)	–	−97	–	dBm
RX Sensitivity, 0.5 Mbps		0.1% BER (Notes 7, 8)	–	−96	–	dBm
RX Sensitivity, 1 Mbps, BLE		0.1% BER (Notes 7, 8) Single−ended on chip antenna match to 50 Ω	–	−94	–	dBm
RX Sensitivity, 2 Mbps, BLE		0.1% BER (Notes 7, 8)	–	−92	–	dBm
RSSI effective range		Without AGC	–	60	–	dB
RSSI step size			–	2.4	–	dB
RX AGC range			–	48	–	dB
RX AGC step size		Programmable	–	6	–	dB
Max usable signal level		0.1% BER	0	5	–	dBm
RADIO FRONT−END: Transmit Mode Specifications						
Tx peak power consumption at VBAT = 1.25 V (Note 9)	$IBAT_{RFTX}$	Tx power 0 dBm, VDDRF = 1.07 V, VDDPA: off, LDO mode	–	8.9	–	mA
		Tx power 3 dBm, VDDRF = 1.1 V, VDDPA = 1.26 V, LDO mode	–	17.4	–	mA
		Tx power 6 dBm, VDDRF = 1.1 V, VDDPA = 1.60 V, LDO mode	–	25	–	mA
Tx peak power consumption at VBAT = 3 V (Note 9)	$IBAT_{RFTX}$	Tx power 0 dBm, VDDRF = 1.07 V, VDDPA: off, DC−DC mode	–	4.6	–	mA
		Tx power 3 dBm, VDDRF = 1.1 V, VDDPA = 1.26 V, DC−DC mode	–	8.6	–	mA
		Tx power 6 dBm, VDDRF = 1.1 V, VDDPA = 1.60 V, DC−DC mode	–	12	–	mA
Transmit power range		BLE or 802.15.4 OQPSK	−17	+0.5	+6	dBm

Table 4. ELECTRICAL PERFORMANCE SPECIFICATIONS (continued)
Unless otherwise noted, the specifications mentioned in the table below are valid at 25°C at VBAT = VDDO = 1.25 V.

Description	Symbol	Conditions	Min	Typ	Max	Units
RADIO FRONT−END: Transmit Mode Specifications						
Transmit power step size		Full band.	–	2	–	dB
Transmit power accuracy		Tx power 3 dBm. Full band. Relative to the typical value.	−1.5	–	+1	dB
		Tx power 0 dBm. Full band. Relative to the typical value.	−1.5	–	1.5	dB
Power in 2nd harmonic		0 dBm mode. 50 Ω for “Typ” value. (Note 10)	–	−31	−18	dBm
Power in 3rd harmonic		0 dBm mode. 50 Ω for “Typ” value. (Note 10)	–	−40	−31	dBm
Power in 4th harmonic		0 dBm mode. 50 Ω for “Typ” value. (Note 10)	–	−49	−42	dBm
ADC						
Resolution	ADC_{RES}		8	12	14	bits
Input voltage range	ADC_{RANGE}		0	–	2	V
INL	ADC_{INL}		−2	–	+2	mV
DNL	ADC_{DNL}		−1	–	+1	mV
Channel sampling frequency	ADC_{CH_SF}	For the 8 channels sequentially, SLOWCLK = 1 MHz	0.0195	–	6.25	kHz
32 kHz ON−CHIP RC OSCILLATOR						
Untrimmed Frequency	$Freq_{UNTR}$		20	32	50	kHz
Trimming steps	Steps		–	1.5	–	%
3 MHz ON−CHIP RC OSCILLATOR						
Untrimmed Frequency	$Freq_{UNTR}$		2	3	5	MHz
Trimming steps	Steps		–	1.5	–	%
Hi Speed mode	Fhi		–	10	–	MHz
32 kHz ON−CHIP CRYSTAL OSCILLATOR (Note 11)						
Output Frequency	$Freq_{32k}$	Depends on xtal parameters	–	32768	–	Hz
Startup time			–	1	3	s
Internal load trimming range		Steps of 0.4 pF	0		25.2	pF
Load Capacitance		No external load capacitors required. Maximum external parasitic capacity allowed (package, routing, etc.)	–	–	3.5	pF
ESR			–	–	100	kΩ
Duty Cycle			40	50	60	%
DC CHARACTERISTICS OF THE DIGITAL PADS − With VDDO = 2.97 V − 3.3 V, nominal: 3.0 V Logic						
Voltage level for high input	V_{IH}		2	–	VDDO+0.3	V
Voltage level for low input	V_{IL}		VSSD−0.3	–	0.8	V
DC CHARACTERISTICS OF THE DIGITAL PADS − With VDDO = 1.1 V − 1.32 V, nominal: 1.2 V Logic						
Voltage level for high Input	V_{IH}		0.65* VDDO	–	VDDO+0.3	V
Voltage level for low input	V_{IL}		VSSD−0.3	–	0.35* VDDO	V
DIO DRIVE STRENGTH						
DIO drive strength	IDIO		2	12	12	mA

Table 4. ELECTRICAL PERFORMANCE SPECIFICATIONS (continued)
Unless otherwise noted, the specifications mentioned in the table below are valid at 25°C at VBAT = VDDO = 1.25 V.

Description	Symbol	Conditions	Min	Typ	Max	Units
FLASH SPECIFICATIONS						
Endurance of the 384 kB of flash			10000	–	–	write/ erase cycles
Endurance for sections NVR1, NVR2, and NVR3 (6 kB in total)			1000	–	–	write/ erase cycles
Retention			25	–	–	years

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

2. The maximum VDDC voltage cannot exceed the VBAT input voltage or the VCC output from the buck converter.
3. The maximum VDDM voltage cannot exceed the VBAT input voltage or the VCC output from the buck converter.
4. The maximum VDDRF voltage cannot exceed the VBAT input voltage or the VCC output from the buck converter.
5. The VDDRF calibrated targets are:
   – 1.10 V (TX power > 0 dBm, with optimal RX sensitivity)
   – 1.07 V (TX power = 0 dBm)
   – 1.20 V (TX power = 2 dBm)
   The VDDPA calibrated targets are:
   – 1.30 V
   – 1.26 V (TX power = 3 dBm, assumes VDDRF = 1.10 V)
   – 1.60 V (TX power = 6 dBm, assumes VDDRF = 1.10 V)
6. The LDO can be used to regulate down from VBAT and generate VCC. For VBAT values higher than 1.5 V, the LDO is less efficient and it is possible to save power by activating the DC−DC converter to generate VCC.
7. Signal generated by RF tester.
8. 0.5 to 1.0 dB degradation in the RX sensitivity is present on the QFN package vs WLCSP. This is attributed to the presence of the metal slug of the QFN package which is in close proximity to on−chip inductors.
9. All values are based on evaluation board performance at the antenna connector, including the harmonic filter loss
10. The values shown here are without RF filter. Harmonics need to be filtered with an external filter.
11. These specifications have been validated with the Epson Toyocom MC − 306 crystal

Table 5. VDDM Target Trimming Voltage in Function of VDDO Voltage

VDDM Voltage (V)	DIO_PAD_CFG DRIVE	Maximum VDDO Voltage (V)
1.05	1	2.7
1.05	0	3.2
1.10	0	3.3

NOTE: These are trimming targets at room/ATE temperature 25~30°C.

Table 6. VDDC Target Trimming Voltage in Function of SYSCLK Frequency

VDDC Voltage (V)	Maximum SYSCLK Frequency (MHz)	Restriction
0.92	≤ 24	The ADC will be functional in low frequency mode and between 0 and 85°C only.
1.00	≤ 24	Fully functional
1.05	48	Fully functional

NOTE: These are trimming targets at room/ATE temperature 25~30°C.

ANTENNA SPECIFICATIONS

The antenna performance of the RSL10 SIP depends on the size of the ground plane on which it is mounted. Figure 4 shows an overview of different ground plane sizes with expected antenna return losses shown in Figure 5.

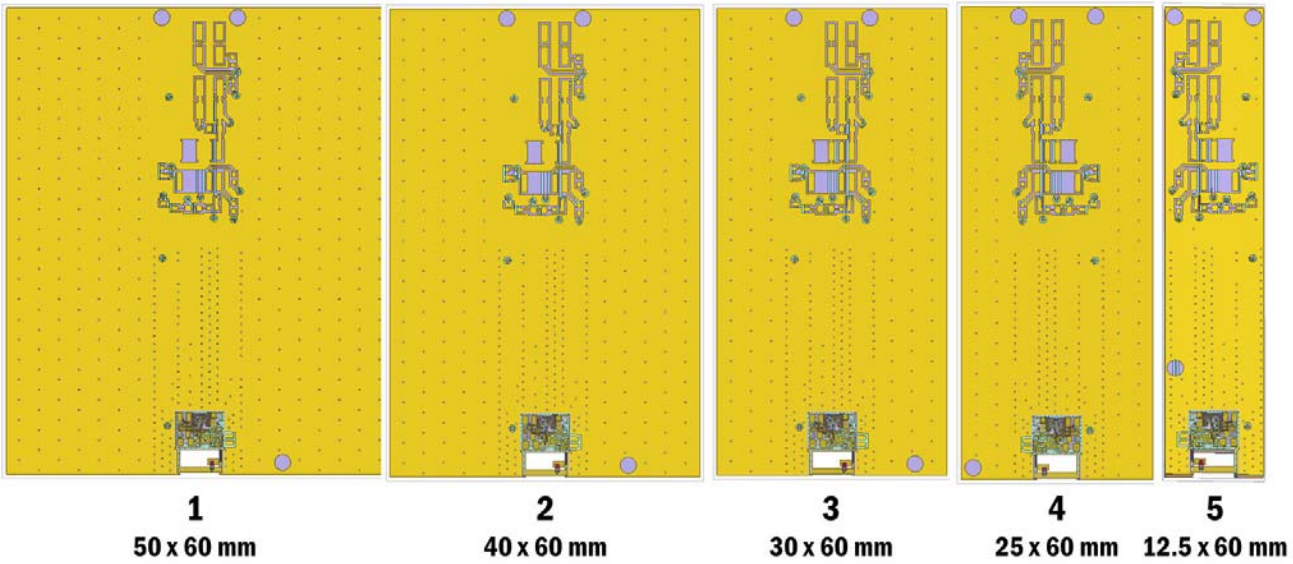


Figure 4. PCB ground planes. 1) 50x60, 2) 40x60, 3) 30x60, 4) 25x60, 5) 12.5x60. All sizes in mm.

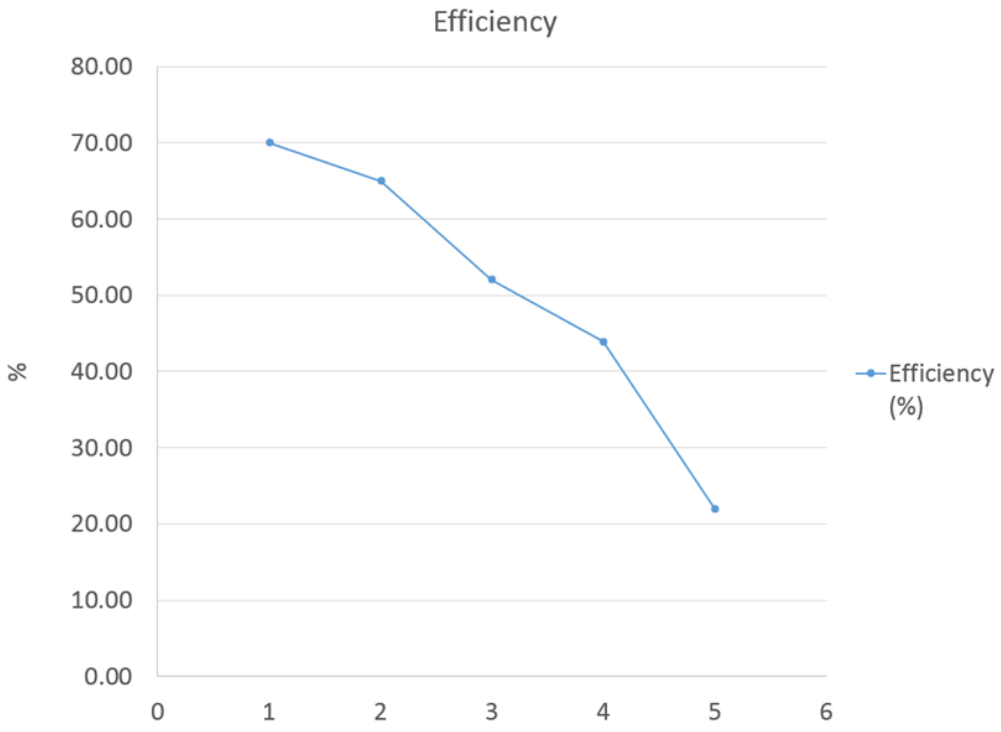


Figure 5. Antenna Efficiency vs. PCB Size.

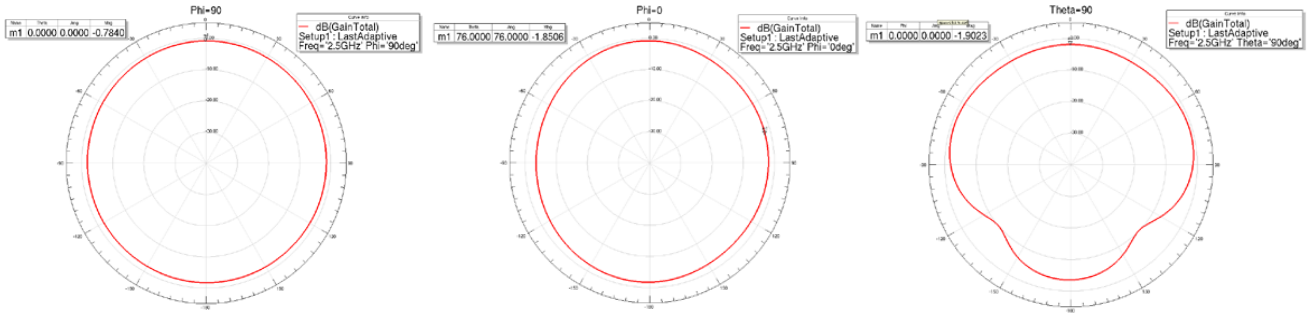


Figure 6. Radiation Pattern for PCB Ground Plane 1 (50 x 60 mm)

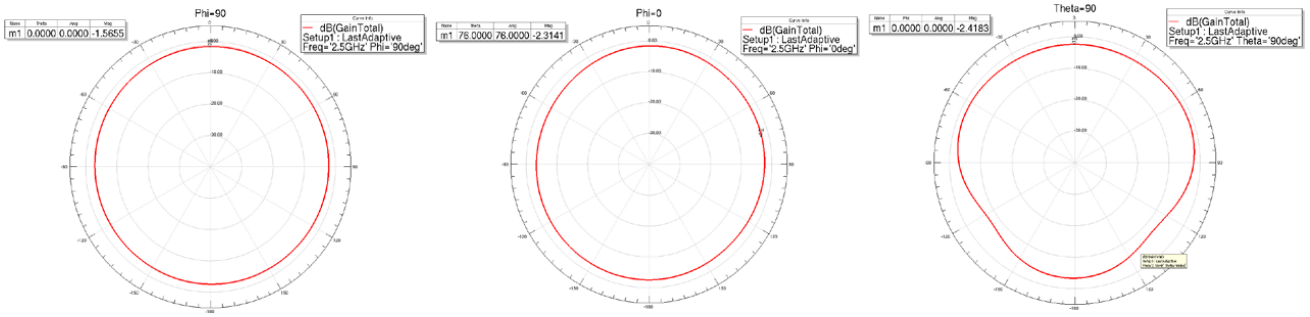


Figure 7. Radiation Pattern for PCB Ground Plane 2 (40 x 60 mm)

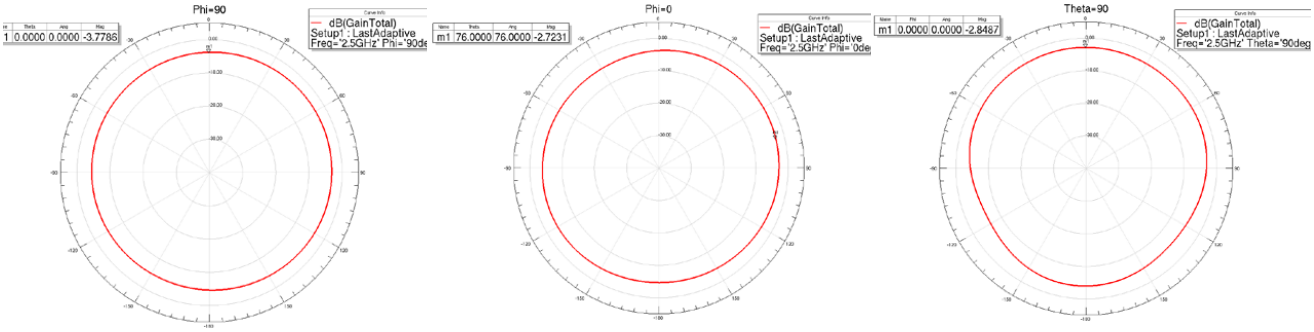


Figure 8. Radiation Pattern for PCB Ground Plane 3 (30 x 60 mm)

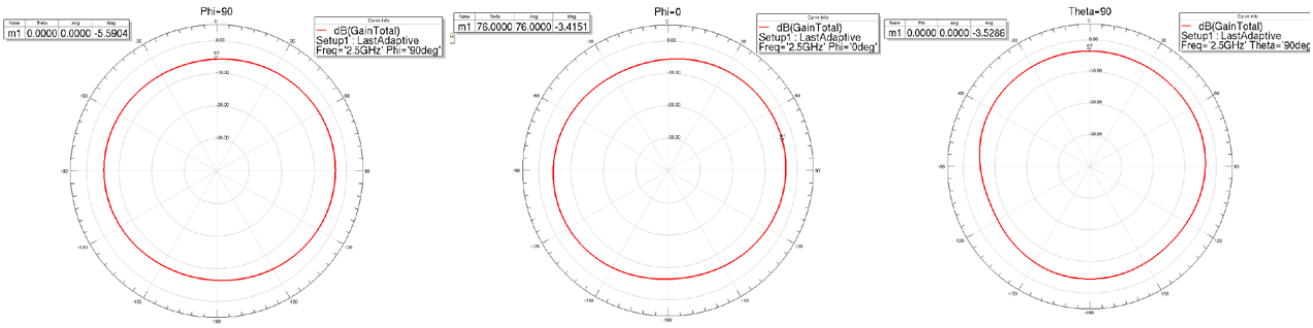


Figure 9. Radiation Pattern for PCB Ground Plane 4 (25 x 60 mm)

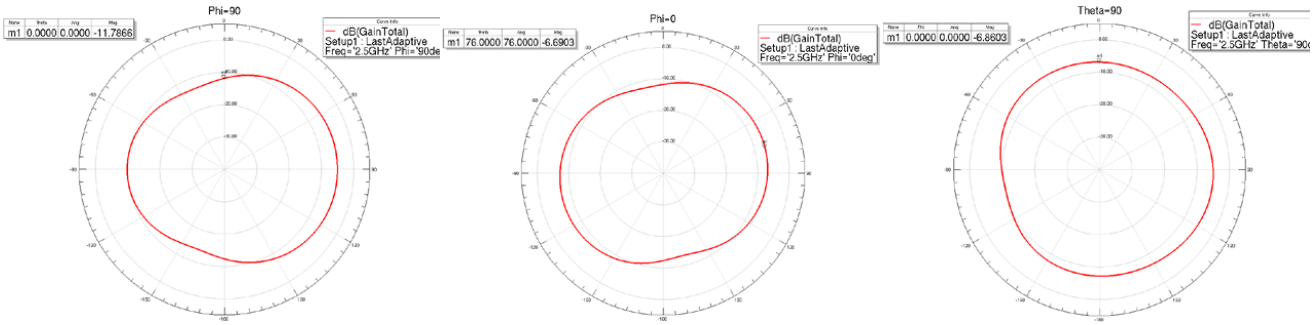


Figure 10. Radiation Pattern for PCB Ground Plane 5 (12.5 x 60 mm)

ENVIRONMENTAL SPECIFICATIONS

Electrostatic Discharge (ESD) Sensitive Device

CAUTION: ESD sensitive device. Permanent damage may occur on devices subjected to high−energy electrostatic discharges.

Proper ESD precautions in handling, packaging and testing are recommended to avoid performance degradation or loss of functionality.

Solder Information

The RSL10 SIP is constructed with all RoHS compliant material and should be reflowed accordingly. This device is Moisture Sensitive Class MSL3 and must be stored and handled accordingly. Re−flow according to IPC/JEDEC standard J−STD−020C, Joint Industry Standard: Re−flow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices. Hand soldering is not recommended for this part.

For more information, see SOLDERRM/D available from http://onsemi.com.

REGULATORY INFORMATION

FCC Regulatory and User Information

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) this device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation. Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

Note:

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

The following ID information needs to be added to the product package (application and user documentation).

FCC ID: Pending
IC: Pending
HVIN: Pending

ISED Regulatory and User Information

This device complies with Industry Canada−s licence−exempt RSSs. Operation is subject to the following two conditions: (1) This device may not cause interference; and (2) This device must accept any interference, including interference that may cause undesired operation of the device.

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes : (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

CAN ICES−3 (B)/NMB−3(B) – This Class B Digital Apparatus Complies with Canadian ICES−003.

Cet Appareil numerique de la classe (B) est conforme a la norme NMB−003 du Canada.

The following ID information needs to be added to the product package (application and user documentation).

IC: Pending
HVIN: Pending

Korean Regulatory and User Information

특정소출력 무선기기(데이터통신시스템용 무선기기)

제 조 자 (Manufacturer): ON Semiconductor
제 조 국 (Origin): Canada
제 품 명 (Product): Pending
모 델 명 (Model): Pending
제조년월 (Production date): Pending
이 장치는 이동전화, Wi-Fi 또는 블루투스 장치 등 무선통신장치와 매우 근접한 장소에서 사용할 경우 오작동을 일으킬 가능성이 있습니다.
해당 무선설비는 전파혼신 가능성이 있으므로 인명안전과 관련된 서비스는 할 수 없음.

The following ID information needs to be added to the product package (application and user documentation).

Korean KC Mark and Identifier as shown below. Height of KC mark is 5mm minimum. Colour preference is Navy. Acceptable other colours are black, gold and silver. Other colours may only be used if preferred colours are not legible for the mark.

R-CRM-oNs-Pending

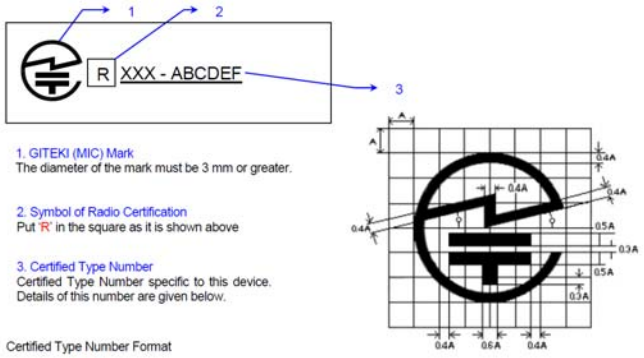
European Regulatory and User Information

The following ID information needs to be added to the product package (application and user documentation).

Japanese Regulatory and User Information

The following ID information needs to be added to the product package (application and user documentation).

ID (pending) and must be combined with the Giteki (MIC) Mark as specified below.



Development Tools

RSL10 is supported by a full suite of comprehensive tools including:

- An easy−to−use development board
- Software Development Kit (SDK) including an Oxygen Eclipse−based development environment, Bluetooth protocol stacks, sample code, libraries, and documentation

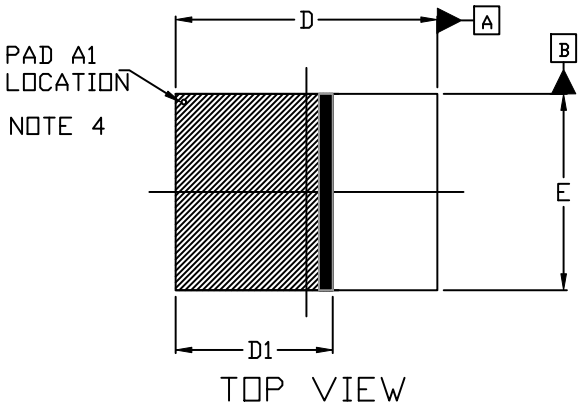
Company or Product Inquiries

For more information about ON Semiconductor products or services visit our Web site at http://onsemi.com.

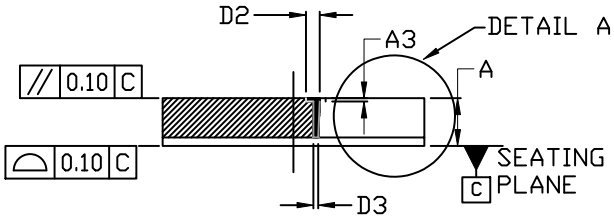
For sales or technical support, contact your local representative or authorized distributor.

PACKAGE DIMENSIONS

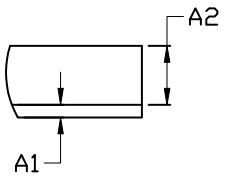
SIP51 8x6
CASE 127EY
ISSUE A



TOP VIEW



SIDE VIEW

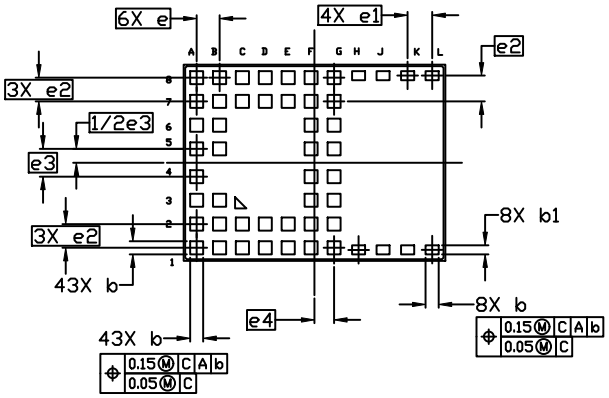


DETAIL A

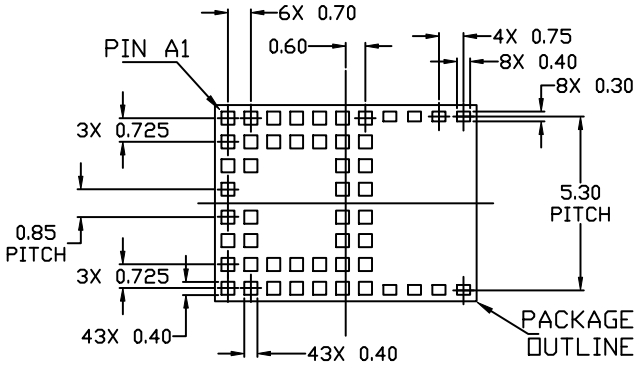
NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM THE TERMINAL TIP.
4. PIN 1 IDENTIFIER IS LOCATED HERE MAY APPEAR AS A CHAMFER, INK MARK, METALLIZED MARK, ETC.
5. REFER TO PRODUCT DATASHEET FOR SPECIFIC KEEP-OUT AREA AND GROUND PLANE REQUIREMENTS.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	1.36	1.46	1.56
A1	0.23	0.26	0.29
A2	1.13	1.20	1.27
A3		0.10 REF	
b	0.35	0.40	0.45
b1	0.225	0.275	0.325
D	7.90	8.00	8.10
D1		4.805 REF	
D2		0.42 REF	
D3		0.15 REF	
E	5.90	6.00	6.10
e		0.70 BSC	
e1		0.75 BSC	
e2		0.725 BSC	
e3		0.85 BSC	
e4		0.60 REF	



BOTTOM VIEW



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