Serial RTC with Alarm and Timer

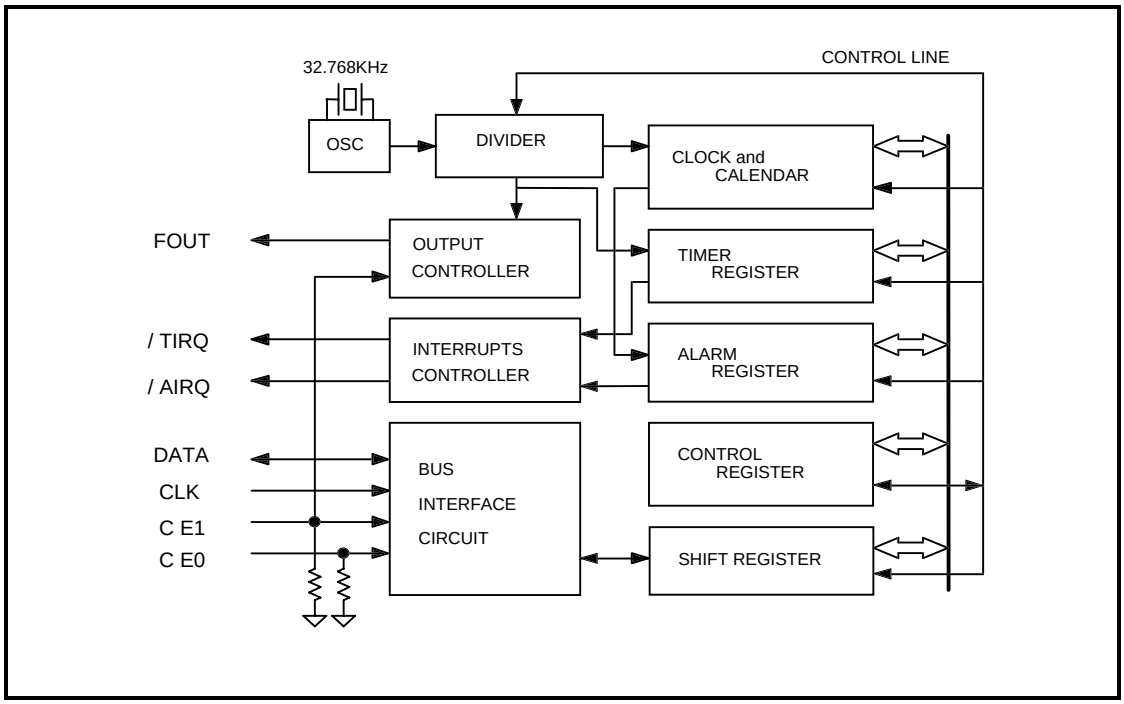
RTC - 4573

- Built-in frequency adjusted 32.768KHz crystal oscillator
- Serial interface that can be controlled through three signal lines
- Week , Day , hour , and minute alarm interrupt functions
- Interval timer interrupt function that can be set with an interval ranging from 1/4096th of a second to 255minutes
- Dual dedicated interrupt outputs for software maskable alarms and for timers
- Functions that detect halting of crystal oscillation, and when the time is being updated
- Automatic leap year compensation function
- Wide interface voltage range, from 1.6 to 5.5V
- Wide timing voltage range, from 1.6 to 5.5V
- Low current consumption : 0.5μA/3V (typ.)
- Small SOP package suited for high-density mounting

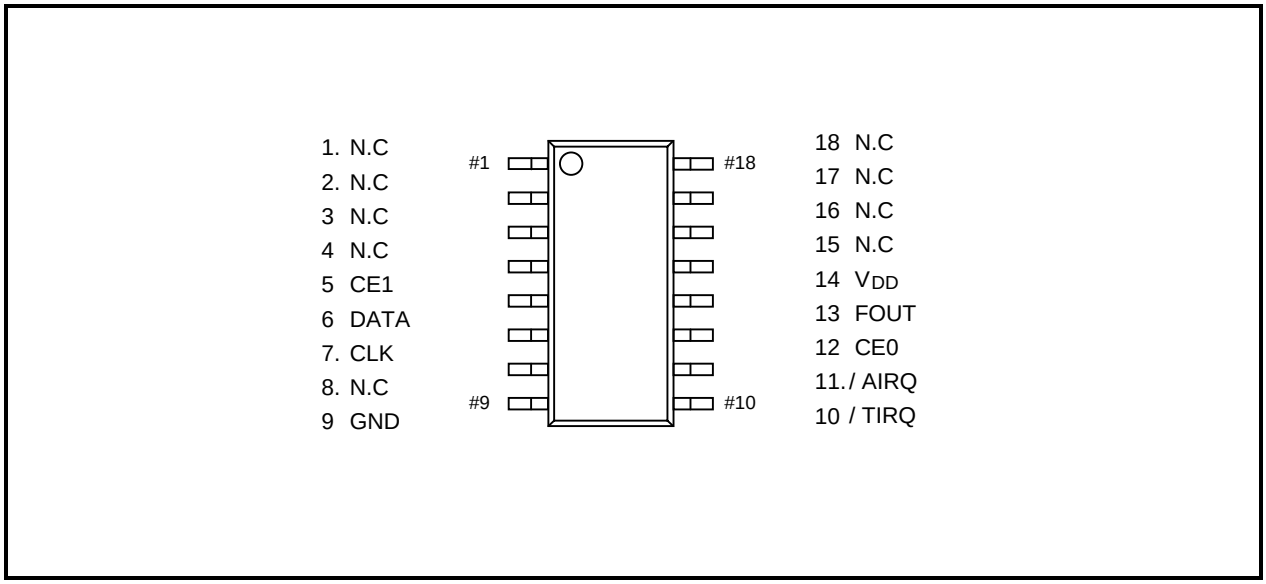
■ Overview

This module is a serial interface-type real-time clock with a crystal oscillator on chip. This module includes clock and calendar circuitry (from seconds to years) with automatic leap year compensation, alarms, and timer interrupt functions, as well as functions that detect when oscillation is halted, the time is being updated. The serial interface permits control through three signal lines, keeping the number of ports required on the system side to a minimum. Because the small SOP package can be used in high-density mounting, this module is ideal for portable telephones, hand-held terminals, and other compact electronic equipment.

■ Block Diagram



■ Pin Connection



Symbol	Pin-No.	I / O	Function
CE1	5	Input	Chip enable 1 input pin. This terminal has pull-down resistor built-in. Access to this RTC is possible in "H" level both CE0,CE1 terminal. FOUT terminal can output frequency when inputs "H" level into this terminal regardless of state of CE0 terminal. FOUT terminal is high impedance state in input "L" level.
DATA	6	Bi-directional	This I/O pin is used to for setting write mode/read mode, for writing an address, and for reading and writing data. This pin functions either as an input pin or an output pin, according to the write mode/read mode setting made in the first 8 bits of input data following the rising edge of the CE input.
CLK	7	Input	Shift clock input pin. In write mode, the data is read from the DATA pin at the rising edge of the CLK signal; in read mode, the data is output from the DATA pin at the rising edge of the CLK signal.
GND	9	-	Connect to the negative (ground) line of the power supply.
/ TIRQ	10	Output	Open drain interrupt output pin for the interval timer.
/ AIRQ	11	Output	Output Open drain interrupt output pin for alarms.
CE0	12	Input	Chip enable 0 input pin. When high, access to the internal registers is enabled. While low, the DATA pin goes to high impedance. When the CE pin is set low, the fr, TEST, and RESET bits are forcibly cleared to "0".Set this pin low when turning the power on, when the device is not to be accessed, and when using the backup power supply. This pin does not affect FOUT terminal.
FOUT	13	Output	Frequency output terminal. Frequency is selectable by software.
VDD	14	-	Connect to the positive line of the power supply. Access is possible between 1.6 and 5.5V
N.C.	1,2,3, 4,8, 15,16, 17,18		Although these pins are not connected internally, they should always be left open in order to obtain the most stable oscillation possible.

* Always connect a passthrough capacitor of at least 0.1μF as close as possible between VDD and GND.

■ Electrical Characteristics

1. Absolute Maximum Ratings

Description	Symbol	Conditions	Rated values	Unit
Power supply Voltage	V_{DD}	-	-0.3 to +7.0	V
Input Voltage	V_{IN1}	input pins	GND-0.3 to V_{DD}+0.3	V
Output Voltage	V_{OUT1}	/ TIRQ,/ AIRQ	-0.3 to +8.0	V
	V_{OUT2}	FOUT,DATA	GND-0.3 to V_{DD}+0.3	
Temperature	T_{STG}	-	-55 to +125	°C

2. Operating Condition

Item	Symbol	Conditions	MIN.	MAX.	Unit
Supply Voltage	V_{DD}	-	1.6	5.5	V
Data Holding Voltage	V_{CLK}	-	1.6	5.5	V
Operating Temperature Range	T_{OPR}	-		+85	° C

3. Frequency Characteristics

Item	Symbol	Conditions	Specifications	Unit
Frequency accuracy	f / fo	Ta=25 °C,V_{DD}=3V	5 ± 23 *	ppm
Oscillator start up time	t_{STA}	Ta=25°C,V_{DD}=1.6V	3 (MAX)	sec
Temperature characteristics		-10 to 70 °C 25 °C(Typ)	+10 / -120	ppm
Voltage characteristics		Ta=25°C,V_{DD}=1.6 to 5.5V	± 2.0	ppm / V

* Monthly error of about 1 minute

4. DC Characteristics

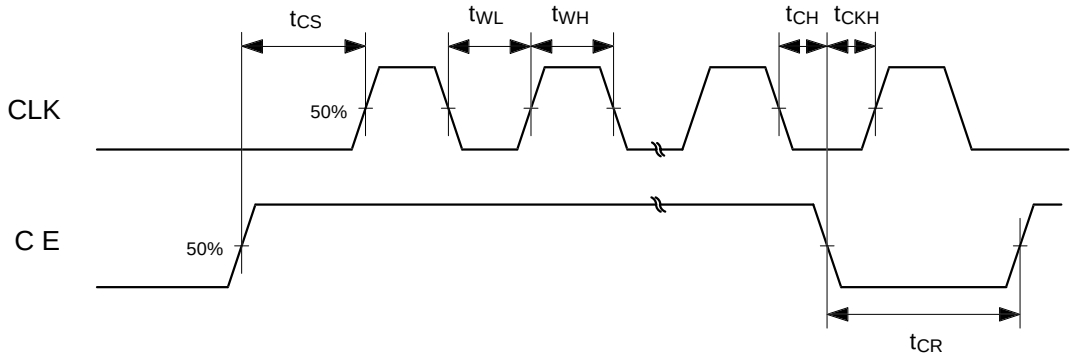
(V_{DD} =1.6 to 5.5V,Ta=-40 to 85°C)

Description	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Standby current 1	I_{DD1}	VDD=5V	CE0,CE1=GND	-	1.0	2.0	mA
Standby current 2	I_{DD2}	VDD=3V	CE0,CE1=GND	-	0.5	1.0	mA
Input Voltage	VIH	CE0,CE1		0.8V_{DD}	-	V_{DD}	V
	VIL	CLK,DATA pins		0	-	0.2V_{DD}	V
Input leakage current	ILK	VI=V_{DD} or GND CLK pins		-0.5	-	0.5	mA
Pulldown R 1	R_{DWN1}	VDD=5V		75	150	300	kW
Pulldown R 2	R_{DWN2}	VDD=3V	CE0,CE1 pins	150	300	600	kW
Output voltage 1	V_{OH1}	VDD=5V	I_{OH}=-1mA	4.5		5.0	V
	V_{OH2}	VDD=3V	DATA,FOUT pins	2.0		3.0	V
	V_{OH3}	VDD=3V	I_{OH}=-100mA DATA,FOUT pins	2.9		3.0	V
	V_{OL1}	VDD=5V	I_{OL}=1mA			GND+0.5	V
	V_{OL2}	VDD=3V	DATA,FOUT pins			GND+0.8	V
	V_{OL3}	VDD=3V	I_{OL}=100 mA DATA,FOUT pins			GND+0.1	V
Output voltage 2	V_{OL4}	VDD=5V	I_{OL}=1mA			GND+0.25	V
	V_{OL5}	VDD=3V	/ AIRQ,/ TIRQ pins			GND+0.4	V
Leakage current	IOZ	VO=GND or V_{DD} DATA,/ AIRQ,/ TIRQ pins		-0.5		0.5	mA

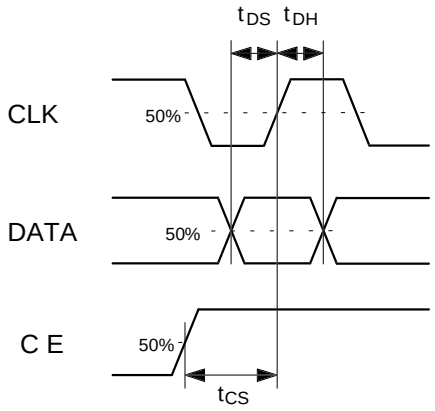
5. AC Characteristics

(CL=50pF,Ta=-40 to 85°C)

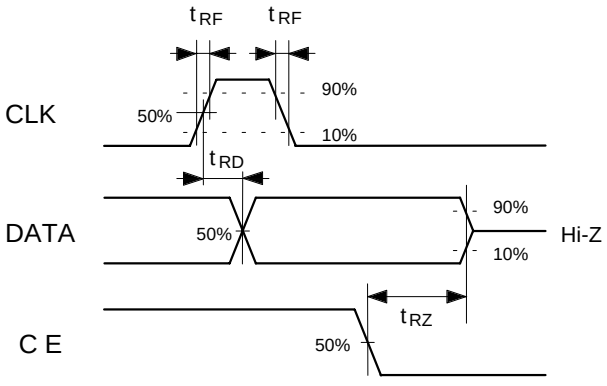
Description	Symbol	VDD=3.0V±10%			VDD=5.0V±10%			Unit
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
CLK clock cycle	tCLK	1200			600			ns
CLK H Pulse Width	tWH	600	-	-	300	-	-	ns
CLK L Pulse Width	tWL	600	-	-	300	-	-	ns
CE setup time	tCS	300	-	-	150	-	-	ns
CE hold time	tCH	400	-	-	200	-	-	ns
CE recovery time	tCR	600	-	-	300	-	-	ns
CLK hold time	tCKH	100	-	-	50	-	-	ns
Write DATA in setup time	tDS	50	-	-	50	-	-	ns
Write DATA in hold time	tDH	50	-	-	50	-	-	ns
Read DATA in delay time	tRD	0	-	400	0	-	200	ns
Output disable delay time	tRZ	-	-	200	-	-	100	ns
rise and fall time	tRF	-	-	40	-	-	20	ns
FOUT duty ratio (32.768kHz output)	Duty	35	-	65	40	-	60	%



Write Mode



ReadMode



■ Register Table

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
0	Sec	fos	40	20	10	8	4	2	1
1	Min	fr	40	20	10	8	4	2	1
2	Hour	fr	*	20	10	8	4	2	1
3	Week	fr	6	5	4	3	2	1	0
4	Day	fr	*	20	10	8	4	2	1
5	Month	fr	*	*	10	8	4	2	1
6	Year	80	40	20	10	8	4	2	1
7	Minutes Alarm	AE	40	20	10	8	4	2	1
8	Hours Alarm	AE	*	20	10	8	4	2	1
9	Week Alarm	AE	6	5	4	3	2	1	0
A	Day Alarm	AE	*	20	10	8	4	2	1
B	FOUT control	FE	*	FD4	FD3	*	FD2	FD1	FD0
C	Timer interrupt control	TE	*	TD1	TD0	*	*	*	*
D	Count Down Timer	128	64	32	16	8	4	2	1
E	Control 1	*	*	*	TI/TP	AF	TF	AIE	TIE
F	Control 2	*	TEST	STOP	RESET	HOLD	*	*	*

1.1 Timekeeping/calendar registers (register 0 to register 6)

- The data in these registers is BCD format. For example, "0101 1001" represents 59 seconds. In addition, the "*" mark in the register table means that the register is readable and writable, and can be used as RAM. Time is kept in the 24-hour format.

- Writing to a bit marked with an asterisk ("*") is permitted; such bits can be used as RAM. When the alarm and timer functions are not used, registers 7 to A can be used as 8-bit memory registers, and registers C and D can be used as 7-bit memory registers.

- **Year register and leap years**
  A leap year is detected by dividing the two BCD digits of the year register by four; if the remainder is zero, the year is a leap year. Therefore, leap years can be automatically determined whether the year is numbered according to the western calendar or the Japanese calendar (year of Heisei).

- **Day of the week**
  The day of the week register uses 7 bits, from 0 to 6; the meanings of the bits are shown in the table below. Do not set more than one bit to "1" at any one time.

bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	day of week
0	0	0	0	0	0	1	Sunday
0	0	0	0	0	1	0	Monday
0	0	0	0	1	0	0	Tuesday
0	0	0	1	0	0	0	Wednesday
0	0	1	0	0	0	0	Thursday
0	1	0	0	0	0	0	Friday
1	0	0	0	0	0	0	Saturday

- **fos** (OSC Flag)
  This flag uses it for a monitor of battery listing degradation with the binary digit which that oscillation stopped is set at. Oscillation stopping shows "1", and it is cleared by writing in "0". But fo flag can't write in "0" when oscillation stopped. And fo can write in "1", but don't write in it. Other binary digit (HOLD,STOP,RESET) doesn't receive affect even in case of "1".

- **fr** (READ Flag)
  It is the binary digit that turn into "1" when CE was input, and carry occurred during "H" for 1 second. The distinction that carry to a figure rose during (CE input ="H" during readout of register in an indicator by this for 1 second is possible. When fr was "1", I need to read register in all indicators once again.

1.2 Alarm registers (register 7 to register A)

Alarms can be set for days of the week, hours, and minutes. Bit 7 of each alarm register is an AE bit that can be used to set an hourly alarm or a daily alarm. An alarm can also be set for multiple days of the week.However, when using the day of the week alarm, also set either or both the hour and minute alarms. If the day of the week alarm is set by itself, the alarm may not be output properly.When the AE bit is "0", the register in question and the timekeeping register is compared; when the AE bit is "1", this indicates "don't care", and the registers are assumed to match, regardless of the data.

1.3. Frequency output control register (Reg-B)

FE bit is Frequency output enable bit. Source clock is selectable by FD4 and FD3 bits. And Count down rate is selectable by FD0 , FD1 and FD2 bits. This frequency is output from FOUT terminal.

FOUT control (Reg.B)

FD4	FD3	Source Clk.
0	0	32768Hz
0	1	1024Hz
1	0	32Hz
1	1	1Hz

FD2	FD1	FD0	Div.	FOUT Duty
0	0	0	1 / 1	50%
0	0	1	1 / 2	50%
0	1	0	1 / 3	33%
0	1	1	1 / 6	50%
1	0	0	1 / 5	20%
1	0	1	1 / 10	50%
1	1	0	1 / 15	33%
1	1	1	1 / 30	50%

1.4. Timer register(Reg-C to Reg-D)

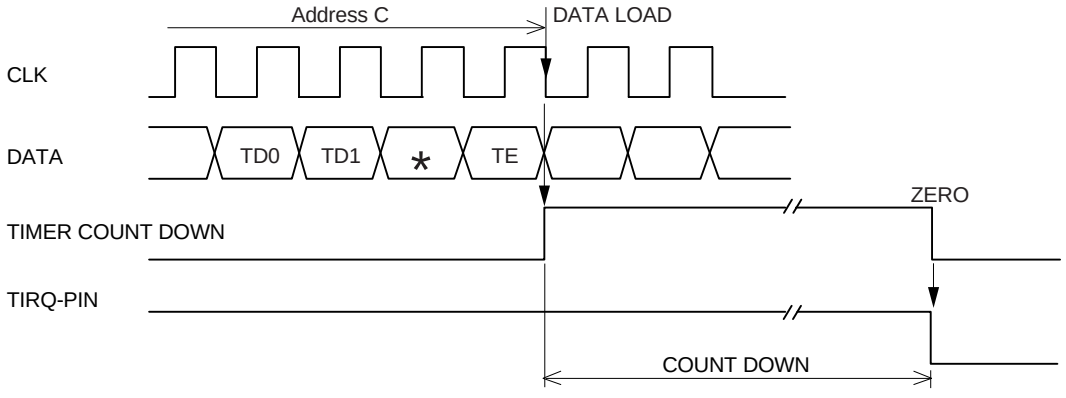
Register-D is presetable binary down counter of 8 bits.
Source clock of this counter does setup by TD bit of Register-C.
Register-D does countdown by a period of selected source clock.
When data of register-D becomes 0, /TIRQ terminal changes to Low level.
In that time, register-D does written data reloads again if TI/TP bit is 1.
And counter does countdown repeatedly.
As a result, by a same period, interrupt occurs repeatedly.
When TIE bit of Register-E is "0", /TIRQ terminal keep high impedance.
When TI/TP bit is 0, Register-D does never reload the data.
Set TI/TP.TD,TIE and TE bits carefully, for perfect function of timer.

Source clock control for Timer (Reg.C)

TD1	TD0	Source Clk.
0	0	4096Hz
0	1	64Hz
1	0 sec.	update
1	1 min.	update

When TEbit is 0, Register-D loads preset data, and keeps stop. Note:There isn't pause.
When TE bit is cleared, Register-D starts countdown from preset data.
Timer interrupt doesn't occur when set 0 in Register-D.
Therefore pay attention because 1 period error of source clock occurs as for timer time.

Timing of Timer start



1.5. Control register1 (Reg-E)

Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
E	*	*	*	TI/TP	AF	TF	AIE	TIE

TI / TPbits: (Interrupt Signal Output Mode Select. Timer-Interrupt / Timer-Periodic)
output mode of timer signaling.

bit	0	1
TI / TP	TIRQ terminal is maintained by "L" till it is written in "0" at TF bit when turn into interrupt mode, and timer interrupt occurs, and, but, timer interrupt signal does it with TIE=1	Timer interrupt signaling is set in a mode repeatedly. When timer interrupt occurs, TIRQ terminal is set at "L" immediately and, but, does it with TIE=1. TF bit is set in "1", and TIRQ terminal is set in Hi-Z after approximately 3.9 m s, and TF bit holds "1" till it is write clear by "0".

AF / TF bits: (Alarm Flag / Timer Flag)
When alarm occurs, AF bit is set in "1", and a timer is set in "1" at 0 o?clock, and TF bit can?t write in "1" at both bit.

AIE,TIE bits: (Alarm / Timer Interrupt Enable)
It is decided whether IRQ terminal drives it when alarm, timer interrupt occurred, and AIE corresponds in alarm, and TIE corresponds to a timer, and AIRQ terminal is set in case of "0" AIE bit by Hi-Z, and TIRQ terminal is set in case of "0" TIE bit by Hi-Z.

1.6 Control register 2 (register F)

Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
F	*	TEST	STOP	RESET	HOLD	*	*	*

· **TEST bit :** This is a test bit for Seiko-Epson?s use.
Always set this bit to "0". When writing to the other bits in the CF register, be careful not to accidentally write a "1" to this bit. This bit is cleared by setting CE low.

· **STOP bit**
If this bit is set to "1", timekeeping stops (after 4KHz). If this bit is set back to "0", timekeeping resumes.

· **RESET bit**
Setting this bit to "1" resets the counter below the seconds counter, stopping timekeeping. If a "1" is written to this bit, it is cleared either by writing a "0" to this bit again with the auto increment function, or by setting CE low.
The only effect on timekeeping precision is a maximum error 61 [micro]s. This bit is unaffected by the status of other bits.

· **HOLD bit**
This bit stops carries to the ones digit of the seconds counter. Timekeeping continues below the seconds counter, and if there was a carry to the seconds counter while HOLD = 1, compensation (by means of adding one second) is made immediately (within 0 to 122 [micro]s) after HOLD is released.This bit is cleared by writing a "0" to it.

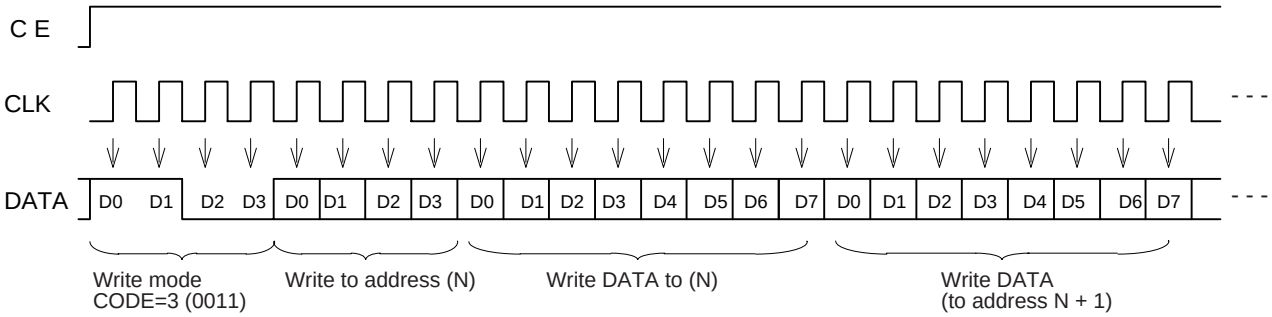
■ Usage

Functional Overview

The basic sequence for reads and writes is the same: after the CE input goes high, the 4-bit mode is set, the 4-bit address is specified, and then the data is read or written in 8-bit units.If the input of an 8-bit unit of data is not yet complete when the CE input is set low, the 8-bit data that was being written when the CE input went low is ignored. (Prior data is valid. Also, in these circumstances, the WF bit is set to "1", indicating that the write operation was not completed normally.)Writes and reads are both LSB first.

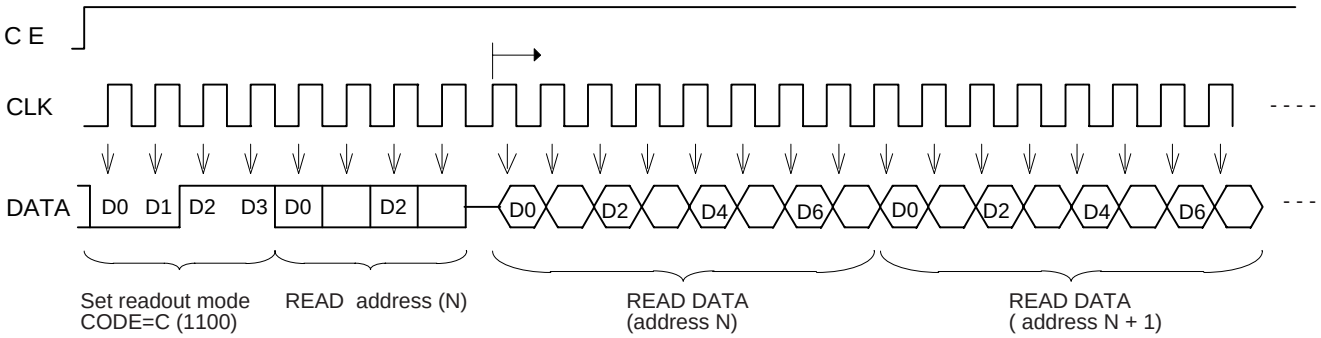
[Writes]

1) After the CE input goes high, set the value of the first four write bits is to "3", indicating write mode, and then set the address to be written in the next four bits.
2) The 8 bits of write data that follow are written to the address that was set; the address is then automatically incremented, and the next 8 bits of data are written to the new address.
3) The automatic address incrementation is cyclic, with address 0 following address F.



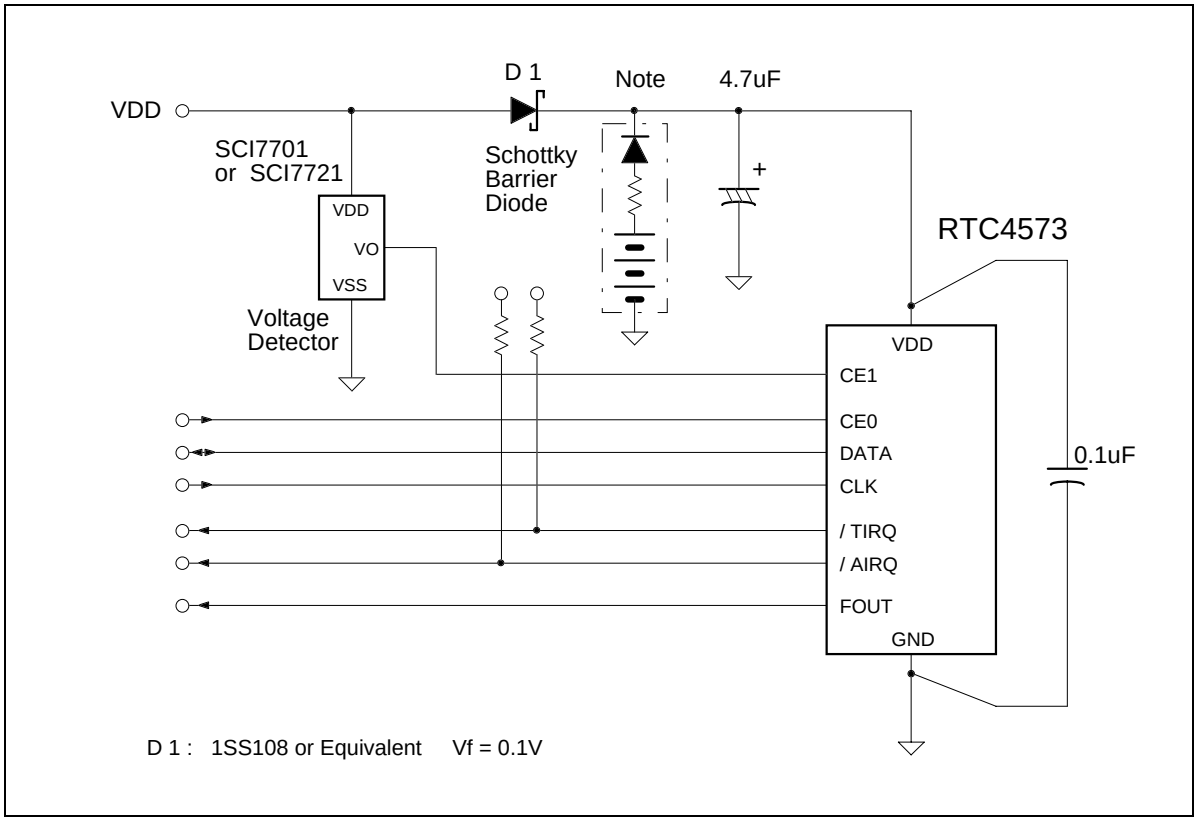
[Reads]

1) After the CE input goes high, set the value of the first four write bits to "C", indicating read mode, and then set the address to be written in the next four bits.
2) The 8 bits of data that follow are read from the address that was set; the address is then automatically incremented, and the next 8 bits of data are read from the new address.
3) The automatic address incrementation is cyclic, with address 0 following address F.

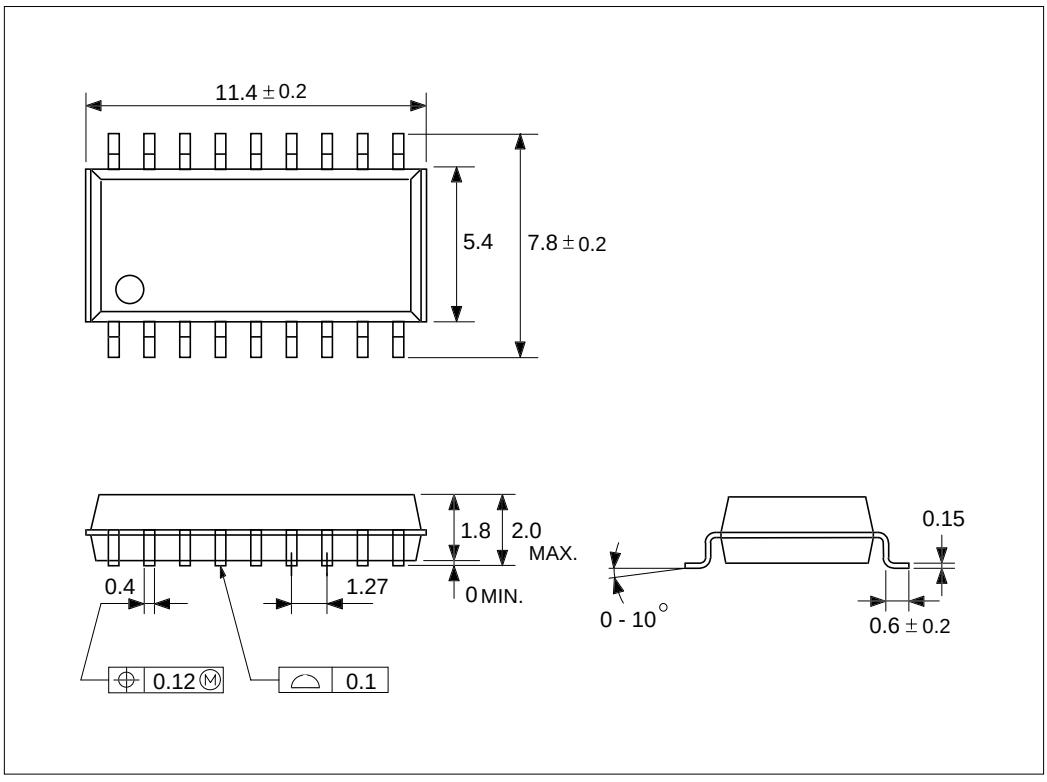


If the mode setting code was set to a value other than "C" or "3", the subsequent data is ignored and the DATA pin remains in the input state.

■ Examples of External Connections



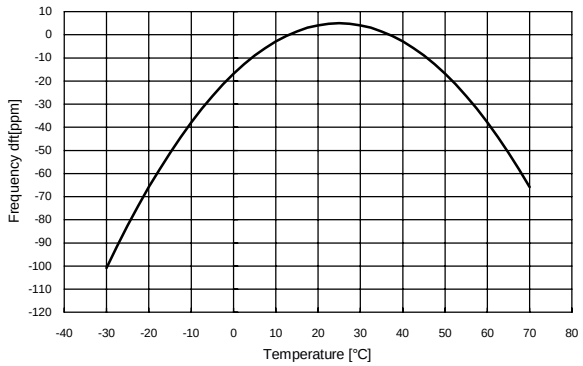
■ Package Outline



■ Reference data

(1) Frequency temperature characteristics (typical)

q_T = 25℃ TYP.
a = -0.035ppm/℃² TYP.



Finding the frequency stability (clock error)

1. The frequency temperature characteristics can be approximated by using the following expression:

$$Df_T(ppm)=a(q_T-q_X)^2$$

Δf_T(ppm)	: Frequency deviation at target temperature
α(ppm/°C^2)	: Secondary temperature coefficient (-0.035 0.005ppm/°C^2)
θ_T(°C)	: Peak temperature (25°C±5°C)
θ_X(°C)	: Target temperature

2. To determine the overall clock accuracy, add the frequency tolerance and the voltage characteristics:

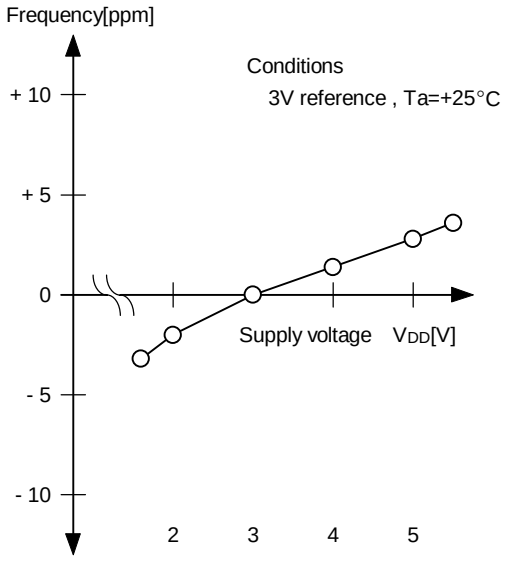
$$Df/f(ppm) = Df/f0 + Df_T + Df_V$$

$\Delta f/f$ (ppm)	: Clock accuracy at a given temperature and voltage
$\Delta f/f_0$(ppm)	: Frequency tolerance
Δf_T (ppm)	: Temperature dependent frequency deviation
Δf_V (ppm)	: Voltage dependent frequency deviation

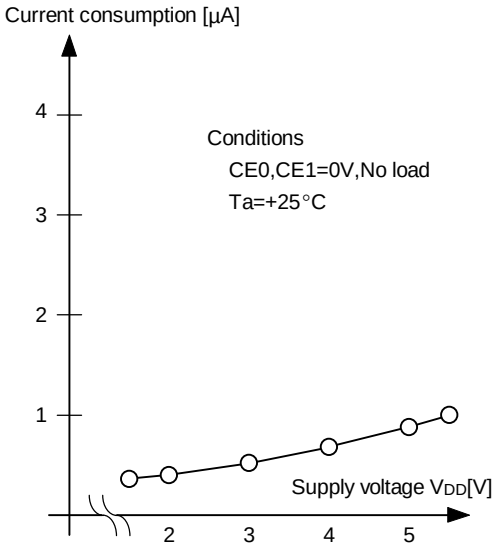
3. Finding the daily deviation:

Daily deviation (seconds) = $Df/f \times 10^{-6} \times 86400$
The clock error is one second per day at 11.574 ppm.

(2) Frequency voltage characteristics (typical)



(3) Current consumption voltage characteristics (typical)



Note : This data shows average values for a sample lot.
For rated values, see the spacifications on page 3.

■ Notes on Use

(1) Notes on handling

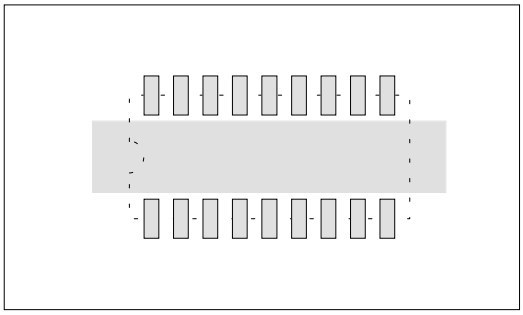
In order to attain low power consumption, this module incorporates a CMOS IC. Therefore, the following points should be kept in mind when using this module.

1. Static electricity

While this module does have built-in circuitry designed to protect it against damage from electrostatic discharge, the module could still be damaged by an extremely large electrostatic discharge. Therefore, packing materials and shipping containers should be made of conductive materials.Furthermore, use soldering equipment, test circuits, etc., that do not have high-voltage leakage, and ground such equipment when working with it.

2. Electronic noise

If excessive external noise is applied to the power supply and I/O pins, the module may operate incorrectly or may even be damaged as a result of the latch-up phenomenon.
In order to assure stable operation, connect a passthrough capacitor (ceramic is recommended) of at least 0.1μF located as closely as possible to the power supply pins on this module (between V_{DD} and GND). Furthermore, do not place a device that generates high noise levels near this module.Keep signal lines away from the shaded areas shown in the figure at right, and fill the area with a GND pattern, if possible.



3. Electric potential of I/O pins

Because having the electric potential of the input pins at an intermediate level contributes to increased power consumption, reduced noise margin, and degradation of the device, keep the electric potential as close as possible to the electric potential of V_{DD} or GND.

4. Treatment of unused input pins

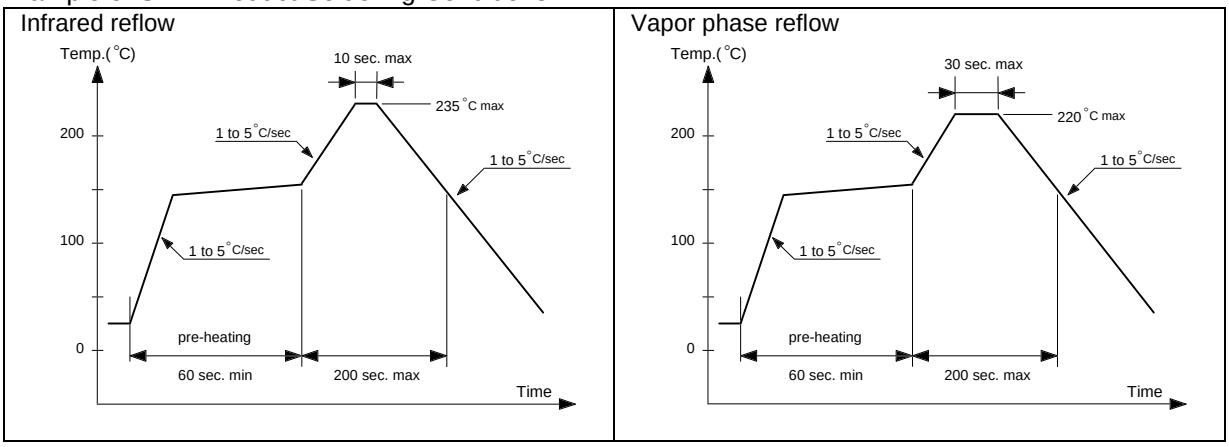
Because the input impedance of the input pins is extremely high and using the module with these pins open can result in unstable electric potential and misoperation due to noise, unused input pins must always be connected to a pull-up or pull-down resistor.

(2) Notes on mounting

1. Soldering temperature conditions

If the internal temperature of the package exceeds 260°C, the characteristics of the crystal resonator may deteriorate and the package may be damaged. Therefore, before using this module, be sure to confirm what temperatures it will be exposed to during the mounting process. If the mounting temperature conditions are ever changed, the suitability of those temperature conditions for this package must be confirmed again.
Soldering conditions: Up to 260°C for up to 10 seconds, twice, or up to 230°C for up to 3 minutes.

Example of SMD Product Soldering Conditions



2. Mounters

While this module can be used with general-purpose mounters, be sure to confirm the force of impact that the module will be subjected to during mounting, since certain machines or conditions can result in damage to the internal crystal resonator. If the mounting conditions are ever changed, the suitability of those conditions for this package must be confirmed again.

3. Ultrasonic cleaning

Under certain conditions, ultrasonic cleaning can damage the crystal resonator. Because we cannot specify the conditions under which you perform ultrasonic cleaning (including the type of cleaner, the power level, the duration, the condition of the inside of the chamber, etc.), Seiko-Epson does not warrant this product against ultrasonic cleaning.

4. Mounting orientation

If this module is mounted backwards, it may be damaged. Always confirm the orientation of the module before mounting it.

5. Leakage between pins

If power is supplied to this module while it is dirty or while condensation is present, leakage between pins may result. Be sure that the module is clean and dry before supplying power to it.