# 128K × 8 ELECTRICALLY ERASABLE EPROM

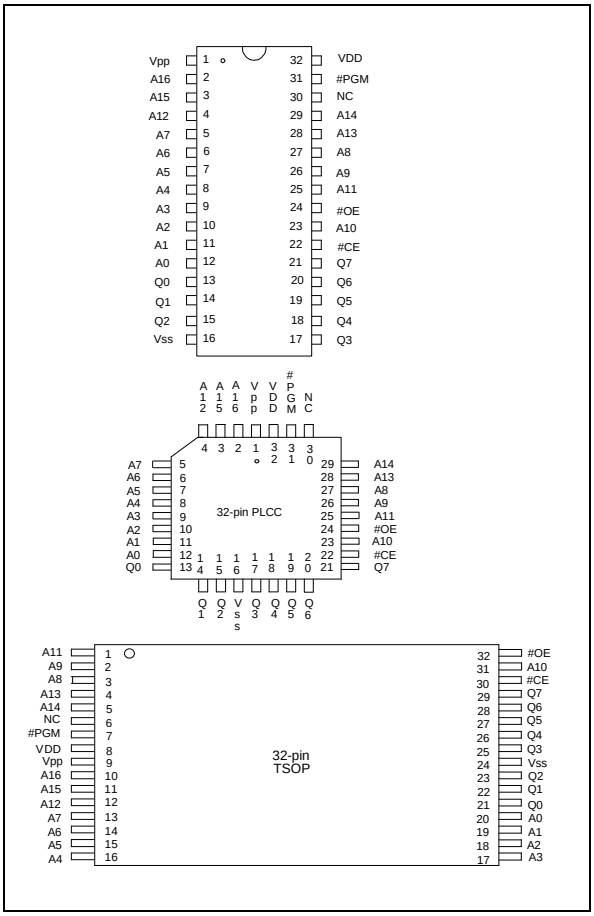
## GENERAL DESCRIPTION

The W27C010 is a high speed, low power Electrically Erasable and Programmable Read Only Memory organized as 131072 × 8 bits that operates on a single 5 volt power supply. The W27C010 provides an electrical chip erase function.

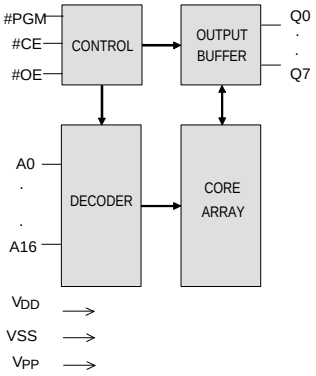
## FEATURES

- High speed access time: 70 nS (max.)
- Read operating current: 30 mA (typ.)
- Erase/Programming operating current: 1 mA (typ.)
- Standby current: 5 µA (typ.)
- Single 5V power supply
- +14V erase/+12V programming voltage
- Fully static operation
- All inputs and outputs directly TTL/CMOS compatible
- Three-state outputs
- Available packages: 32-pin 600 mil DIP, 32-lead PLCC and STSOP

## PIN CONFIGURATIONS




## BLOCK DIAGRAM




## PIN DESCRIPTION

| SYMBOL | DESCRIPTION |
|---|---|
| A0–A16 | Address Inputs |
| Q0–Q7 | Data Inputs/Outputs |
| #CE | Chip Enable |
| #OE | Output Enable |
| #PGM | Program Enable |
| VPP | Program/Erase Supply Voltage |
| VDD | Power Supply |
| Vss | Ground |
| NC | No Connection |



*Publication Release Date: June 2001*
*Revision A4*

## FUNCTIONAL DESCRIPTION

### Read Mode

Like conventional UVEPROMs, the W27C010 has two control functions, both of which produce data at the outputs.

#CE is for power control and chip select. #OE controls the output buffer to gate data to the output pins. When addresses are stable, the address access time ($T_{ACC}$) is equal to the delay from #CE to output ($T_{CE}$), and data are available at the outputs $T_{OE}$ after the falling edge of #OE, if $T_{ACC}$ and $T_{CE}$ timings are met.

### Erase Mode

The erase operation is the only way to change data from "0" to "1." Unlike conventional UVEPROMs, which use ultraviolet light to erase the contents of the entire chip (a procedure that requires up to half an hour), the W27C010 uses electrical erasure. Generally, the chip can be erased within 100 mS by using an EPROM writer with a special erase algorithm.

Erase mode is entered when $V_{PP}$ is raised to $V_{PE}$ (14V), $V_{DD}$= $V_{CE}$ (5V), #CE = $V_{IL}$, (0.8V or below but higher than Vss), #OE = $V_{IH}$ (2V or above but lower than $V_{DD}$), A9 = $V_{HH}$ (14V), A0 = $V_{IL}$, and all other address pins equal $V_{IL}$ and data input pins equal $V_{IH}$. Pulsing #PGM low starts the erase operation.

### Erase Verify Mode

After an erase operation, all of the bytes in the chip must be verified to check whether they have been successfully erased to "1" or not. The erase verify mode automatically ensures a substantial erase margin. This mode will be entered after the erase operation if $V_{PP}$ = $V_{PE}$ (14V), #CE = $V_{IL}$, and #OE = $V_{IL}$, #PGM = $V_{IH}$.

### Program Mode

Programming is performed exactly as it is in conventional UVEPROMs, and programming is the only way to change cell data from "1" to "0." The program mode is entered when $V_{PP}$ is raised to $V_{PP}$ (12V), $V_{DD}$ = $V_{CP}$ (5V), #CE = $V_{IL}$, #OE = $V_{IH}$, the address pins equal the desired addresses, and the input pins equal the desired inputs. Pulsing #PGM low starts the programming operation.

### Program Verify Mode

All of the bytes in the chip must be verified to check whether they have been successfully programmed with the desired data or not. Hence, after each byte is programmed, a program verify operation should be performed. The program verify mode automatically ensures a substantial program margin. This mode will be entered after the program operation if $V_{PP}$ = $V_{PP}$ (12V), #CE = $V_{IL}$, #OE = $V_{IL}$, and #PGM = $V_{IH}$.

### Erase/Program Inhibit

Erase or program inhibit mode allows parallel erasing or programming of multiple chips with different data. When #CE = $V_{IH}$, erasing or programming of non-target chips is inhibited, so that except for the #CE, the W27C010 may have common inputs.

### Standby Mode

The standby mode significantly reduces VDD current. This mode is entered when #CE = VIH. In standby mode, all outputs are in a high impedance state, independent of #OE and #PGM.

### Two-line Output Control

Since EPROMs are often used in large memory arrays, the W27C010 provides two control inputs for multiple memory connections. Two-line control provides for lowest possible memory power dissipation and ensures that data bus contention will not occur.

### System Considerations

EPROM power switching characteristics require careful device decoupling. System designers are concerned with three supply current issues: standby current levels (ISB), active current levels (ICC), and transient current peaks produced by the falling and rising edges of #CE. Transient current magnitudes depend on the device output's capacitive and inductive loading. Two-line control and proper decoupling capacitor selection will suppress transient voltage peaks. Each device should have a 0.1 µF ceramic capacitor connected between its VDD and Vss. This high frequency, low inherent-inductance capacitor should be placed as close as possible to the device. Additionally, for every eight devices, a 4.7 µF electrolytic capacitor should be placed at the array's power supply connection between VDD and Vss. The bulk capacitor will overcome voltage slumps caused by PC board trace inductances.

## TABLE OF OPERATING MODES

VPP = 12V, VPE = 14V, VHH = 12V, VCP = 5V, X = VIH or VIL

| MODE | PINS | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | #CE | #OE | #PGM | A0 | A9 | VDD | VPP | OUTPUTS |
| Read | VIL | VIL | X | X | X | VDD | VDD | DOUT |
| Output Disable | VIL | VIH | X | X | X | VDD | VDD | High Z |
| Standby (TTL) | VIH | X | X | X | X | VDD | VDD | High Z |
| Standby (CMOS) | VDD ±0.3V | X | X | X | X | VDD | VDD | High Z |
| Program | VIL | VIH | VIL | X | X | VCP | VPP | DIN |
| Program Verify | VIL | VIL | VIH | X | X | VCP | VPP | DOUT |
| Program Inhibit | VIH | X | X | X | X | VCP | VPP | High Z |
| Erase | VIL | VIH | VIL | VIL | VPE | VDD | VPE | FF (Hex) |
| Erase Verify | VIL | VIL | VIH | X | X | VDD | VPE | DOUT |
| Erase Inhibit | VIH | X | X | X | X | VCP | VPE | High Z |
| Product Identifier-manufacturer | VIL | VIL | X | VIL | VHH | VDD | VDD | DA (Hex) |
| Product Identifier-device | VIL | VIL | X | VIH | VHH | VDD | VDD | 01 (Hex) |

## DC CHARACTERISTICS

### Absolute Maximum Ratings

| PARAMETER | RATING | UNIT |
|---|---|---|
| Ambient Temperature with Power Applied | -55 to +125 | °C |
| Storage Temperature | -65 to +125 | °C |
| Voltage on all Pins with Respect to Ground Except $V_{DD}$, $V_{PP}$ and A9 Pins | -0.5 to $V_{DD}$ +0.5 | V |
| Voltage on $V_{DD}$ Pin with Respect to Ground | -0.5 to +7 | V |
| Voltage on $V_{PP}$ Pin with Respect to Ground | -0.5 to +14.5 | V |
| Voltage on A9 Pin with Respect to Ground | -0.5 to +14.5 | V |

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

### DC Erase Characteristics

($T_A$ = 25° C ±5° C, $V_{DD}$ = 5.0V ±5%, $V_{HH}$ = 14V)

| PARAMETER | SYM. | CONDITIONS | LIMITS | | | UNIT |
|---|---|---|---|---|---|---|
| | | | MIN. | TYP. | MAX. | |
| Input Load Current | $I_{LI}$ | $V_{IN}$ = $V_{IL}$ or $V_{IH}$ | -10 | - | 10 | µA |
| $V_{DD}$ Erase Current | $I_{CP}$ | #CE = $V_{IL}$, #OE = $V_{IH}$, #PGM = $V_{IL}$, A9 = $V_{HH}$ | - | - | 30 | mA |
| $V_{PP}$ Erase Current | $I_{PP}$ | #CE = $V_{IL}$, #OE = $V_{IH}$, #PGM = $V_{IL}$, A9 = $V_{HH}$ | - | - | 30 | mA |
| Input Low Voltage | $V_{IL}$ | - | -0.3 | - | 0.8 | V |
| Input High Voltage | $V_{IH}$ | - | 2.4 | - | 5.5 | V |
| Output Low Voltage (Verify) | $V_{OL}$ | $I_{OL}$ = 2.1 mA | - | - | 0.45 | V |
| Output High Voltage (Verify) | $V_{OH}$ | $I_{OH}$ = -0.4 mA | 2.4 | - | - | V |
| A9 Erase Voltage | $V_{ID}$ | - | 13.75 | 14.0 | 14.25 | V |
| $V_{PP}$ Erase Voltage | $V_{PE}$ | - | 13.75 | 14.0 | 14.25 | V |
| $V_{DD}$ Supply Voltage (Erase) | $V_{CE}$ | - | 4.5 | 5.0 | 5.5 | V |

Note: $V_{DD}$ must be applied simultaneously or before $V_{PP}$ and removed simultaneously or after $V_{PP}$.

## CAPACITANCE

($V_{DD}$ = 5V, TA = 25° C, f = 1 MHz)

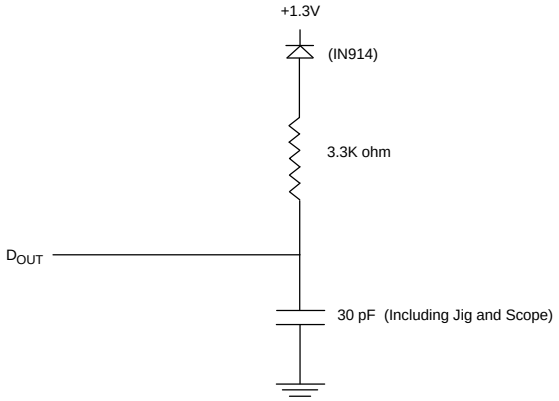
| PARAMETER | SYMBOL | CONDITIONS | MAX. | UNIT |
|---|---|---|---|---|
| Input Capacitance | $C_{IN}$ | $V_{IN}$ = 0V | 6 | pF |
| Output Capacitance | $C_{OUT}$ | $V_{OUT}$ = 0V | 12 | pF |

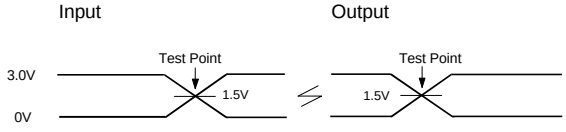
## AC CHARACTERISTICS

### AC Test Conditions

| PARAMETER | CONDITIONS |
|---|---|
| Input Pulse Levels | 0 to 3.0V |
| Input Rise and Fall Times | 5 nS |
| Input and Output Timing Reference Level | 1.5V/1.5V |
| Output Load | $C_L$ = 30 pF, $I_{OH}/I_{OL}$ = -0.4 mA/2.1 mA |

### AC Test Load and Waveforms



## READ OPERATION DC CHARACTERISTICS

($V_{DD}$ = 5.0V ±5%)

| PARAMETER | SYM. | CONDITIONS | LIMITS | | | UNIT |
|---|---|---|---|---|---|---|
| | | | MIN. | TYP. | MAX. | |
| Input Load Current | $I_{LI}$ | $V_{IN}$ = 0V to $V_{DD}$ | -5 | - | 5 | µA |
| Output Leakage Current | $I_{LO}$ | $V_{OUT}$ = 0V to $V_{DD}$ | -10 | - | 10 | µA |
| Standby $V_{DD}$ Current (TTL input) | $I_{SB}$ | #CE = $V_{IH}$ | - | - | 1.0 | mA |
| Standby $V_{DD}$ Current (CMOS input) | $I_{SB1}$ | #CE = $V_{DD}$ ±0.2V | - | 5 | 100 | µA |
| $V_{DD}$ Operating Current | $I_{CC}$ | #CE = $V_{IL}$<br>$I_{OUT}$ = 0 mA<br>f = 5 MHz | - | - | 30 | mA |
| $V_{PP}$ Operating Current | $I_{PP}$ | $V_{PP}$ = $V_{DD}$ | - | - | 10 | µA |
| Input Low Voltage | $V_{IL}$ | - | -0.3 | - | 0.6 | V |
| Input High Voltage | $V_{IH}$ | - | 2.2 | - | $V_{DD}$ +0.5 | V |
| Output Low Voltage | $V_{OL}$ | $I_{OL}$ = 2.1 mA | - | - | 0.45 | V |
| Output High Voltage | $V_{OH}$ | $I_{OH}$ = -0.4 mA | 2.4 | - | - | V |
| $V_{PP}$ Operating Voltage | $V_{PP}$ | - | $V_{DD}$ -0.7 | - | $V_{DD}$ | V |

## READ OPERATION AC CHARACTERISTICS

($V_{DD}$ = 5.0V ±5%, $T_A$ = 0 to 70° C)

| PARAMETER | SYM. | W27C010-70 | | UNIT |
|---|---|---|---|---|
| | | MIN. | MAX. | |
| Read Cycle Time | $T_{RC}$ | 70 | - | nS |
| Chip Enable Access Time | $T_{CE}$ | - | 70 | nS |
| Address Access Time | $T_{ACC}$ | - | 70 | nS |
| Output Enable Access Time | $T_{OE}$ | - | 30 | nS |
| #OE High to High-Z Output | $T_{DF}$ | - | 25 | nS |
| Output Hold from Address Change | $T_{OH}$ | 0 | - | nS |

Note: $V_{DD}$ must be applied simultaneously or before $V_{PP}$ and removed simultaneously or after $V_{PP}$.

## DC PROGRAMMING CHARACTERISTICS

($V_{DD}$ = 5.0V ±5%, TA = 25° C ±5° C)

| PARAMETER | SYM. | CONDITIONS | LIMITS | | | UNIT |
|---|---|---|---|---|---|---|
| | | | MIN. | TYP. | MAX. | |
| Input Load Current | $I_{LI}$ | $V_{IN} = V_{IL}$ or $V_{IH}$ | - | - | 10 | µA |
| $V_{DD}$ Program Current | $I_{CP}$ | #CE = $V_{IL}$, #OE = $V_{IH}$, #PGM = $V_{IL}$ | - | - | 30 | mA |
| $V_{PP}$ Program Current | $I_{PP}$ | #CE = $V_{IL}$, #OE = $V_{IH}$, #PGM = $V_{IL}$ | - | - | 30 | mA |
| Input Low Voltage | $V_{IL}$ | - | -0.3 | - | 0.8 | V |
| Input High Voltage | $V_{IH}$ | - | 2.4 | - | 5.5 | V |
| Output Low Voltage (Verify) | $V_{OL}$ | $I_{OL}$ = 2.1 mA | - | - | 0.45 | V |
| Output High Voltage (Verify) | $V_{OH}$ | $I_{OH}$ = -0.4 mA | 2.4 | - | - | V |
| A9 Silicon I.D. Voltage | $V_{ID}$ | - | 11.5 | 12.0 | 12.5 | V |
| $V_{PP}$ Program Voltage | $V_{PP}$ | - | 11.75 | 12.0 | 12.25 | V |
| $V_{DD}$ Supply Voltage (Program) | $V_{CP}$ | - | 4.5 | 5.0 | 5.5 | V |

## AC PROGRAMMING/ERASE CHARACTERISTICS

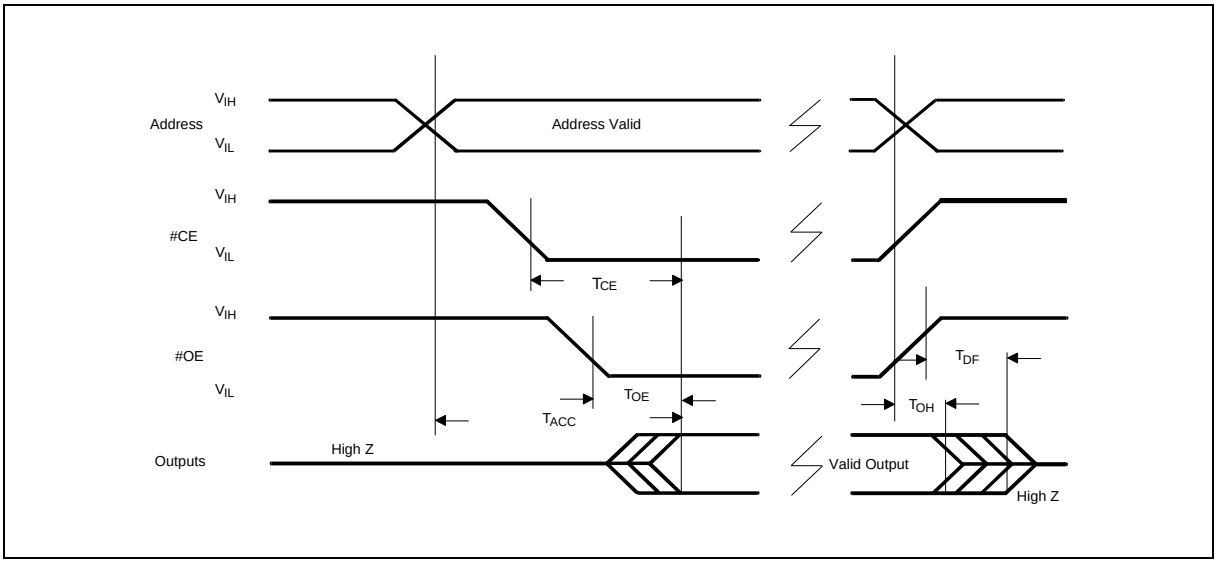
($V_{DD}$ = 5.0V ±5%, TA = 25° C ±5° C)

| PARAMETER | SYM. | LIMITS | | | UNIT |
|---|---|---|---|---|---|
| | | MIN. | TYP. | MAX. | |
| $V_{PP}$ Setup Time | $T_{VPS}$ | 2.0 | - | - | µS |
| Address Setup Time | $T_{AS}$ | 2.0 | - | - | µS |
| Data Setup Time | $T_{DS}$ | 2.0 | - | - | µS |
| #PGM Program Pulse Width | $T_{PWP}$ | 95 | 100 | 105 | µS |
| #PGM Erase Pulse Width | $T_{PWE}$ | 95 | 100 | 105 | mS |
| Data Hold Time | $T_{DH}$ | 2.0 | - | - | µS |
| #OE Setup Time | $T_{OES}$ | 2.0 | - | - | µS |
| Data Valid from #OE | $T_{OEV}$ | - | - | 150 | nS |
| #OE High to Output High Z | $T_{DFP}$ | 0 | - | 130 | nS |
| Address Hold Time after #PGM High | $T_{AH}$ | 0 | - | - | µS |
| Address Hold Time (Erase) | $T_{AHE}$ | 2.0 | - | - | µS |
| #CE Setup Time | $T_{CES}$ | 2.0 | - | - | µS |

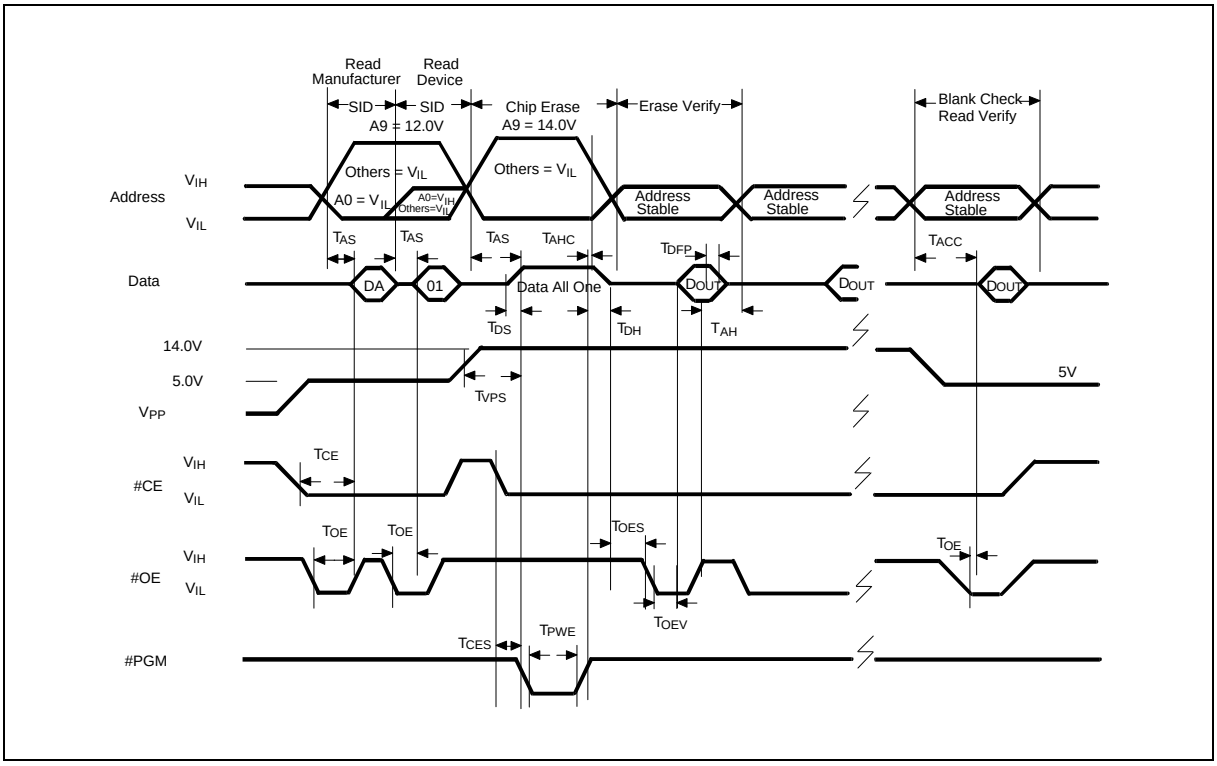
Note: $V_{DD}$ must be applied simultaneously or before $V_{PP}$ and removed simultaneously or after $V_{PP}$.

## TIMING WAVEFORMS

### AC Read Waveform

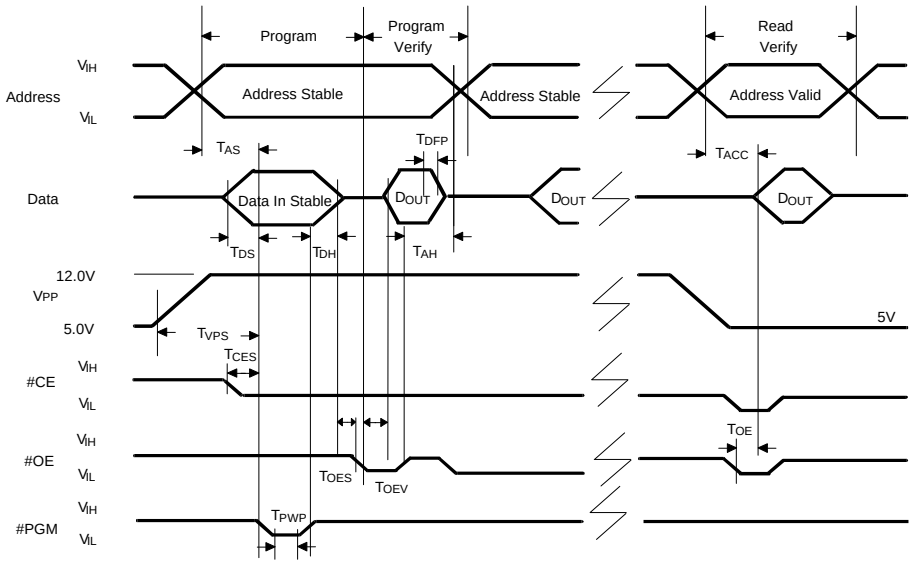



### Erase Waveform

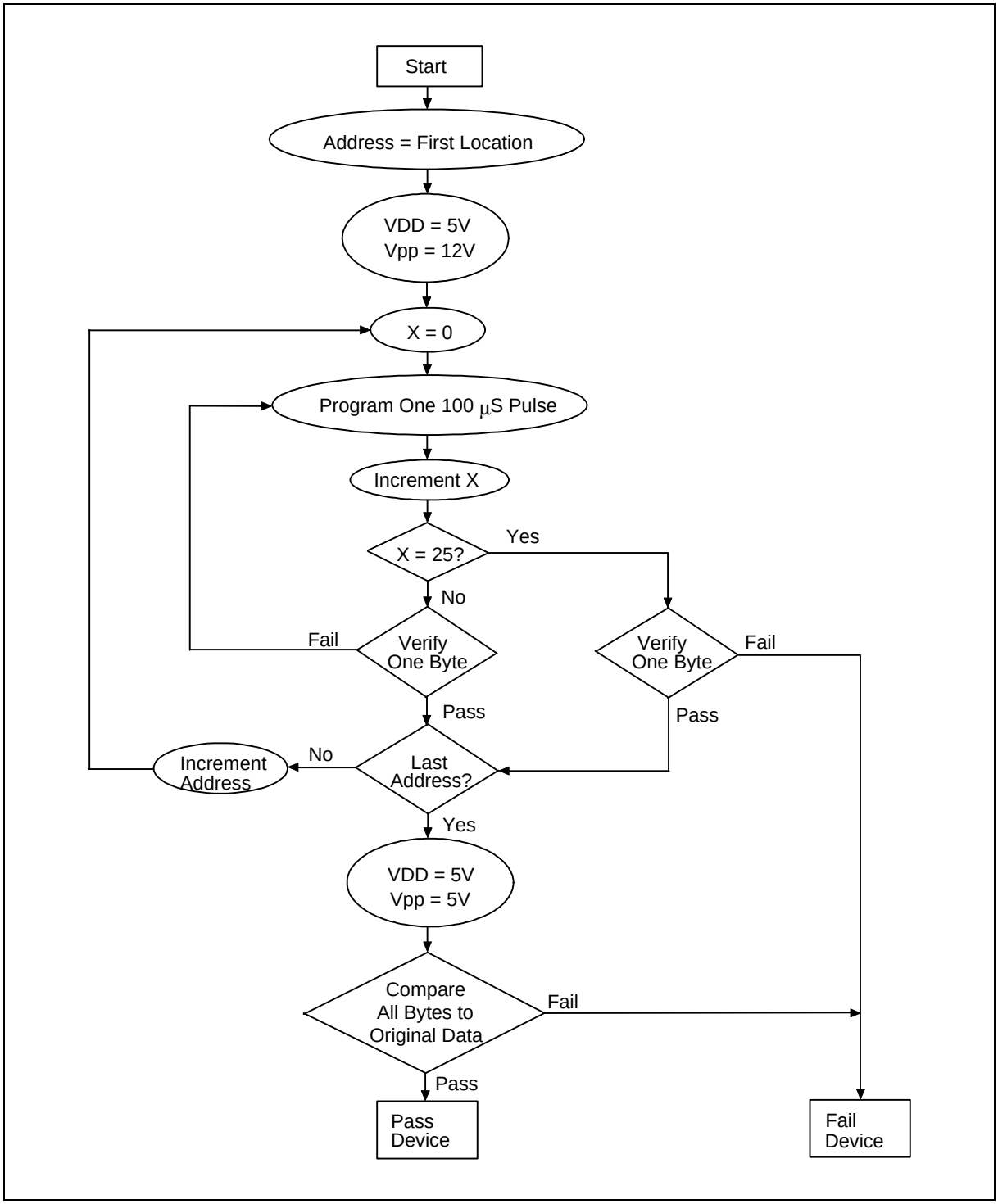


Timing Waveforms, continued

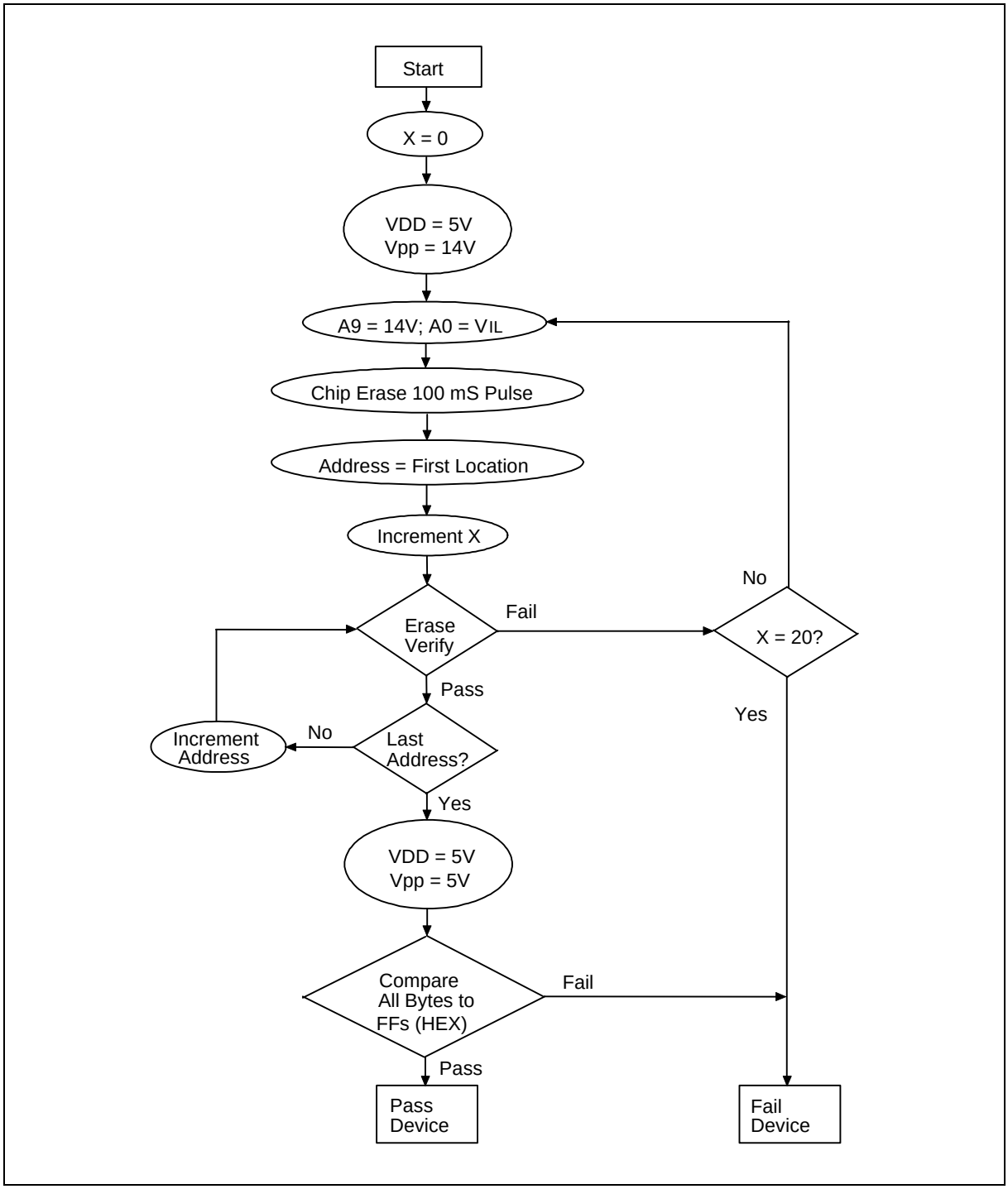
## Programming Waveform



## SMART PROGRAMMING ALGORITHM



## SMART ERASE ALGORITHM



## ORDERING INFORMATION

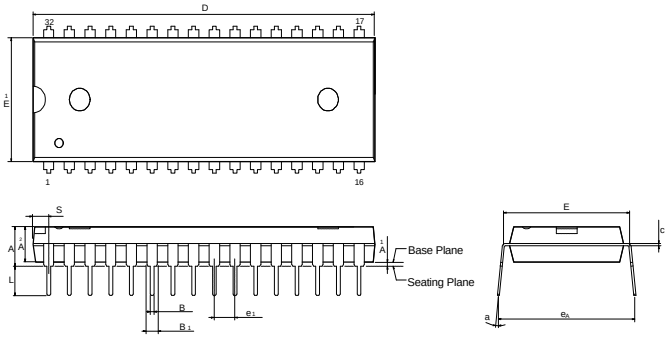
| PART NO. | ACCESS TIME (nS) | POWER SUPPLY CURRENT MAX. (mA) | STANDBY $V_{DD}$ CURRENT MAX. (μA) | PACKAGE |
|---|---|---|---|---|
| W27C010-70 | 70 | 30 | 100 | 600 mil DIP |
| W27C010P-70 | 70 | 30 | 100 | 32-Lead PLCC |
| W27C010Q-70 | 70 | 30 | 100 | 32-Lead STSOP (8 x 14 mm) |

Notes:

1. Winbond reserves the right to make changes to its products without prior notice.
2. Purchasers are responsible for performing appropriate quality assurance testing on products intended for use in applications where personal injury might occur as a consequence of product failure.

## PACKAGE DIMENSIONS

### 32-pin P-DIP

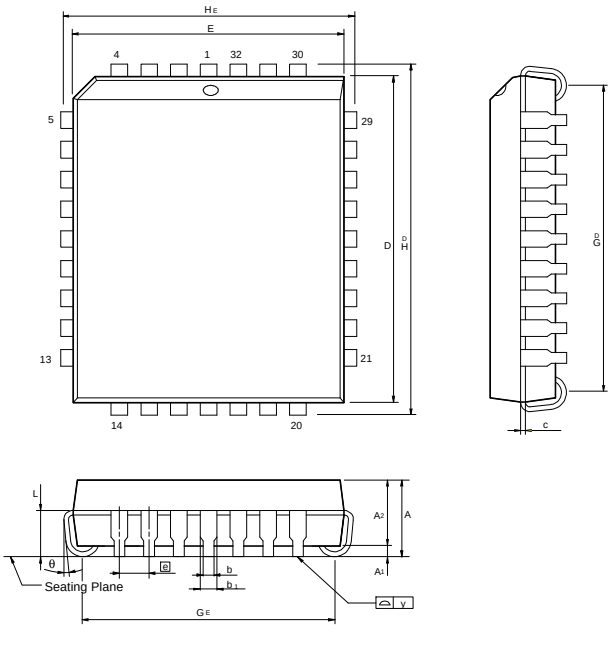



| Symbol | Dimension in Inches | | | Dimension in mm | | |
|---|---|---|---|---|---|---|
| | Min. | Nom. | Max. | Min. | Nom. | Max. |
| A | — | — | 0.210 | — | — | 5.33 |
| $A_1$ | 0.010 | — | — | 0.25 | — | — |
| $A_2$ | 0.150 | 0.155 | 0.160 | 3.81 | 3.94 | 4.06 |
| B | 0.016 | 0.018 | 0.022 | 0.41 | 0.46 | 0.56 |
| $B_1$ | 0.048 | 0.050 | 0.054 | 1.22 | 1.27 | 1.37 |
| c | 0.008 | 0.010 | 0.014 | 0.20 | 0.25 | 0.36 |
| D | — | 1.650 | 1.660 | — | 41.91 | 42.16 |
| E | 0.590 | 0.600 | 0.610 | 14.99 | 15.24 | 15.49 |
| $E_1$ | 0.540 | 0.550 | 0.555 | 13.84 | 13.97 | 14.10 |
| $e_1$ | 0.090 | 0.100 | 0.110 | 2.29 | 2.54 | 2.79 |
| L | 0.120 | 0.130 | 0.140 | 3.05 | 3.30 | 3.56 |
| a | 0 | — | 15 | 0 | — | 15 |
| $e_A$ | 0.630 | 0.650 | 0.670 | 16.00 | 16.51 | 17.02 |
| S | — | — | 0.085 | — | — | 2.16 |

Notes:

1. Dimensions D Max. & S include mold flash o tie bar burrs.
2. Dimension E1 does not include interlead flas
3. Dimensions D & E1 include mold mismatch a are determined at the mold parting line.
4. Dimension B1 does not include dambar protrusion/intrusion.
5. Controlling dimension: Inches.
6. General appearance spec. should be based o final visual inspection spec.

### 32-Lead PLCC



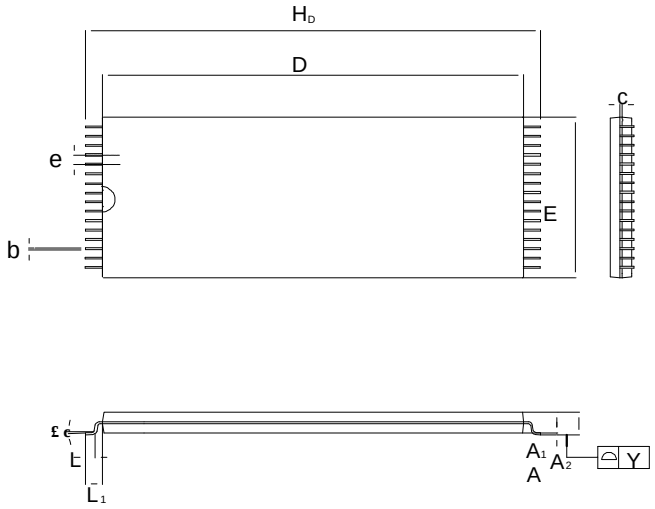

| Symbol | Dimension in Inches | | | Dimension in mm | | |
|---|---|---|---|---|---|---|
| | Min. | Nom. | Max. | Min. | Nom. | Max. |
| A | — | — | 0.140 | — | — | 3.56 |
| $A_1$ | 0.020 | — | — | 0.50 | — | — |
| $A_2$ | 0.105 | 0.110 | 0.115 | 2.67 | 2.80 | 2.93 |
| $b_1$ | 0.026 | 0.028 | 0.032 | 0.66 | 0.71 | 0.81 |
| b | 0.016 | 0.018 | 0.022 | 0.41 | 0.46 | 0.56 |
| c | 0.008 | 0.010 | 0.014 | 0.20 | 0.25 | 0.35 |
| D | 0.547 | 0.550 | 0.553 | 13.89 | 13.97 | 14.05 |
| E | 0.447 | 0.450 | 0.453 | 11.35 | 11.43 | 11.51 |
| e | 0.044 | 0.050 | 0.056 | 1.12 | 1.27 | 1.42 |
| $G_D$ | 0.490 | 0.510 | 0.530 | 12.45 | 12.95 | 13.46 |
| $G_E$ | 0.390 | 0.410 | 0.430 | 9.91 | 10.41 | 10.92 |
| $H_D$ | 0.585 | 0.590 | 0.595 | 14.86 | 14.99 | 15.11 |
| $H_E$ | 0.485 | 0.490 | 0.495 | 12.32 | 12.45 | 12.57 |
| L | 0.075 | 0.090 | 0.095 | 1.91 | 2.29 | 2.41 |
| y | — | — | 0.004 | — | — | 0.10 |
| θ | 0 ° | — | 10 ° | 0 ° | — | 10 ° |

Notes:

1. Dimensions D & E do not include interlead flash.
2. Dimension b does not include dambar protrusion/intrusion.
3. Controlling dimension: Inches.
4. General appearance spec. should be based onfinal visual inspection sepc.

Package Dimensions, continued

## 32-Lead Small Type One TSOP (8mm x 14mm)




| Symbol | Dimension in Inches | | | Dimension in mm | | |
|---|---|---|---|---|---|---|
| | Min. | Nom. | Max. | Min. | Nom. | Max. |
| A | | | 0.047 | | | 1.20 |
| $A_1$ | 0.002 | | 0.006 | 0.05 | | 0.15 |
| $A_2$ | 0.035 | 0.040 | 0.041 | 0.95 | 1.00 | 1.05 |
| b | 0.007 | 0.009 | 0.010 | 0.17 | 0.22 | 0.27 |
| c | 0.004 | ----- | 0.008 | 0.10 | ----- | 0.21 |
| D | | 0.488 | | | 12.40 | |
| E | | 0.315 | | | 8.00 | |
| $H_D$ | | 0.551 | | | 14.00 | |
| e | | 0.020 | | | 0.50 | |
| L | 0.020 | 0.024 | 0.028 | 0.50 | 0.60 | 0.70 |
| $L_1$ | | 0.031 | | | 0.80 | |
| Y | 0.000 | | 0.004 | 0.00 | | 0.10 |
| θ | 0 | 3 | 5 | 0 | 3 | 5 |

## VERSION HISTORY

| VERSION | DATE | PAGE | DESCRIPTION |
|---|---|---|---|
| A1 | May. 1997 | - | Initial Issued |
| A2 | Aug. 1997 | 1, 5, 6, 12 | Add 70 nS bining |
| A3 | Jun. 2001 | 1, 12, 14 | Add in 32-lead STSOP package |
| | | all | Change Vcc to VDD; GND to Vss |
| | | 1, 12, 14 | Delete SOP package |
| | | 14 | Correct STSOP package diagram |
| A4 | Jun. 2001 | 1 | Correct STSOP pin configuration |
| | | 1, 5, 6, 12 | Delete 150 nS bining |

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