



# SDRAM Buffer - 4 DIMM

## Features

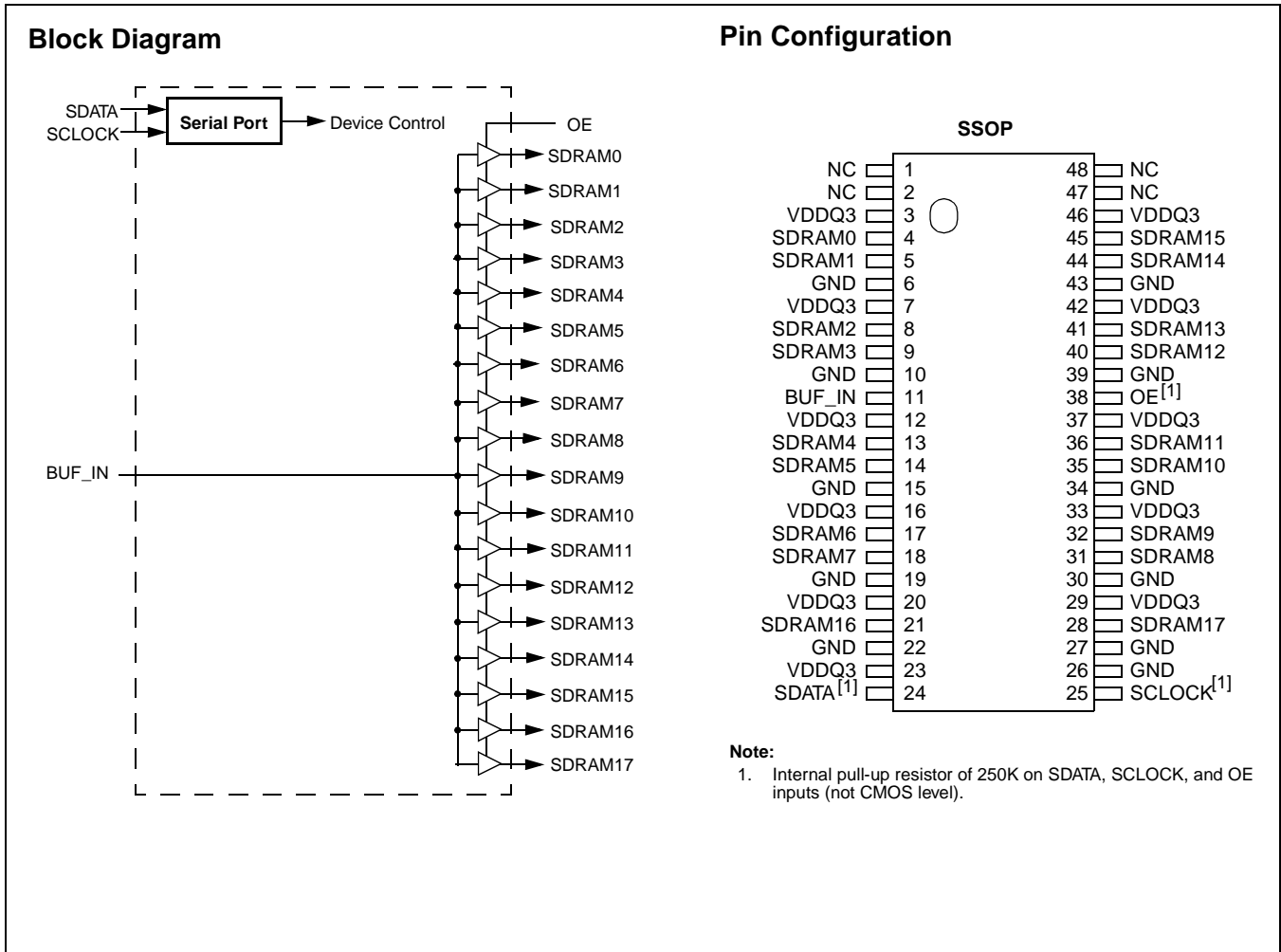
- Eighteen skew controlled CMOS outputs (SDRAM0:17)
- Supports four SDRAM DIMMs
- Ideal for high-performance systems designed around Intel®'s 440BX chip set
- SMBus serial configuration interface
- Output skew between any two outputs is less than 250 ps
- 1 to 5 ns propagation delay
- DC to 133-MHz operation
- Single 3.3V supply voltage
- Low power CMOS design packaged in a 48-pin SSOP (Small Shrink Outline Package)

## Overview

The Cypress W40S01-04 is a low-voltage, eighteen-output signal buffer. Output buffer impedance is approximately 15Ω which is ideal for driving SDRAM DIMMs.

## Key Specifications

Supply Voltages: .....  $V_{DDQ3} = 3.3V \pm 5\%$   
 Operating Temperature: ..... 0°C to +70°C  
 Input Threshold: ..... 1.5V typical  
 Maximum Input Voltage: .....  $V_{DDQ3} + 0.5V$   
 Input Frequency: ..... 0 to 133 MHz  
 BUF\_IN to SDRAM0:17 Propagation Delay: ..... 1.0 to 5.0 ns  
 Output Edge Rate: .....  $\geq 1.5 V/ns$   
 Output Skew: .....  $\pm 250 ps$   
 Output Duty Cycle: ..... 45/55% worst case  
 Output Impedance: ..... 15Ω typical  
 Output Type: ..... CMOS rail-to-rail  
 Part to Part Skew: ..... 700 ps



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**Pin Definitions**

Pin Name	Pin No.	Pin Type	Pin Description
SDRAM0:17	4, 5, 8, 9, 13, 14, 17, 18, 21, 28, 31, 32, 35, 36, 40, 41, 44, 45	O	<b>SDRAM Outputs:</b> Provides buffered copy of BUF_IN. The propagation delay from a rising input edge to a rising output edge is 1 to 5 ns. All outputs are skew controlled to within $\pm 250$ ps of each other.
BUF_IN	11	I	<b>Clock Input:</b> This clock input has an input threshold voltage of 1.5V (typ).
SDATA	24	I/O	<b>SMBus Data Input:</b> Data should be presented to this input as described in the I <sup>2</sup> C section of this data sheet. Internal 250-k $\Omega$ pull-up resistor.
SCLOCK	25	I	<b>SMBus clock Input:</b> The SMBus data clock should be presented to this input as described in the SMBus section of this data sheet. Internal 250-k $\Omega$ pull-up resistor.
VDDQ3	3, 7, 12, 16, 20, 23, 29, 33, 37, 42, 46	P	<b>Power Connection:</b> Power supply for core logic and output buffers. Connected to 3.3V supply.
GND	6, 10, 15, 19, 22, 26, 27, 30, 34, 39, 43	G	<b>Ground Connection:</b> Connect all ground pins to the common system ground plane.
OE	38	I	<b>Output Enable:</b> Internal 250-k $\Omega$ pull-up resistor. Three-states outputs when LOW.
NC	1, 2, 47, 48	-	<b>No Connect:</b> Do not connect.

## Functional Description

### Output Control Pins

Outputs three-stated when OE = 0, and toggle when OE = 1. Outputs are in phase with BUF\_IN but are phase delayed by 1 to 5 ns. Outputs can also be controlled via the SMBus interface.

### Output Drivers

The W40S01-04 output buffers are CMOS type which deliver a rail-to-rail (GND to  $V_{DD}$ ) output voltage swing into a nominal capacitive load. Thus, output signaling is both TTL and CMOS level compatible. Nominal output buffer impedance is  $15\Omega$ .

### Operation

Data is written to the W40S01-04 in ten bytes of eight bits each. Bytes are written in the order shown in *Table 1*.

**Table 1. Byte Writing Sequence**

Byte Sequence	Byte Name	Bit Sequence	Byte Description
1	Slave Address	11010010	Commands the W40S01-04 to accept the bits in Data Bytes 0-6 for internal register configuration. Since other devices may exist on the same common serial data bus, it is necessary to have a specific slave address for each potential receiver. The slave receiver address for the W40S01-04 is 11010010. Register setting will not be made if the Slave Address is not correct (or is for an alternate slave receiver).
2	Command Code	Don't Care	Unused by the W40S01-04, therefore bit values are ignored (don't care). This byte must be included in the data write sequence to maintain proper byte allocation. The Command Code Byte is part of the standard serial communication protocol and may be used when writing to another addressed slave receiver on the serial data bus.
3	Byte Count	Don't Care	Unused by the W40S01-04, therefore bit values are ignored (don't care). This byte must be included in the data write sequence to maintain proper byte allocation. The Byte Count Byte is part of the standard serial communication protocol and may be used when writing to another addressed slave receiver on the serial data bus.
4	Data Byte 0	Refer to <i>Table 2</i>	The data bits in these bytes set internal W40S01-04 registers that control device operation. The data bits are only accepted when the Address Byte bit sequence is 11010010, as noted above. For description of bit control functions, refer to <i>Table 2</i> , Data Byte Serial Configuration Map.
5	Data Byte 1		
6	Data Byte 2		
7	Data Byte 3	Don't Care	Refer to Cypress clock drivers.
8	Data Byte 4		
9	Data Byte 5		
10	Data Byte 6		

**Writing Data Bytes**

Each bit in the data bytes control a particular device function. Bits are written MSB (most significant bit) first, which is bit 7.

Table 2 gives the bit formats for registers located in Data Bytes 0–6.

**Table 2. Data Bytes 0–2 Serial Configuration Map<sup>[2]</sup>**

Bit(s)	Affected Pin		Control Function	Bit Control	
	Pin No.	Pin Name		0	1
<b>Data Byte 0 SDRAM Active/Inactive Register (1 = Enable, 0 = Disable)</b>					
7	18	SDRAM7	Clock Output Disable	Low	Active
6	17	SDRAM6	Clock Output Disable	Low	Active
5	14	SDRAM5	Clock Output Disable	Low	Active
4	13	SDRAM4	Clock Output Disable	Low	Active
3	9	SDRAM3	Clock Output Disable	Low	Active
2	8	SDRAM2	Clock Output Disable	Low	Active
1	5	SDRAM1	Clock Output Disable	Low	Active
0	4	SDRAM0	Clock Output Disable	Low	Active
<b>Data Byte 1 SDRAM Active/Inactive Register (1 = Enable, 0 = Disable)</b>					
7	45	SDRAM15	Clock Output Disable	Low	Active
6	44	SDRAM14	Clock Output Disable	Low	Active
5	41	SDRAM13	Clock Output Disable	Low	Active
4	40	SDRAM12	Clock Output Disable	Low	Active
3	36	SDRAM11	Clock Output Disable	Low	Active
2	35	SDRAM10	Clock Output Disable	Low	Active
1	32	SDRAM9	Clock Output Disable	Low	Active
0	31	SDRAM8	Clock Output Disable	Low	Active
<b>Data Byte 2 SDRAM Active/Inactive Register (1 = Enable, 0 = Disable)</b>					
7	28	SDRAM17	Clock Output Disable	Low	Active
6	21	SDRAM16	Clock Output Disable	Low	Active
5	N/A	Reserved	(Reserved)	--	--
4	N/A	Reserved	(Reserved)	--	--
3	N/A	Reserved	(Reserved)	--	--
2	N/A	Reserved	(Reserved)	--	--
1	N/A	Reserved	(Reserved)	--	--
0	N/A	Reserved	(Reserved)	--	--

**Note:**

- At power-up all SDRAM outputs are enabled and active. Program Reserved bits to 0.

## How To Use the Serial Data Interface

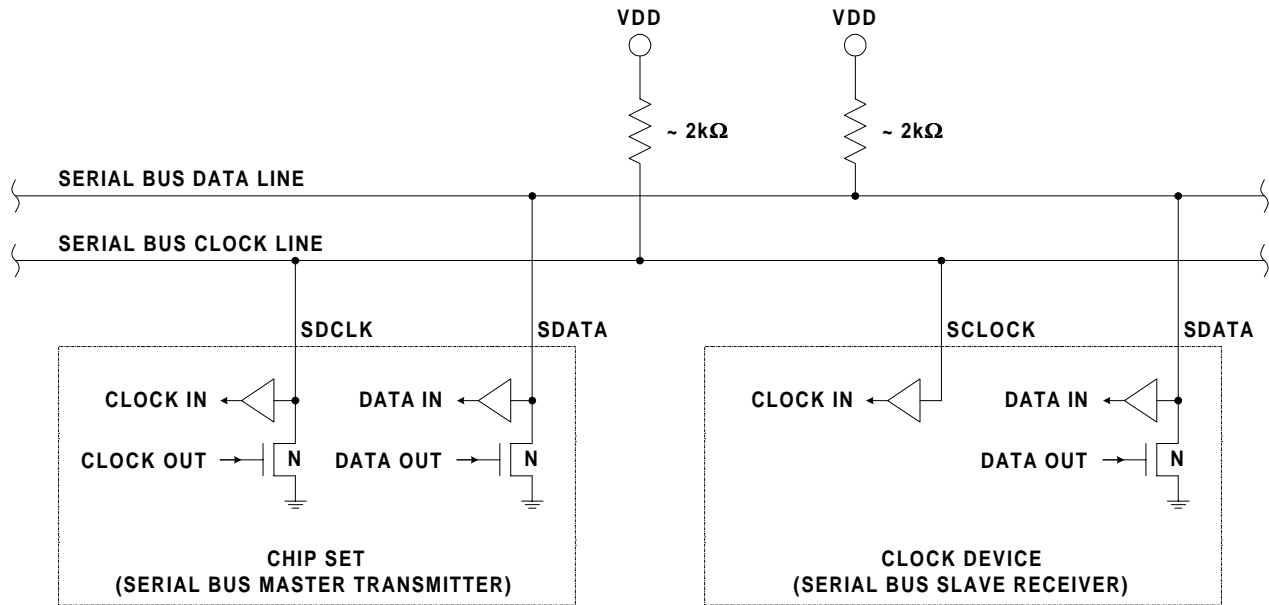
### Electrical Requirements

Figure 1 illustrates electrical characteristics for the serial interface bus used with the W40S01-04. Devices send data over the bus with an open drain logic output that can (a) pull the bus line LOW, or (b) let the bus default to logic 1. The pull-up resistor on the bus (both clock and data lines) establish a default

logic 1. All bus devices generally have logic inputs to receive data.

Although the W40S01-04 is a receive-only device (no data write-back capability), it does transmit an “acknowledge” data pulse after each byte is received. Thus, the SDATA line can both transmit and receive data.

The pull-up resistor should be sized to meet the rise and fall times specified in AC parameters, taking into consideration total bus line capacitance.



**Figure 1. Serial Interface Bus Electrical Characteristics**

### Signaling Requirements

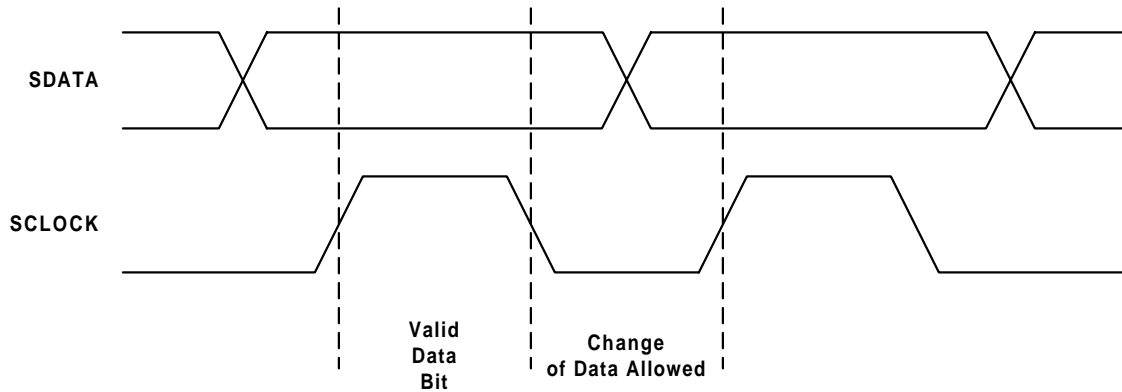
As shown in *Figure 2*, valid data bits are defined as stable logic 0 or 1 condition on the data line during a clock HIGH (logic 1) pulse. A transitioning data line during a clock HIGH pulse may be interpreted as a start or stop pulse (it will be interpreted as a start or stop pulse if the start/stop timing parameters are met).

A write sequence is initiated by a “start bit” as shown in *Figure 3*. A “stop bit” signifies that a transmission has ended.

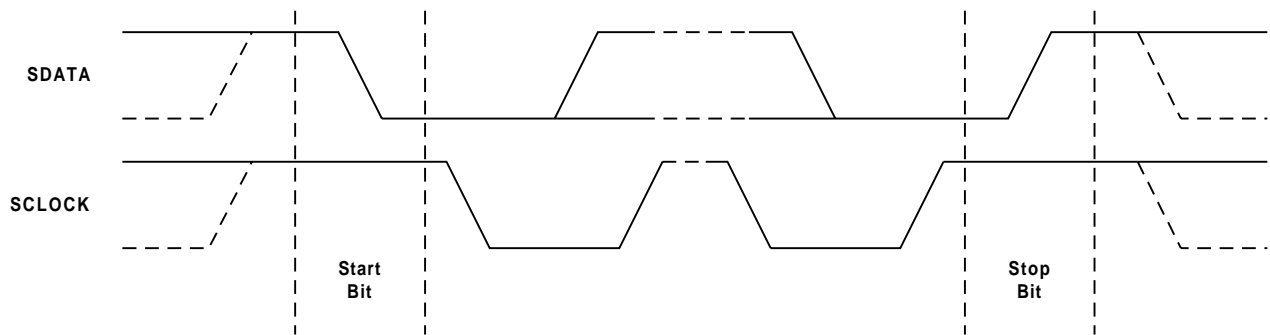
As stated previously, the W40S01-04 sends an “acknowledge” pulse after receiving eight data bits in each byte as shown in *Figure 4*.

### Sending Data to the W40S01-04

The device accepts data once it has detected a valid start bit and address byte sequence. Device functionality is changed upon the receipt of each data bit (registers are not double buffered). Partial transmission is allowed meaning that a transmission can be truncated as soon as the desired data bits are transmitted (remaining registers will be unmodified). Transmission is truncated with either a stop bit or new start bit (restart condition).



**Figure 2. Serial Data Bus Valid Data Bit**



**Figure 3. Serial Data Bus Start and Stop Bit**

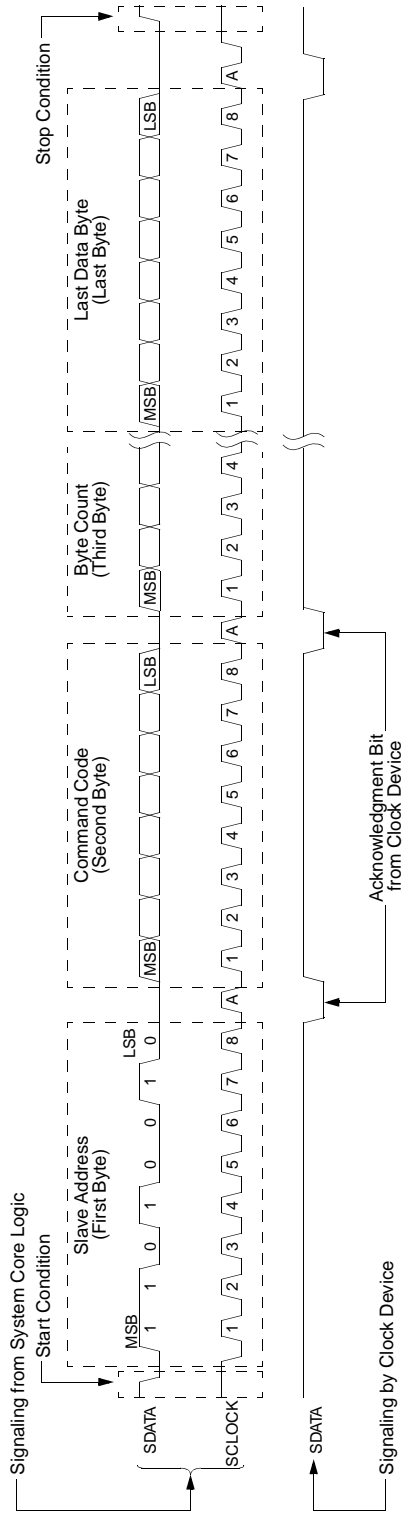


Figure 4. Serial Data Bus Write Sequence

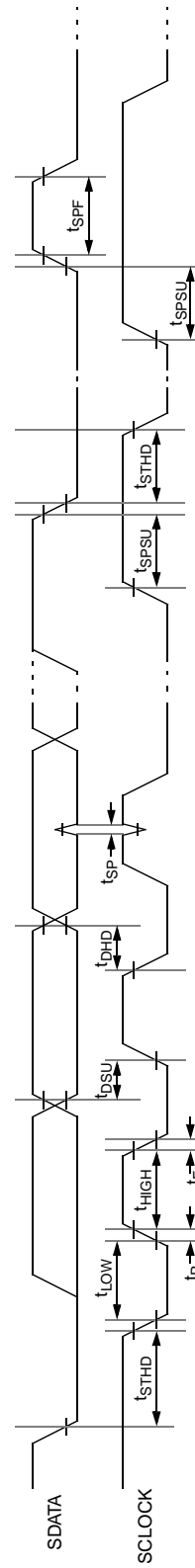


Figure 5. Serial Data Bus Timing Diagram

### Absolute Maximum Ratings

Stresses greater than those listed in this table may cause permanent damage to the device. These represent a stress rating only. Operation of the device at these or any other conditions

above those specified in the operating sections of this specification is not implied. Maximum conditions for extended periods may affect reliability

Parameter	Description	Rating	Unit
$V_{DD}, V_{IN}$	Voltage on any pin with respect to GND	-0.5 to +7.0	V
$T_{STG}$	Storage Temperature	-65 to +150	°C
$T_A$	Operating Temperature	0 to +70	°C
$T_B$	Ambient Temperature under Bias	-55 to +125	°C

### DC Electrical Characteristics: $T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$ , $V_{DDQ3} = 3.3\text{V} \pm 5\%$

Parameter	Description	Test Condition/ Comments	Min.	Typ.	Max.	Unit
$I_{DD}$	3.3V Supply Current	BUF_IN = 100 MHz		320		mA
$I_{DD \text{ Tristate}}$	3.3V Supply Current in Three-state	BUF_IN = 100 MHz		5		mA
<b>Logic Inputs (BUF_IN, OE, SCLOCK, SDATA)</b>						
$V_{IL}$	Input Low Voltage		GND-0.3		0.8	V
$V_{IH}$	Input High Voltage		2.0		$V_{DDQ3}+0.5$	V
$I_{ILEAK}$	Input Leakage Current, BUF_IN		-5		+5	μA
$I_{ILEAK}$	Input Leakage Current <sup>[3]</sup>		-20		+5	μA
<b>Logic Outputs (SDRAM0:17)<sup>[4]</sup></b>						
$V_{OL}$	Output Low Voltage	$I_{OL} = 1 \text{ mA}$			50	mV
$V_{OH}$	Output High Voltage	$I_{OH} = -1 \text{ mA}$	3.1			V
$I_{OL}$	Output Low Current	$V_{OL} = 1.5\text{V}$	70	110	185	mA
$I_{OH}$	Output High Current	$V_{OH} = 1.5\text{V}$	65	100	160	mA
<b>Pin Capacitance/Inductance</b>						
$C_{IN}$	Input Pin Capacitance (Except BUF_IN)				5	pF
$C_{OUT}$	Output Pin Capacitance				6	pF
$L_{IN}$	Input Pin Inductance				7	nH

**Notes:**

3. OE, SCLOCK, and SDATA logic pins have a 250-kΩ internal pull-up resistor (not CMOS level).
4. Outputs loaded by 6" 60Ω transmission lines with 20-pF capacitors.



**AC Electrical Characteristics:**  $T_A = 0^{\circ}\text{C}$  to  $+70^{\circ}\text{C}$ ,  $V_{DDQ3} = 3.3\text{V} \pm 5\%$  (Lump Capacitance Test Load = 30 pF)

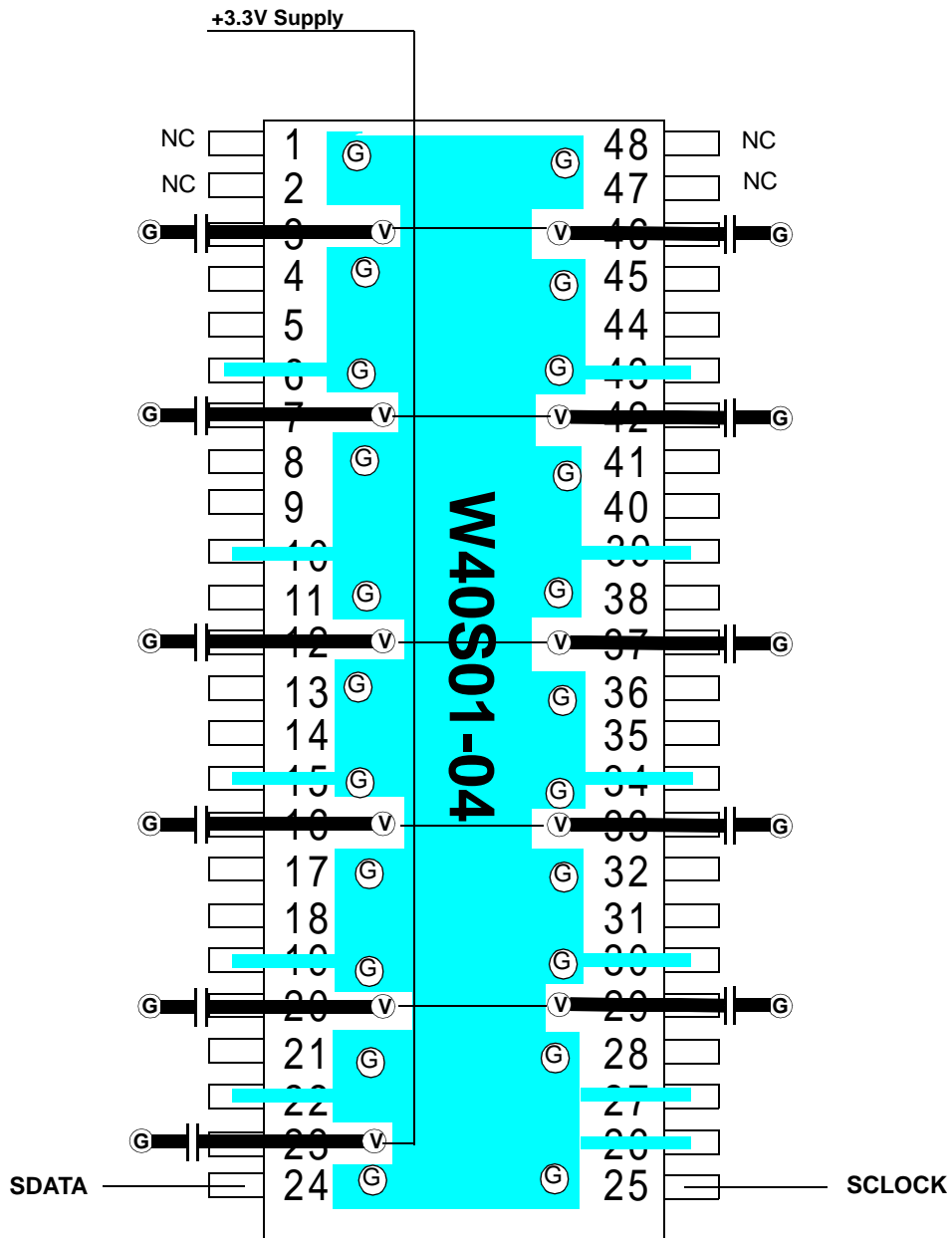
Parameter	Description	Test Condition	Min.	Typ.	Max.	Unit
$f_{IN}$	Input Frequency		0		133	MHz
$t_R$	Output Rise Edge Rate	Measured from 0.4V to 2.4V	1.5		4.0	V/ns
$t_F$	Output Fall Edge Rate	Measured from 2.4V to 0.4V	1.5		4.0	V/ns
$t_{SR}$	Output Skew, Rising Edges				250	ps
$t_{SF}$	Output Skew, Falling Edges				250	ps
$t_{EN}$	Output Enable Time		1.0		8.0	ns
$t_{DIS}$	Output Disable Time		1.0		8.0	ns
$t_{PR}$	Rising Edge Propagation Delay		1.0		5.0	ns
$t_{PF}$	Falling Edge Propagation Delay		1.0		5.0	ns
$t_D$	Duty Cycle	Measured at 1.5V	45		55	%
$Z_o$	AC Output Impedance			15		$\Omega$
$T_{SPP}$	Part to Part Skew				700	ps

**Ordering Information**

Ordering Code	Freq. Mask Code	Package Name	Package Type
W40S01	04	H	48-pin SSOP (300 mils)

Document #: 38-00811-\*A

Layout Example



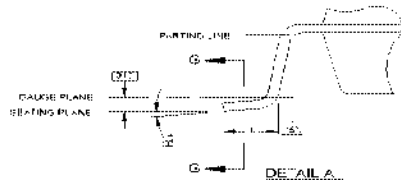
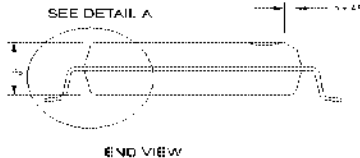
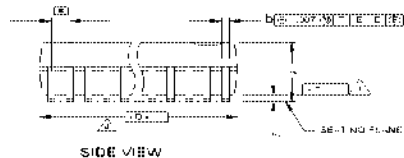
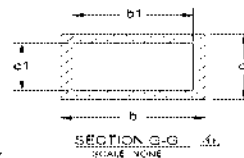
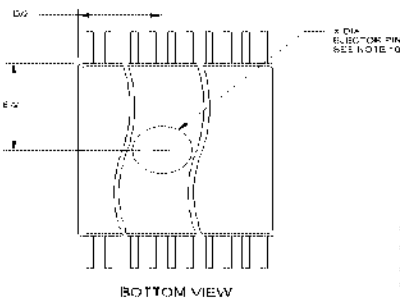
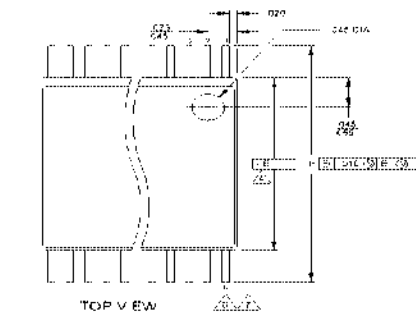
C = 0.1 μF

⊗ = VIA to GND plane layer    ⊙ = VIA to supply plane layer



Package Diagram

48-Pin Shrink Small Outline Package (SSOP, 0.300 inch)



NOTES:

1. MAXIMUM LEAD THICKNESS ALLOWABLE IS .025
2. DIMENSIONING & TOLERANCING PER ANSI Y14.5M - 1982
3. "T" IS A REFERENCE DATUM.
4. "D" & "E" ARE REFERENCE DATUMS AND DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS, BUT DO INCLUDE MOLD MISMATCH AND ARE MEASURED AT THE MOLD PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .003 INCHES PER SIDE.
5. "L" IS THE LENGTH OF TERMINAL FOR SOLDERING TO A SUBSTRATE.
6. "N" IS THE NUMBER OF TERMINAL POSITIONS.
7. TERMINAL POSITIONS ARE SHOWN FOR REFERENCE ONLY.
8. FORMED LEADS SHALL BE PLANAR WITH RESPECT TO ONE ANOTHER WITHIN .004 INCHES AT SEATING PLANE.
9. CONTROLLING DIMENSION INCHES.
10. COUNTRY OF ORIGIN LOCATION AND EJECTOR PIN ON PACKAGE BOTTOM IS OPTIONAL AND DEPENDS ON ASSEMBLY LOCATION.
11. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN .005 INCHES AND .013 INCHES FROM THE LEAD TIPS.
12. THIS PART IS COMPLIANT WITH JEDEC SPECIFICATION MO-118, VARIATIONS AA, AB, EXCEPT CHAMFER DIMENSION F. JEDEC SPECIFICATION FOR THIS IS 0°-7.025°.

DIMENSION	COMMON DIMENSIONS			NOTE VARIATIONS	4 D NOM. MAX.			6 N
	MIN.	NOM.	MAX.		MIN.	NOM.	MAX.	
A	.095	.102	.110	AA	.620	.625	.630	48
A1	.088	.090	.092	AB	.720	.725	.730	56
b	.008	.010	.0135		THIS TABLE IN INCHES			
b1	.008	.010	.012					
c	.005		.010					
c1	.005	.006	.0085					
D	SEE VARIATIONS			4				
E	.292	.295	.299					
e	.025 BSC							
H	.400	.406	.410					
h	.010	.013	.016					
L	.024	.032	.040					
N	SEE VARIATIONS			6				
X	.085	.093	.100	10				
α	0°	5°	8°					

DIMENSION	COMMON DIMENSIONS			NOTE VARIATIONS	4 D NOM. MAX.			6 N
	MIN.	NOM.	MAX.		MIN.	NOM.	MAX.	
A	2.41	2.59	2.79	AA	15.75	15.88	16.00	48
A1	0.20	0.31	0.41	AB	18.29	18.42	18.54	56
b	0.203	0.254	0.343		THIS TABLE IN MILLIMETERS			
b1	0.203	0.254	0.305					
c	0.127		0.254					
c1	0.127	0.152	0.216					
D	SEE VARIATIONS			4				
E	7.42	7.52	7.59					
e	0.635 BSC							
H	10.16	10.31	10.41					
h	0.25	0.33	0.41					
L	0.61	0.81	1.02					
N	SEE VARIATIONS			6				
X	2.16	2.36	2.54	10				
α	0°	5°	8°					