W83977TF

WINBOND I/O

W83977TF Data Sheet Revision History

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6					
7					
8					
9					
10					

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WINBOND I/O

GENERAL DESCRIPTION

The W83977TF is an evolving product from Winbond's most popular I/O chip W83877F --- which integrates the disk drive adapter, serial port (UART), IrDA 1.0 SIR, parallel port, configurable plug-and-play registers for the whole chip --- plus additional powerful features: **ACPI**, 8042 keyboard controller with PS/2 mouse support, 23 general purpose I/O ports, full 16-bit address decoding, OnNow keyboard wake-up, OnNow mouse wake-up.

The disk drive adapter functions of W83977TF include a floppy disk drive controller compatible with the industry standard 82077/ 765, data separator, write pre-compensation circuit, decode logic, data rate selection, clock generator, drive interface control logic, and interrupt and DMA logic. The wide range of functions integrated into the W83977TF greatly reduces the number of components required for interfacing with floppy disk drives. The W83977TF supports four 360K, 720K, 1.2M, 1.44M, or 2.88M disk drives and data transfer rates of 250 Kb/s, 300 Kb/s, 500 Kb/s,1 Mb/s, and 2 Mb/s.

The W83977TF provides two high-speed serial communication ports (UARTs), one of which supports serial Infrared communication. Each UART includes a 16-byte send/receive FIFO, a programmable baud rate generator, complete modem control capability, and a processor interrupt system. Both UARTs provide legacy speed with baud rate up to 115.2k bps and also advanced speed with baud rates of **230k**, **460k**, or **921k bps** which support higher speed modems.

The W83977TF supports one PC-compatible printer port (SPP), Bi-directional Printer port (BPP) and also Enhanced Parallel Port (EPP) and Extended Capabilities Port (ECP). Through the printer port interface pins, also available are: Extension FDD Mode and Extension 2FDD Mode allowing one or two external floppy disk drives to be connected.

The configuration registers support mode selection, function enable/disable, and power down function selection. Furthermore, the configurable PnP features are compatible with the plug-and-play feature demand of Windows 95^{TM}, which makes system resource allocation more efficient than ever.

W83977TF provides functions that comply with **ACPI** (*Advanced Configuration and Power Interface*), which includes support of legacy and ACPI power management through $\overline{\text{SMI}}$ or $\overline{\text{SCI}}$ function pins. W83977TF also has auto power management to reduce power consumption.

The keyboard controller is based on 8042 compatible instruction set with a 2K Byte programmable ROM and a 256-Byte RAM bank. Keyboard BIOS firmware is available with optional AMIKEY^{TM}-2, Phoenix MultiKey/42^{TM}, or customer code.

The W83977TF provides a set of flexible I/O control functions to the system designer through a set of General Purpose I/O ports. These GPIO ports may serve as simple I/O or may be individually configured to provide a predefined alternate function.

W83977TF is made to fully comply with **Microsoft PC97 Hardware Design Guide**. IRQs, DMAs, and I/O space resource are flexible to adjust to meet ISA PnP requirement. Moreover W83977TF is made to meet the specification of PC97's requirement in the power management: **ACPI** and **DPM** (Device Power Management).

Another benifit is that W83977TF has the same pin assignment as W83977AF, W83977F, W83977ATF. This makes the design very flexible.

FEATURES

General

- Plug & Play 1.0A compatible
- Support 13 IRQs, 4 DMA channels, full 16-bit address decoding
- Capable of ISA Bus IRQ Sharing
- Compliant with **Microsoft PC97** Hardware Design Guide
- Support **DPM** (Device Power Management), **ACPI**
- Report ACPI status interrupt by $\overline{\text{SCI}}$ signal issued from any of the 13 IQRs pins or GPIO xx
- Programmable configuration settings
- Single 24/48 Mhz clock input

FDC

- Compatible with IBM PC AT disk drive systems
- Variable write pre-compensation with track selectable capability
- Support vertical recording format
- DMA enable logic
- 16-byte data FIFOs
- Support floppy disk drives and tape drives
- Detects all overrun and underrun conditions
- Built-in address mark detection circuit to simplify the read electronics
- FDD anti-virus functions with software write protect and FDD write enable signal (write data signal was forced to be inactive)
- Support up to four 3.5-inch or 5.25-inch floppy disk drives
- Completely compatible with industry standard 82077
- 360K/720K/1.2M/1.44M/2.88M format; 250K, 300K, 500K, 1M, 2M bps data transfer rate
- Support **3-mode FDD, and its Win95 driver**

UART

- Two high-speed 16550 compatible UARTs with 16-byte send/receive FIFOs
- MIDI compatible
- Fully programmable serial-interface characteristics:
  --- 5, 6, 7 or 8-bit characters
  --- Even, odd or no parity bit generation/detection
  --- 1, 1.5 or 2 stop bits generation
- Internal diagnostic capabilities:
  --- Loop-back controls for communications link fault isolation
  --- Break, parity, overrun, framing error simulation
- Programmable baud generator allows division of 1.8461 Mhz and 24 Mhz by 1 to (2^{16}-1)

Maximum baud rate up to 921k bps **for 14.769 Mhz and 1.5M bps for 24 Mhz**

Infrared

- Support IrDA version 1.0 SIR protocol with maximum baud rate up to 115.2K bps
- Support SHARP ASK-IR protocol with maximum baud rate up to 57,600 bps
- **Support S/W driver for Windows95^{TM} and Windows98^{TM} (Memphis^{TM})**

Parallel Port

- Compatible with IBM parallel port
- Support PS/2 compatible bi-directional parallel port
- Support Enhanced Parallel Port (EPP) – Compatible with IEEE 1284 specification
- Support Extended Capabilities Port (ECP) – Compatible with IEEE 1284 specification
- Extension FDD mode supports disk drive B; and Extension 2FDD mode supports disk drives A and B through parallel port
- Enhanced printer port back-drive current protection

Keyboard Controller

- 8042 based with optional F/W from AMIKKEY^{TM}-2, Phoenix MultiKey/42^{TM} or customer code with 2K bytes of programmable ROM, and 256 bytes of RAM
- Asynchronous Access to Two Data Registers and One status Register
- Software compatibility with the 8042 and PC87911 microcontrollers
- Support PS/2 mouse
- Support port 92
- Support both interrupt and polling modes
- **Fast Gate A20 and Hardware Keyboard Reset**
- 8 Bit Timer/ Counter
- Support binary and BCD arithmetic
- 6MHz, 8 MHz, 12 MHz, or 16 MHz operating frequency

General Purpose I/O Ports

- 23 programmable general purpose I/O ports; 3 dedicate, 20 optional
- General purpose I/O ports can serve as simple I/O ports, interrupt steering inputs, watching dog timer output, power LED output, infrared I/O pins, general purpose address decoder, KBC control I/O pins

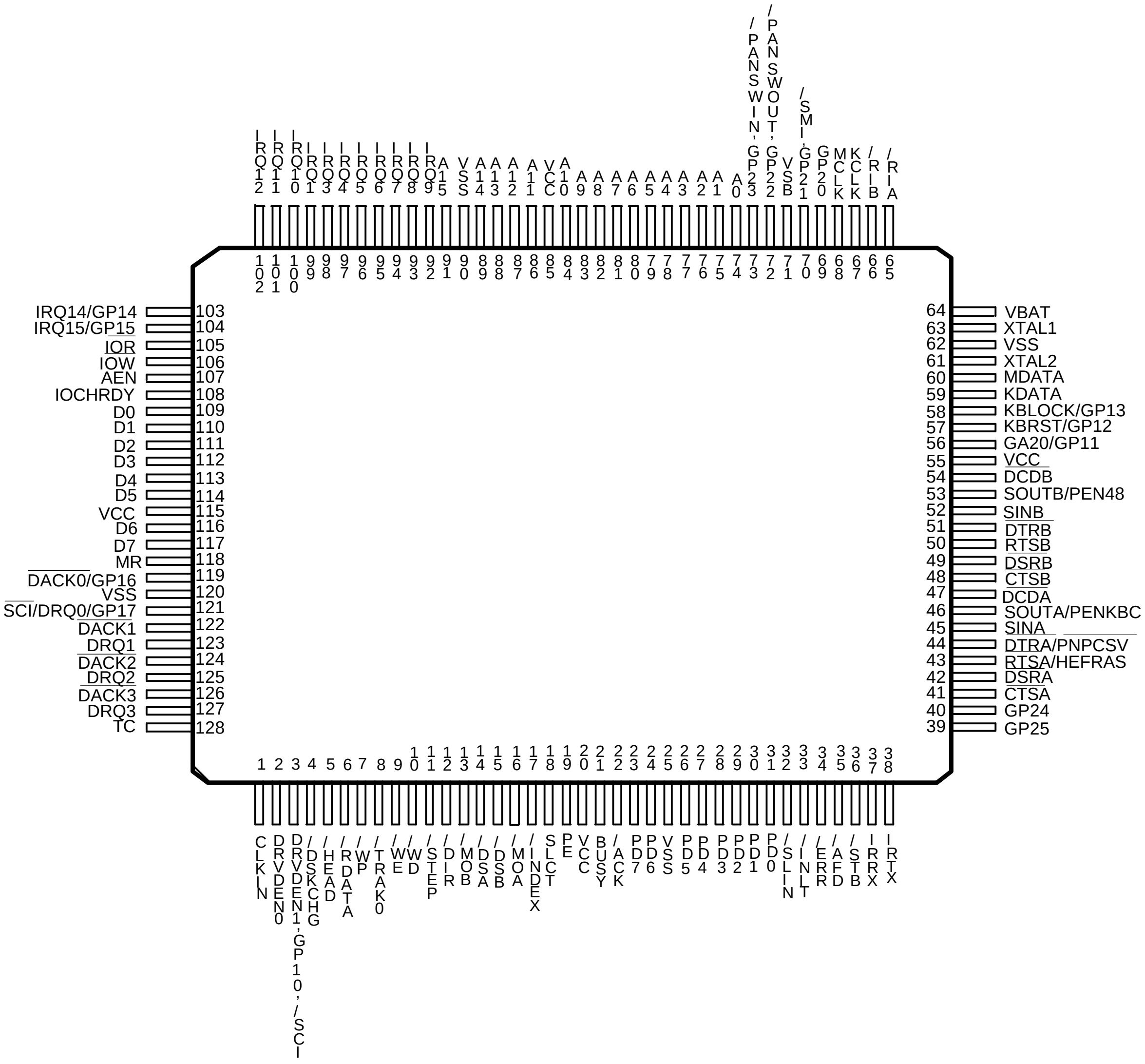
OnNow Funtions

- Keyboard wake-up by programmable keys
- Mouse wake-up by programmable buttons

Package

- 128-pin PQFP

PIN CONFIGURATION


102 IRQ12
101 IRQ11
100 IRQ10
99 IRQ1
98 IRQ3
97 IRQ4
96 IRQ5
95 IRQ6
94 IRQ7
93 IRQ8
92 IRQ9
91 A15
90 VSS
89 A14
88 A13
87 A12
86 A11
85 VCC
84 A10
83 A9
82 A8
81 A7
80 A6
79 A5
78 A4
77 A3
76 A2
75 A1
74 A0
73 /PANSWIN,GP23
72 /PANSWOUT,GP22
71 VSB
70 /SMI,GP21
69 GP20
68 MCLK
67 KCLK
66 /RIB
65 /RIA
103 IRQ14/GP14
104 IRQ15/GP15
105 IOR
106 IOW
107 AEN
108 IOCHRDY
109 D0
110 D1
111 D2
112 D3
113 D4
114 D5
115 VCC
116 D6
117 D7
118 MR
119 DACK0/GP16
120 VSS
121 SCI/DRQ0/GP17
122 DACK1
123 DRQ1
124 DACK2
125 DRQ2
126 DACK3
127 DRQ3
128 TC
64 VBAT
63 XTAL1
62 VSS
61 XTAL2
60 MDATA
59 KDATA
58 KBLOCK/GP13
57 KBRST/GP12
56 GA20/GP11
55 VCC
54 DCDB
53 SOUTB/PEN48
52 SINB
51 DTRB
50 RTSB
49 DSRB
48 CTSB
47 DCDA
46 SOUTA/PENKBC
45 SINA
44 DTRA/PNPCSV
43 RTSA/HEFRAS
42 DSRA
41 CTSA
40 GP24
39 GP25
1 CLKIN
2 DRVDEN0
3 DRVDEN1,GP10,/SCI
4 /DSKCHG
5 /HEAD
6 /RDATA
7 /WP
8 /TRAK0
9 /WE
10 /WD
11 /STEP
12 /DIR
13 /MOB
14 /DSA
15 /DSB
16 /MOA
17 /INDEX
18 SLCT
19 PE
20 VCC
21 BUSY
22 /ACK
23 PD7
24 PD6
25 VSS
26 PD5
27 PD4
28 PD3
29 PD2
30 PD1
31 PD0
32 /SLIN
33 /INIT
34 /ERR
35 /AFD
36 /STB
37 IRRX
38 IRTX

1. PIN DESCRIPTION

Note: Please refer to Section 11.2 DC CHARACTERISTICS for details.

I/O$_{6t}$ - TTL level bi-directional pin with 6 mA source-sink capability

I/O$_{8t}$ - TTL level bi-directional pin with 8 mA source-sink capability

I/O$_{8}$ - CMOS level bi-directional pin with 8 mA source-sink capability

I/O$_{12t}$ - TTL level bi-directional pin with 12 mA source-sink capability

I/O$_{12}$ - CMOS level bi-directional pin with 12 mA source-sink capability

I/O$_{16u}$ - CMOS level bi-directional pin with 16 mA source-sink capability with internal pull-up resistor

I/OD$_{16u}$ - CMOS level bi-directional pin open drain output with 16 mA sink capability with internal pull-up resistor

I/O$_{24t}$ - TTL level bi-directional pin with 24 mA source-sink capability

OUT$_{8t}$ - TTL level output pin with 8 mA source-sink capability

OUT$_{12t}$ - TTL level output pin with 12 mA source-sink capability

OD$_{12}$ - Open-drain output pin with 12 mA sink capability

OD$_{24}$ - Open-drain output pin with 24 mA sink capability

IN$_{t}$ - TTL level input pin

IN$_{c}$ - CMOS level input pin

IN$_{cu}$ - CMOS level input pin with internal pull-up resitor

IN$_{cs}$ - CMOS level Schmitt-triggered input pin

IN$_{ts}$ - TTL level Schmitt-triggered input pin

IN$_{tsu}$ - TTL level Schmitt-triggered input pin with internal pull-up resistor

1.1 Host Interface

SYMBOL	PIN	I/O	FUNCTION
A0–A10	74-84	IN$_{t}$	System address bus bits 0-10
A11-A14	86-89	IN$_{t}$	System address bus bits 11-14
A15	91	IN$_{t}$	System address bus bit 15
D0–D5	109-114	I/O$_{12t}$	System data bus bits 0-5
D6–D7	116-117	I/O$_{12t}$	System data bus bits 6-7
$\overline{\text{IOR}}$	105	IN$_{ts}$	CPU I/O read signal
$\overline{\text{IOW}}$	106	IN$_{ts}$	CPU I/O write signal
AEN	107	IN$_{ts}$	System address bus enable
IOCHRDY	108	OD$_{24}$	In EPP Mode, this pin is the IO Channel Ready output to extend the host read/write cycle.
MR	118	IN$_{ts}$	Master Reset; Active high; MR is low during normal operations.

1.1 Host Interface, continued

SYMBOL	PIN	I/O	FUNCTION
$\overline{\text{DACK0}}$	119	IN$_{tsu}$	DMA Channel 0 Acknowledge signal. (CR2C bit 5_4 = 00, default)
GP16 (WDTO)		I/O$_{12t}$	General purpose I/O port 1bit 6. (CR2C bit 5_4 = 01) Alternate function from GP16: Watch dog timer output
P15		I/O$_{12t}$	KBC P15 I/O port. (CR2C bit 5_4 = 10)
DRQ0	121	OUT$_{12t}$	DMA Channel 0 request signal. (CR2C bit 7_6 = 00, default)
GP17 (PLEDO)		I/O$_{12t}$	General purpose I/O port 1bit 7. (CR2C bit 7_6 = 01) Alternate Function from GP17: Power LED output.
P14		I/O$_{12t}$	KBC P14 I/O port (CR2C bit 7_6 = 10)
$\overline{\text{SCI}}$		OUT$_{12t}$	System Control Interrupt (CR2C bit 7_6 = 11)
$\overline{\text{DACK1}}$	122	IN$_{ts}$	DMA Channel 1 Acknowledge signal
DRQ1	123	OUT$_{12t}$	DMA Channel 1 request signal
$\overline{\text{DACK2}}$	124	IN$_{ts}$	DMA Channel 2 Acknowledge signal
DRQ2	125	OUT$_{12t}$	DMA Channel 2 request signal
$\overline{\text{DACK3}}$	126	IN$_{ts}$	DMA Channel 3 Acknowledge signal
DRQ3	127	OUT$_{12t}$	DMA Channel 3 request signal
TC	128	IN$_{ts}$	Terminal Count. When active, this pin indicates termination of a DMA transfer.
IRQ1	99	OUT$_{12t}$	Interrupt request 1
IRQ3	98	OUT$_{12t}$	Interrupt request 3
IRQ4	97	OUT$_{12t}$	Interrupt request 4
IRQ5	96	OUT$_{12t}$	Interrupt request 5
IRQ6	95	OUT$_{12t}$	Interrupt request 6
IRQ7	94	OUT$_{12t}$	Interrupt request 7
IRQ8	93	OUT$_{12t}$	Interrupt request 8
IRQ9	92	OUT$_{12t}$	Interrupt request 9
IRQ10	100	OUT$_{12t}$	Interrupt request 10
IRQ11	101	OUT$_{12t}$	Interrupt request 11
IRQ12	102	OUT$_{12t}$	Interrupt request 12

1.1 Host Interface, continued

SYMBOL	PIN	I/O	FUNCTION
IRQ14	103	OUT$_{12t}$	Interrupt request 14. (CR2C bit 1_0 = 00, default)
GP14		I/O$_{12t}$	General purpose I/O port 1 bit 4. (CR2C bit 1_0 = 01)
($\overline{\text{GPACS}}$)			Alternate Function 1 from GP14: General purpose address decode output.
(P17)			Alternate Function 2 from GP14: KBC P17 I/O port.
PLEDO		OUT$_{12t}$	Power LED output. (CR2C bit 1_0 = 10)
IRQ15	104	OUT$_{12t}$	Interrupt request 15.(CR2C bit 3_2 = 00, default)
GP15		I/O$_{12t}$	General purpose I/O port 1 bit 5. (CR2C bit 3_2 = 01)
($\overline{\text{GPAWE}}$)			Alternate Function 1 from GP15: General purpose address write enable output.
(P12)			Alternate Function 2 from GP15: KBC P12 I/O port.
WDT		OUT$_{12t}$	Watch-Dog timer output. (CR2C bit 3_2 = 10)
CLKIN	1	IN$_t$	24 or 48 MHz clock input, selectable through bit 5 of CR24.

1.2 General Purpose I/O Port

SYMBOL	PIN	I/O	FUNCTION
GP20	69	I/O$_{12t}$	General purpose I/O port 2 bit 0.
(KBRST)			Alternate Function from GP20: Keyboard reset (KBC P20)
$\overline{\text{SMI}}$	70	OUT$_{12t}$	For the power management, the $\overline{\text{SMI}}$ is active low by the power management events, that generate and $\overline{\text{SCI}}$ in ACPI mode. (CR2B bit 4_3 = 00, default)
GP21		I/O$_{12t}$	General purpose I/O port 2 bit 1. (CR2B bit 4_3 = 01)
(P13)			Alternate Function from GP21: KBC P13 I/O port.
P16		I/O$_{12t}$	KBC P16 I/O port. (CR2B bit 4_3 = 10)
$\overline{\text{PANSWOUT}}$	72	OUT$_{12t}$	Panel Switch output. (CR2B bit 5 = 0, default)
GP22		I/O$_{12t}$	General purpose I/O port 2 bit 2. (CR2B bit 5 = 1)
(P14)			Alternate Function from GP22: KBC P14 I/O port.
$\overline{\text{PANSWIN}}$	73	IN$_{12t}$	Panel Switch input. (CR2B bit 7_6 = 00, default)
GP23		I/O$_{12t}$	General purpose I/O port 2 bit 3. (CR2B bit 7_6 = 01)
(P15)			Alternate Function from GP23: KBC P15 I/O port
GP24	40	I/O$_{12t}$	General purpose I/O port 2 bit 4 (CR2A bit 5_4 = 01)
(P16)			Alternate Function from GP24: KBC P16 I/O port
P13		I/O$_{12t}$	KBC P13 I/O port. (CR2A bit 5_4 = 10)
GP25	39	I/O$_{12}$	General purpose I/O port 2 bit 5.
(GA20)			Alternate Function from GP25: GATE A20 (KBC P21)

1.3 Serial Port Interface

SYMBOL	PIN	I/O	FUNCTION
$\overline{\text{CTSA}}$ $\overline{\text{CTSB}}$	41 48	IN_t	Clear To Send is the modem control input. The function of these pins can be tested by reading Bit 4 of the handshake status register.
$\overline{\text{DSRA}}$ $\overline{\text{DSRB}}$	42 49	IN_t	Data Set Ready. An active low signal indicates the modem or data set is ready to establish a communication link and transfer data to the UART.
$\overline{\text{RTSA}}$ HEFRAS	43	I/O_{8t}	UART A Request To Send. An active low signal informs the modem or data set that the controller is ready to send data. During power-on reset, this pin is pulled down internally and is defined as HEFRAS, which provides the power-on value for CR26 bit 6 (HEFRAS). A 4.7 kΩ is recommended if intends to pull up. (select 370H as configuration I/O port′s address)
$\overline{\text{RTSB}}$	50	I/O_{8t}	UART B Request To Send. An active low signal informs the modem or data set that the controller is ready to send data.
$\overline{\text{DTRA}}$ $\overline{\text{PNPCSV}}$	44	I/O_{8t}	UART A Data Terminal Ready. An active low signal informs the modem or data set that the controller is ready to communicate. During power-on reset, this pin is pulled down internally and is defined as $\overline{\text{PNPCSV}}$, which provides the power-on value for CR24 bit 0 ($\overline{\text{PNPCSV}}$). A 4.7 kΩ is recommended if intends to pull up. (clear the default value of FDC, UARTs, and PRT)
$\overline{\text{DTRB}}$	51	I/O_{8t}	UART B Data Terminal Ready. An active low signal informs the modem or data set that controller is ready to communicate.
SINA SINB	45, 52	IN_t	Serial Input. Used to receive serial data through the communication link.
SOUTA PENKBC	46	I/O_{8t}	UART A Serial Output. Used to transmit serial data out to the communication link. During power-on reset, this pin is pulled down internally and is defined as PENKBC, which provides the power-on value for CR24 bit 2 (ENKBC). A 4.7 kΩ resistor is recommended if intends to pull up. (enable KBC)
SOUTB PEN48	53	I/O_{8t}	UART B Serial Output. During power-on reset, this pin is pulled down internally and is defined as PEN48, which provides the power-on value for CR24 bit 6 (EN48). A 4.7 kΩ resistor is recommended if intends to pull up.
$\overline{\text{DCDA}}$ $\overline{\text{DCDB}}$	47 54	IN_t	Data Carrier Detect. An active low signal indicates the modem or data set has detected a data carrier.

1.3 Serial Port Interface, continued

SYMBOL	PIN	I/O	FUNCTION
$\overline{\text{RIA}}$ $\overline{\text{RIB}}$	65 66	IN_t	Ring Indicator. An active low signal indicates that a ring signal is being received from the modem or data set.

1.4 Infrared Interface

SYMBOL	PIN	I/O	FUNCTION
IRRX	37	IN_{cs}	Infrared Receiver input.
IRTX	38	OUT_{12t}	Infrared Transmitter Output.

1.5 Multi-Mode Parallel Port

The following pins have alternate functions, which are controlled by CR28 and L3-CRF0.

SYMBOL	PIN	I/O	FUNCTION
SLCT	18	IN_t OD_{12} OD_{12}	PRINTER MODE: SLCT An active high input on this pin indicates that the printer is selected. This pin is pulled high internally. Refer to description of the parallel port for definition of this pin in ECP and EPP mode. EXTENSION FDD MODE: $\overline{\text{WE2}}$ This pin is for Extension FDD B; its function is the same as the $\overline{\text{WE}}$ pin of FDC. EXTENSION 2FDD MODE: $\overline{\text{WE2}}$ This pin is for Extension FDD A and B; it function is the same as the $\overline{\text{WE}}$ pin of FDC.
PE	19	IN_t OD_{12} OD_{12}	PRINTER MODE: PE An active high input on this pin indicates that the printer has detected the end of the paper. This pin is pulled high internally. Refer to description of the parallel port for definition of this pin in ECP and EPP mode. EXTENSION FDD MODE: $\overline{\text{WD2}}$ This pin is for Extension FDD B; its function is the same as the $\overline{\text{WD}}$ pin of FDC. EXTENSION 2FDD MODE: $\overline{\text{WD2}}$ This pin is for Extension FDD A and B; its function is the same as the $\overline{\text{WD}}$ pin of FDC.

1.5 Multi-Mode Parallel Port, continued

SYMBOL	PIN	I/O	FUNCTION
BUSY	21	IN_t	PRINTER MODE: BUSY An active high input indicates that the printer is not ready to receive data. This pin is pulled high internally. Refer to description of the parallel port for definition of this pin in ECP and EPP mode.
		OD_{12}	EXTENSION FDD MODE: $\overline{\text{MOB2}}$ This pin is for Extension FDD B; the function of this pin is the same as the $\overline{\text{MOB}}$ pin of FDC.
		OD_{12}	EXTENSION 2FDD MODE: $\overline{\text{MOB2}}$ This pin is for Extension FDD A and B; the function of this pin is the same as the $\overline{\text{MOB}}$ pin of FDC.
$\overline{\text{ACK}}$	22	IN_t	PRINTER MODE: $\overline{\text{ACK}}$ An active low input on this pin indicates that the printer has received data and is ready to accept more data. This pin is pulled high internally. Refer to description of the parallel port for definition of this pin in ECP and EPP mode.
		OD_{12}	EXTENSION FDD MODE: $\overline{\text{DSB2}}$ This pin is for the Extension FDD B; its functions is the same as the $\overline{\text{DSB}}$ pin of FDC.
		OD_{12}	EXTENSION 2FDD MODE: $\overline{\text{DSB2}}$ This pin is for Extension FDD A and B; it functions is the same as the $\overline{\text{DSB}}$ pin of FDC.
$\overline{\text{ERR}}$	34	IN_t	PRINTER MODE: $\overline{\text{ERR}}$ An active low input on this pin indicates that the printer has encountered an error condition. This pin is pulled high internally. Refer to description of the parallel port for definition of this pin in ECP and EPP mode.
		OD_{12}	EXTENSION FDD MODE: $\overline{\text{HEAD2}}$ This pin is for Extension FDD B; its function is the same as the $\overline{\text{HEAD}}$pin of FDC.
		OD_{12}	EXTENSION 2FDD MODE: $\overline{\text{HEAD2}}$ This pin is for Extension FDD A and B; its function is the same as the $\overline{\text{HEAD}}$ pin of FDC.

1.5 Multi-Mode Parallel Port, continued

SYMBOL	PIN	I/O	FUNCTION
$\overline{\text{SLIN}}$	32	OD_{12}	PRINTER MODE: $\overline{\text{SLIN}}$ Output line for detection of printer selection. This pin is pulled high internally. Refer to description of the parallel port for definition of this pin in ECP and EPP mode.
		OD_{12}	EXTENSION FDD MODE: $\overline{\text{STEP2}}$ This pin is for Extension FDD B; its function is the same as the $\overline{\text{STEP}}$ pin of FDC.
		OD_{12}	EXTENSION 2FDD MODE: $\overline{\text{STEP2}}$ This pin is for Extension FDD A and B; its function is the same as the $\overline{\text{STEP}}$ pin of FDC.
$\overline{\text{INIT}}$	33	OD_{12}	PRINTER MODE: $\overline{\text{INIT}}$ Output line for the printer initialization. This pin is pulled high internally. Refer to description of the parallel port for definition of this pin in ECP and EPP mode.
		OD_{12}	EXTENSION FDD MODE: $\overline{\text{DIR2}}$ This pin is for Extension FDD B; its function is the same as the $\overline{\text{DIR}}$ pin of FDC.
		OD_{12}	EXTENSION 2FDD MODE: $\overline{\text{DIR2}}$ This pin is for Extension FDD A and B; its function is the same as the $\overline{\text{DIR}}$ pin of FDC.
$\overline{\text{AFD}}$	35	OD_{12}	PRINTER MODE: $\overline{\text{AFD}}$ An active low output from this pin causes the printer to auto feed a line after a line is printed. This pin is pulled high internally. Refer to description of the parallel port for definition of this pin in ECP and EPP mode.
		OD_{12}	EXTENSION FDD MODE: DRVDEN0 This pin is for Extension FDD B; its function is the same as the DRVDEN0 pin of FDC.
		OD_{12}	EXTENSION 2FDD MODE: DRVDEN0 This pin is for Extension FDD A and B; its function is the same as the DRVDEN0 pin of FDC.

1.5 Multi-Mode Parallel Port, continued

SYMBOL	**PIN**	**I/O**	**FUNCTION**
$\overline{\text{STB}}$	36	OD_{12}	PRINTER MODE: $\overline{\text{STB}}$ An active low output is used to latch the parallel data into the printer. This pin is pulled high internally. Refer to description of the parallel port for definition of this pin in ECP and EPP mode.
		-	EXTENSION FDD MODE: This pin is a tri-state output.
		-	EXTENSION 2FDD MODE: This pin is a tri-state output.
PD0	31	I/O_{24t}	PRINTER MODE: PD0 Parallel port data bus bit 0. Refer to description of the parallel port for definition of this pin in ECP and EPP mode.
		IN_t	EXTENSION FDD MODE: $\overline{\text{INDEX2}}$ This pin is for Extension FDD B; the function of this pin is the same as the $\overline{\text{INDEX}}$ pin of FDC. It is pulled high internally.
		IN_t	EXTENSION 2FDD MODE: $\overline{\text{INDEX2}}$ This pin is for Extension FDD A and B; the function of this pin is the same as the $\overline{\text{INDEX}}$ pin of FDC. It is pulled high internally.
PD1	30	I/O_{24t}	PRINTER MODE: PD1 Parallel port data bus bit 1. Refer to description of the parallel port for definition of this pin in ECP and EPP mode.
		IN_t	EXTENSION FDD MODE: $\overline{\text{TRAK02}}$ This pin is for Extension FDD B; the function of this pin is the same as the $\overline{\text{TRAK0}}$ pin of FDC. It is pulled high internally.
		IN_t	EXTENSION. 2FDD MODE: $\overline{\text{TRAK02}}$ This pin is for Extension FDD A and B; the function of this pin is the same as the $\overline{\text{TRAK0}}$ pin of FDC. It is pulled high internally.
PD2	29	I/O_{24t}	PRINTER MODE: PD2 Parallel port data bus bit 2. Refer to description of the parallel port for definition of this pin in ECP and EPP mode.
		IN_t	EXTENSION FDD MODE: $\overline{\text{WP2}}$ This pin is for Extension FDD B; the function of this pin is the same as the $\overline{\text{WP}}$ pin of FDC. It is pulled high internally.
		IN_t	EXTENSION. 2FDD MODE: $\overline{\text{WP2}}$ This pin is for Extension FDD A and B; the function of this pin is the same as the $\overline{\text{WP}}$ pin of FDC. It is pulled high internally.

1.5 Multi-Mode Parallel Port, continued

SYMBOL	PIN	I/O	FUNCTION
PD3	28	I/O_{24t} IN_t IN_t	PRINTER MODE: PD3 Parallel port data bus bit 3. Refer to description of the parallel port for definition of this pin in ECP and EPP mode. EXTENSION FDD MODE: $\overline{\text{RDATA2}}$ This pin is for Extension FDD B; the function of this pin is the same as the $\overline{\text{RDATA}}$ pin of FDC. It is pulled high internally. EXTENSION 2FDD MODE: $\overline{\text{RDATA2}}$ This pin is for Extension FDD A and B; this function of this pin is the same as the $\overline{\text{RDATA}}$ pin of FDC. It is pulled high internally.
PD4	27	I/O_{24t} IN_t IN_t	PRINTER MODE: PD4 Parallel port data bus bit 4. Refer to description of the parallel port for definition of this pin in ECP and EPP mode. EXTENSION FDD MODE: $\overline{\text{DSKCHG2}}$ This pin is for Extension FDD B; the function of this pin is the same as the $\overline{\text{DSKCHG}}$ pin of FDC. It is pulled high internally. EXTENSION 2FDD MODE: $\overline{\text{DSKCHG2}}$ This pin is for Extension FDD A and B; this function of this pin is the same as the $\overline{\text{DSKCHG}}$ pin of FDC. It is pulled high internally.
PD5	26	I/O_{24t} - -	PRINTER MODE: PD5 Parallel port data bus bit 5. Refer to description of the parallel port for definition of this pin in ECP and EPP mode. EXTENSION FDD MODE: This pin is a tri-state output. EXTENSION 2FDD MODE: This pin is a tri-state output.
PD6	24	I/O_{24t} - OD_{24}	PRINTER MODE: PD6 Parallel port data bus bit 6. Refer to description of the parallel port for definition of this pin in ECP and EPP mode. EXTENSION FDD MODE: This pin is a tri-state output. EXTENSION. 2FDD MODE: $\overline{\text{MOA2}}$ This pin is for Extension FDD A; its function is the same as the $\overline{\text{MOA}}$ pin of FDC.

1.5 Multi-Mode Parallel Port, continued

SYMBOL	PIN	I/O	FUNCTION
PD7	23	I/O$_{24t}$	PRINTER MODE: PD7 Parallel port data bus bit 7. Refer to description of the parallel port for definition of this pin in ECP and EPP mode.
		-	EXTENSION FDD MODE: This pin is a tri-state output.
		OD$_{24}$	EXTENSION 2FDD MODE: $\overline{\text{DSA}}$2 This pin is for Extension FDD A; its function is the same as the $\overline{\text{DSA}}$ pin of FDC.

1.6 FDC Interface

SYMBOL	PIN	I/O	FUNCTION
DRVDEN0	2	OD$_{24}$	Drive Density Select bit 0.
DRVDEN1	3	OD$_{24}$	Drive Density Select bit 1. (CR2A bit 1_0 = 00, default)
GP10		IO$_{24t}$	General purpose I/O port 1 bit 0. (CR2A bit 1_0 = 01)
(IRQIN1)			Alternate Function from GP10: Interrupt channel input.
P12		IO$_{24t}$	KBC P12 I/O port. (CR2A bit 1_0 = 10)
$\overline{\text{SCI}}$		OUT$_{12t}$	System Control Interrupt (CR2A bit 1_0 = 11)
$\overline{\text{HEAD}}$	5	OD$_{24}$	Head select. This open drain output determines which disk drive head is active. Logic 1 = side 0 Logic 0 = side 1
$\overline{\text{WE}}$	9	OD$_{24}$	Write enable. An open drain output.
$\overline{\text{WD}}$	10	OD$_{24}$	Write data. This logic low open drain writes pre-compensation serial data to the selected FDD. An open drain output.
$\overline{\text{STEP}}$	11	OD$_{24}$	Step output pulses. This active low open drain output produces a pulse to move the head to another track.
$\overline{\text{DIR}}$	12	OD$_{24}$	Direction of the head step motor. An open drain output. Logic 1 = outward motion Logic 0 = inward motion
$\overline{\text{MOB}}$	13	OD$_{24}$	Motor B On. When set to 0, this pin enables disk drive 1. This is an open drain output.
$\overline{\text{DSA}}$	14	OD$_{24}$	Drive Select A. When set to 0, this pin enables disk drive A. This is an open drain output.
$\overline{\text{DSB}}$	15	OD$_{24}$	Drive Select B. When set to 0, this pin enables disk drive B. This is an open drain output.

1.6 FDC Interface, continued

SYMBOL	PIN	I/O	FUNCTION
$\overline{\text{MOA}}$	16	OD$_{24}$	Motor A On. When set to 0, this pin enables disk drive 0. This is an open drain output.
$\overline{\text{DSKCHG}}$	4	IN$_{cs}$	Diskette change. This signal is active low at power on and whenever the diskette is removed. This input pin is pulled up internally by a 1 KΩ resistor. The resistor can be disabled by bit 7 of L0-CRF0 (FIPURDWN).
$\overline{\text{RDATA}}$	6	IN$_{cs}$	The read data input signal from the FDD. This input pin is pulled up internally by a 1 KΩ resistor. The resistor can be disabled by bit 7 of L0-CRF0 (FIPURDWN).
$\overline{\text{WP}}$	7	IN$_{cs}$	Write protected. This active low Schmitt input from the disk drive indicates that the diskette is write-protected. This input pin is pulled up internally by a 1 KΩ resistor. The resistor can be disabled by bit 7 of L0-CRF0 (FIPURDWN).
$\overline{\text{TRAK0}}$	8	IN$_{cs}$	Track 0. This Schmitt-triggered input from the disk drive is active low when the head is positioned over the outermost track. This input pin is pulled up internally by a 1 KΩ resistor. The resistor can be disabled by bit 7 of L0-CRF0 (FIPURDWN).
$\overline{\text{INDEX}}$	17	IN$_{cs}$	This Schmitt-triggered input from the disk drive is active low when the head is positioned over the beginning of a track marked by an index hole. This input pin is pulled up internally by a 1 KΩ resistor. The resistor can be disabled by bit 7 of L0-CRF0 (FIPURDWN).

1.7 KBC Interface

SYMBOL	PIN	I/O	FUNCTION
KDATA	59	I/OD$_{16u}$	Keyboard Data
MDATA	60	I/OD$_{16u}$	PS2 Mouse Data
KCLK	67	I/OD$_{16u}$	Keyboard Clock
MCLK	68	I/OD$_{16u}$	PS2 Mouse Clock
GA20 GP11 (IRQIN2)	56	I/O$_{12t}$ I/O$_{12t}$	KBC GATE A20 (P21) Output. (CR2A bit 6 = 0, default) General purpose I/O port 1 bit 1. (CR2A bit 6 = 1) Alternate Function from GP11: Interrupt channel input.
KBRST GP12 (WDTO)	57	I/O$_{12t}$ I/O$_{12t}$	W83C45 Keyboard Reset (P20) Output. (CR2A bit 7 = 0, default) General purpose I/O port 1 bit 2. (CR2A bit 7 = 1) Alternate Function 1 from GP12 : Watchdog timer output.

1.7 KBC Interface, continued

SYMBOL	PIN	I/O	FUNCTION
KBLOCK GP13	58	IN_{ts} I/O_{16t}	W83C45 KINH (P17) Input. (CR2B bit 0 = 0, default) General purpose I/O port 1 bit 3. (CR2B bit 0 = 1)

1.8 POWER PINS

SYMBOL	PIN	FUNCTION
VCC	20, 55, 85, 115	+5V power supply for the digital circuitry
VSB	71	+5V stand-by power supply for the digital circuitry
GND	25, 62, 90, 120	Ground

1.9 ACPI Interface

SYMBOL	PIN	I/O	FUNCTION
VBAT	64	NA	battery voltage input
XTAL1	63	IN_C	32.768Khz Clock Input
XTAL2	61	O_{8t}	32.768Khz Clock Output

2. FDC FUNCTIONAL DESCRIPTION

2.1 W83977TF FDC

The floppy disk controller of the W83977TF integrates all of the logic required for floppy disk control. The FDC implements a PC/AT or PS/2 solution. All programmable options default to compatible values. The FIFO provides better system performance in multi-master systems. The digital data separator supports up to 2 M bits/sec data rate.

The FDC includes the following blocks: AT interface, Precompensation, Data Rate Selection, Digital Data Separator, FIFO, and FDC Core.

2.1.1 AT interface

The interface consists of the standard asynchronous signals: $\overline{RD}$, $\overline{WR}$, A0-A3, IRQ, DMA control, and a data bus. The address lines select between the configuration registers, the FIFO and control/status registers. This interface can be switched between PC/AT, Model 30, or PS/2 normal modes. The PS/2 register sets are a superset of the registers found in a PC/AT.

2.1.2 FIFO (Data)

The FIFO is 16 bytes in size and has programmable threshold values. All command parameter information and disk data transfers go through the FIFO. Data transfers are governed by the RQM and DIO bits in the Main Status Register.

The FIFO defaults to disabled mode after any form of reset. This maintains PC/AT hardware compatibility. The default values can be changed through the CONFIGURE command. The advantage of the FIFO is that it allows the system a larger DMA latency without causing disk errors. The following tables give several examples of the delays with a FIFO. The data are based upon the following formula:

THRESHOLD # × (1/DATA/RATE) *8 - 1.5 µS = DELAY

FIFO THRESHOLD	MAXIMUM DELAY TO SERVICING AT 500K BPS
	Data Rate
1 Byte	1 × 16 µS - 1.5 µS = 14.5 µS
2 Byte	2 × 16 µS - 1.5 µS = 30.5 µS
8 Byte	8 × 16 µS - 1.5 µS = 6.5 µS
15 Byte	15 × 16 µS - 1.5 µS = 238.5 µS

FIFO THRESHOLD	MAXIMUM DELAY TO SERVICING AT 1M BPS
	Data Rate
1 Byte	1 × 8 µS - 1.5 µS = 6.5 µS
2 Byte	2 × 8 µS - 1.5 µS = 14.5 µS
8 Byte	8 × 8 µS - 1.5 µS = 62.5 µS
15 Byte	15 × 8 µS - 1.5 µS = 118.5 µS

At the start of a command the FIFO is always disabled and command parameters must be sent based upon the RQM and DIO bit settings in the main status register. When the FDC enters the command execution phase, it clears the FIFO of any data to ensure that invalid data are not transferred.

An overrun and underrun will terminate the current command and the data transfer. Disk writes will complete the current sector by generating a 00 pattern and valid CRC. Reads require the host to remove the remaining data so that the result phase may be entered.

DMA transfers are enabled with the SPECIFY command and are initiated by the FDC by activating the DRQ pin during a data transfer command. The FIFO is enabled directly by asserting $\overline{\text{DACK}}$ and addresses need not be valid.

Note that if the DMA controller is programmed to function in verify mode a pseudo read is performed by the FDC based only on $\overline{\text{DACK}}$. This mode is only available when the FDC has been configured into byte mode (FIFO disabled) and is programmed to do a read. With the FIFO enabled the above operation is performed by using the new VERIFY command. No DMA operation is needed.

2.1.3 Data Separator

The function of the data separator is to lock onto the incoming serial read data. When a lock is achieved the serial front end logic of the chip is provided with a clock which is synchronized to the read data. The synchronized clock, called the Data Window, is used to internally sample the serial data portion of the bit cell, and the alternate state samples the clock portion. Serial to parallel conversion logic separates the read data into clock and data bytes.

The Digital Data Separator (DDS) has three parts: control logic, error adjustment, and speed tracking. The DDS circuit cycles once every 12 clock cycles ideally. Any data pulse input will be synchronized and then adjusted by immediate error adjustment. The control logic will generate RDD and RWD for every pulse input. During any cycle where no data pulse is present, the DDS cycles are based on speed. A digital integrator is used to keep track of the speed changes in the input data stream.

2.1.4 Write Precompensation

The write precompensation logic is used to minimize bit shifts in the RDDATA stream from the disk drive. Shifting of bits is a known phenomenon in magnetic media and is dependent on the disk media and the floppy drive.

The FDC monitors the bit stream that is being sent to the drive. The data patterns that require precompensation are well known. Depending upon the pattern, the bit is shifted either early or late relative to the surrounding bits.

2.1.5 Perpendicular Recording Mode

The FDC is also capable of interfacing directly to perpendicular recording floppy drives. Perpendicular recording differs from the traditional longitudinal method in that the magnetic bits are oriented vertically. This scheme packs more data bits into the same area.

FDCs with perpendicular recording drives can read standard 3.5" floppy disks and can read and write perpendicular media. Some manufacturers offer drives that can read and write standard and perpendicular media in a perpendicular media drive.

A single command puts the FDC into perpendicular mode. All other commands operate as they normally do. The perpendicular mode requires a 1 Mbps data rate for the FDC. At this data rate the FIFO eases the host interface bottleneck due to the speed of data transfer to or from the disk.

2.1.6 FDC Core

The W83977TF FDC is capable of performing twenty commands. Each command is initiated by a multi-byte transfer from the microprocessor. The result can also be a multi-byte transfer back to the microprocessor. Each command consists of three phases: command, execution, and result.

Command

The microprocessor issues all required information to the controller to perform a specific operation.

Execution

The controller performs the specified operation.

Result

After the operation is completed, status information and other housekeeping information is provided to the microprocessor.

2.1.7 FDC Commands

Command Symbol Descriptions:

C:	Cylinder number 0 - 256
D:	Data Pattern
DIR:	Step Direction DIR = 0, step out DIR = 1, step in
DS0:	Disk Drive Select 0
DS1:	Disk Drive Select 1
DTL:	Data Length
EC:	Enable Count
EOT:	End of Track
EFIFO:	Enable FIFO
EIS:	Enable Implied Seek
EOT:	End of track
FIFOTHR:	FIFO Threshold
GAP:	Gap length selection
GPL:	Gap Length
H:	Head number
HDS:	Head number select
HLT:	Head Load Time
HUT:	Head Unload Time
LOCK:	Lock EFIFO, FIFOTHR, PTRTRK bits prevent affected by software reset
MFM:	MFM or FM Mode
MT:	Multitrack
N:	The number of data bytes written in a sector
NCN:	New Cylinder Number
ND:	Non-DMA Mode
OW:	Overwritten
PCN:	Present Cylinder Number
POLL:	Polling Disable
PRETRK:	Precompensation Start Track Number

R:	Record
RCN:	Relative Cylinder Number
R/W:	Read/Write
SC:	Sector/per cylinder
SK:	Skip deleted data address mark
SRT:	Step Rate Time
ST0:	Status Register 0
ST1:	Status Register 1
ST2:	Status Register 2
ST3:	Status Register 3
WG:	Write gate alters timing of WE

(1) Read Data

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	MT	MFM	SK	0	0	1	1	0	Command codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W	--------------------- C -----------------------								Sector ID information prior to command execution
	W	--------------------- H -----------------------								
	W	--------------------- R -----------------------								
	W	--------------------- N -----------------------								
	W	-------------------- EOT ----------------------								
	W	-------------------- GPL ----------------------								
	W	-------------------- DTL ----------------------								
Execution										Data transfer between the FDD and system
Result	R	-------------------- ST0 ----------------------								Status information after command execution
	R	-------------------- ST1 ----------------------								
	R	-------------------- ST2 ----------------------								
	R	--------------------- C -----------------------								Sector ID information after command execution
	R	--------------------- H -----------------------								
	R	--------------------- R -----------------------								
	R	--------------------- N -----------------------								

(2) Read Deleted Data

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	MT	MFM	SK	0	1	1	0	0	Command codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W	---------------------- C -----------------------								Sector ID information prior to command execution
	W	---------------------- H -----------------------								
	W	---------------------- R -----------------------								
	W	---------------------- N -----------------------								
	W	-------------------- EOT ----------------------								
	W	-------------------- GPL ----------------------								
	W	-------------------- DTL ----------------------								
Execution										Data transfer between the FDD and system
Result	R	-------------------- ST0 ----------------------								Status information after command execution
	R	-------------------- ST1 ----------------------								
	R	-------------------- ST2 ----------------------								
	R	---------------------- C -----------------------								Sector ID information after command execution
	R	---------------------- H -----------------------								
	R	---------------------- R -----------------------								
	R	---------------------- N -----------------------								

(3) Read A Track

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	0	MFM	0	0	0	0	1	0	Command codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W	---------------------- C -----------------------								Sector ID information prior to command execution
	W	---------------------- H -----------------------								
	W	---------------------- R -----------------------								
	W	---------------------- N -----------------------								
	W	-------------------- EOT ----------------------								
	W	-------------------- GPL ----------------------								
	W	-------------------- DTL ----------------------								
Execution										Data transfer between the FDD and system; FDD reads contents of all cylinders from index hole to EOT
Result	R	-------------------- ST0 ----------------------								Status information after command execution
	R	-------------------- ST1 ----------------------								
	R	-------------------- ST2 ----------------------								
	R	---------------------- C -----------------------								Sector ID information after command execution
	R	---------------------- H -----------------------								
	R	---------------------- R -----------------------								
	R	---------------------- N -----------------------								

(4) Read ID

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	0	MFM	0	0	1	0	1	0	Command codes
	W	0	0	0	0	0	HDS	DS1	DS0	
Execution										The first correct ID information on the cylinder is stored in Data Register
Result	R	-------------------- ST0 ----------------------								Status information after command execution
	R	-------------------- ST1 ----------------------								
	R	-------------------- ST2 ----------------------								
	R	--------------------- C -----------------------								Disk status after the command has been completed
	R	--------------------- H -----------------------								
	R	--------------------- R -----------------------								
	R	--------------------- N -----------------------								

(5) Verify

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	MT	MFM	SK	1	0	1	1	0	Command codes
	W	EC	0	0	0	0	HDS	DS1	DS0	
	W	--------------------- C -----------------------								Sector ID information prior to command execution
	W	--------------------- H -----------------------								
	W	--------------------- R -----------------------								
	W	--------------------- N -----------------------								
	W	-------------------- EOT ----------------------								
	W	-------------------- GPL ----------------------								
		-------------------- DTL/SC -------------------								
Execution										No data transfer takes place
Result	R	-------------------- ST0 ----------------------								Status information after command execution
	R	-------------------- ST1 ----------------------								
	R	-------------------- ST2 ----------------------								
	R	--------------------- C -----------------------								Sector ID information after command execution
	R	--------------------- H -----------------------								
	R	--------------------- R -----------------------								
	R	--------------------- N -----------------------								

(6) Version

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	0	0	0	1	0	0	0	0	Command code
Result	R	1	0	0	1	0	0	0	0	Enhanced controller

(7) Write Data

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	MT	MFM	0	0	0	1	0	1	Command codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W	---------------------- C ------------------------								Sector ID information prior to Command execution
	W	---------------------- H ------------------------								
	W	---------------------- R ------------------------								
	W	---------------------- N ------------------------								
	W	-------------------- EOT ----------------------								
	W	-------------------- GPL ----------------------								
	W	-------------------- DTL ----------------------								
Execution										Data transfer between the FDD and system
Result	R	-------------------- ST0 ----------------------								Status information after Command execution
	R	-------------------- ST1 ----------------------								
	R	-------------------- ST2 ----------------------								
	R	---------------------- C ------------------------								Sector ID information after Command execution
	R	---------------------- H ------------------------								
	R	---------------------- R ------------------------								
	R	---------------------- N ------------------------								

(8) Write Deleted Data

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	MT	MFM	0	0	1	0	0	1	Command codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W	--------------------- C -----------------------								Sector ID information prior to command execution
	W	--------------------- H -----------------------								
	W	--------------------- R -----------------------								
	W	--------------------- N -----------------------								
	W	-------------------- EOT ----------------------								
	W	-------------------- GPL ----------------------								
	W	-------------------- DTL ----------------------								
Execution										Data transfer between the FDD and system
Result	R	-------------------- ST0 ----------------------								Status information after command execution
	R	-------------------- ST1 ----------------------								
	R	-------------------- ST2 ----------------------								
	R	--------------------- C -----------------------								Sector ID information after command execution
	R	--------------------- H -----------------------								
	R	--------------------- R -----------------------								
	R	--------------------- N -----------------------								

(9) Format A Track

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	0	MFM	0	0	1	1	0	1	Command codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W	--------------------- N -----------------------								Bytes/Sector
	W	-------------------- SC ----------------------								Sectors/Cylinder
	W	-------------------- GPL --------------------								Gap 3
	W	--------------------- D -----------------------								Filler Byte
Execution for Each Sector Repeat:	W	--------------------- C -----------------------								Input Sector Parameters
	W	--------------------- H -----------------------								
	W	--------------------- R -----------------------								
	W	--------------------- N -----------------------								
Result	R	------------------- ST0 ----------------------								Status information after command execution
	R	------------------- ST1 ----------------------								
	R	------------------- ST2 ----------------------								
	R	---------------- Undefined -------------------								
	R	---------------- Undefined -------------------								
	R	---------------- Undefined -------------------								
	R	---------------- Undefined -------------------								

(10) Recalibrate

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	0	0	0	0	0	1	1	1	Command codes
	W	0	0	0	0	0	0	DS1	DS0	
Execution										Head retracted to Track 0 Interrupt

(11) Sense Interrupt Status

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	0	0	0	0	1	0	0	0	Command code
Result	R	---------------- ST0 ------------------------								Status information at the end of each seek operation
	R	---------------- PCN ------------------------								

(12) Specify

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	0	0	0	0	0	0	1	1	Command codes
	W	| ---------SRT ----------- |				--------- HUT ---------- |				
	W	|------------ HLT ---------------------------------|							ND	

(13) Seek

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	0	0	0	0	1	1	1	1	Command codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W	-------------------- NCN -----------------------								
Execution	R									Head positioned over proper cylinder on diskette

(14) Configure

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	0	0	0	1	0	0	1	1	Configure information
	W	0	0	0	0	0	0	0	0	
	W	0	EIS	EFIFO	POLL	| ------ FIFOTHR ----|				
	W	| --------------------PRETRK ----------------------- |								
Execution										Internal registers written

(15) Relative Seek

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	1	DIR	0	0	1	1	1	1	Command codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W	| -------------------- RCN ---------------------------- |								

(16) Dumpreg

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	0	0	0	0	1	1	1	0	Registers placed in FIFO
Result	R	---------------------- PCN-Drive 0--------------------								
	R	---------------------- PCN-Drive 1 -------------------								
	R	---------------------- PCN-Drive 2--------------------								
	R	---------------------- PCN-Drive 3 -------------------								
	R	--------SRT ------------------ | --------- HUT --------								
	R	----------- HLT -----------------------------------| ND								
	R	----------------------- SC/EOT ----------------------								
	R	LOCK	0	D3	D2	D1	D0	GAP	WG	
	R	0	EIS	EFIFO	POLL	| ------ FIFOTHR --------				
	R	-----------------------PRETRK -------------------------								

(17) Perpendicular Mode

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	0	0	0	1	0	0	1	0	Command Code
	W	OW	0	D3	D2	D1	D0	GAP	WG	

(18) Lock

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	LOCK	0	0	1	0	1	0	0	Command Code
Result	R	0	0	0	LOCK	0	0	0	0	

(19) Sense Drive Status

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	0	0	0	0	0	1	0	0	Command Code
	W	0	0	0	0	0	HDS	DS1	DS0	
Result	R	---------------- ST3 ------------------------								Status information about disk drive

(20) Invalid

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	------------- Invalid Codes -----------------								Invalid codes (no operation- FDC goes to standby state)
Result	R	-------------------- ST0 ----------------------								ST0 = 80H

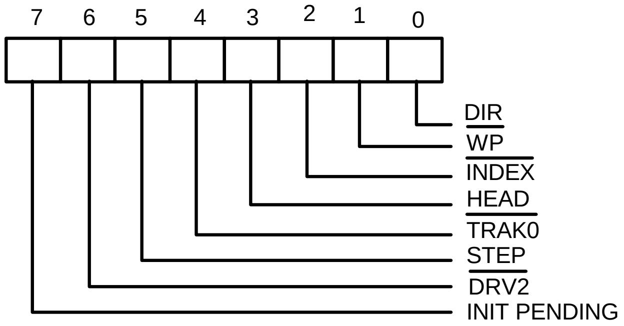
2.2 Register Descriptions

There are several status, data, and control registers in W83977TF. These registers are defined below:

ADDRESS OFFSET	REGISTER	
	READ	WRITE
base address + 0	SA REGISTER	
base address + 1	SB REGISTER	
base address + 2		DO REGISTER
base address + 3	TD REGISTER	TD REGISTER
base address + 4	MS REGISTER	DR REGISTER
base address + 5	DT (FIFO) REGISTER	DT (FIFO) REGISTER
base address + 7	DI REGISTER	CC REGISTER

2.2.1 Status Register A (SA Register) (Read base address + 0)

This register is used to monitor several disk interface pins in PS/2 and Model 30 modes. In PS/2 mode, the bit definitions for this register are as follows:



INIT PENDING (Bit 7):

This bit indicates the value of the floppy disk interrupt output.

$\overline{\text{DRV2}}$ (Bit 6):

0 A second drive has been installed

1 A second drive has not been installed

STEP (Bit 5):

This bit indicates the complement of $\overline{\text{STEP}}$ output.

$\overline{\text{TRAK0}}$ (Bit 4):

This bit indicates the value of $\overline{\text{TRAK0}}$ input.

HEAD (Bit 3):

This bit indicates the complement of $\overline{\text{HEAD}}$ output.

0 side 0

1 side 1

$\overline{\text{INDEX}}$ (Bit 2):

This bit indicates the value of $\overline{\text{INDEX}}$ output.

$\overline{\text{WP}}$ (Bit 1):

0disk is write-protected

1disk is not write-protected

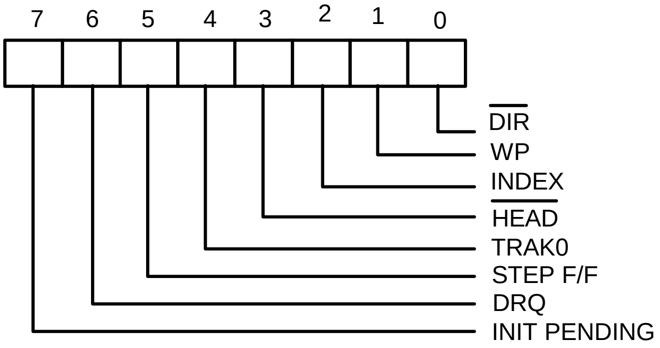
DIR (Bit 0)

This bit indicates the direction of head movement.

0 outward direction

1 inward direction

In PS/2 Model 30 mode, the bit definitions for this register are as follows:



INIT PENDING (Bit 7):

This bit indicates the value of the floppy disk interrupt output.

DRQ (Bit 6):

This bit indicates the value of DRQ output pin.

STEP F/F (Bit 5):

This bit indicates the complement of latched $\overline{\text{STEP}}$ output.

TRAK0 (Bit 4):

This bit indicates the complement of $\overline{\text{TRAK0}}$ input.

$\overline{\text{HEAD}}$ (Bit 3):

This bit indicates the value of $\overline{\text{HEAD}}$ output.

0 side 1

1 side 0

INDEX (Bit 2):

This bit indicates the complement of $\overline{\text{INDEX}}$ output.

WP (Bit 1):

0 disk is not write-protected

1 disk is write-protected

$\overline{\text{DIR}}$ (Bit 0)

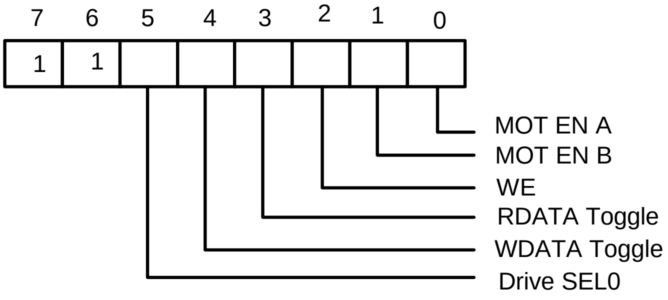
This bit indicates the direction of head movement.

0 inward direction

1 outward direction

2.2.2 Status Register B (SB Register) (Read base address + 1)

This register is used to monitor several disk interface pins in PS/2 and Model 30 modes. In PS/2 mode, the bit definitions for this register are as follows:



Drive SEL0 (Bit 5):

This bit indicates the status of DO REGISTER bit 0 (drive select bit 0).

WDATA Toggle (Bit 4):

This bit changes state at every rising edge of the $\overline{\text{WD}}$ output pin.

RDATA Toggle (Bit 3):

This bit changes state at every rising edge of the $\overline{\text{RDATA}}$ output pin.

WE (Bit 2):

This bit indicates the complement of the $\overline{\text{WE}}$ output pin.

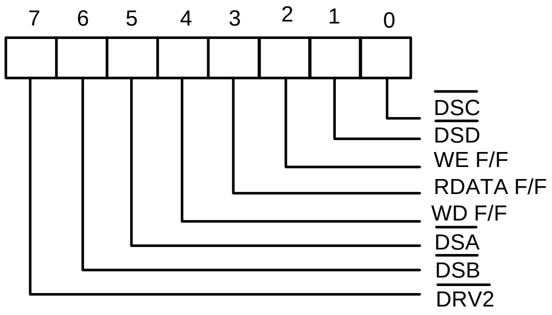
MOT EN B (Bit 1)

This bit indicates the complement of the $\overline{\text{MOB}}$ output pin.

MOT EN A (Bit 0)

This bit indicates the complement of the $\overline{\text{MOA}}$ output pin.

In PS/2 Model 30 mode, the bit definitions for this register are as follows:



$\overline{\text{DRV2}}$ (Bit 7):

0	A second drive has been installed
1	A second drive has not been installed

$\overline{\text{DSB}}$ (Bit 6):

This bit indicates the status of $\overline{\text{DSB}}$ output pin.

$\overline{\text{DSA}}$ (Bit 5):

This bit indicates the status of $\overline{\text{DSA}}$ output pin.

WD F/F(Bit 4):

This bit indicates the complement of the latched $\overline{\text{WD}}$ output pin at every rising edge of the $\overline{\text{WD}}$ output pin.

RDATA F/F(Bit 3):

This bit indicates the complement of the latched $\overline{\text{RDATA}}$ output pin .

WE F/F (Bit 2):

This bit indicates the complement of latched $\overline{\text{WE}}$ output pin.

$\overline{\text{DSD}}$ (Bit 1):

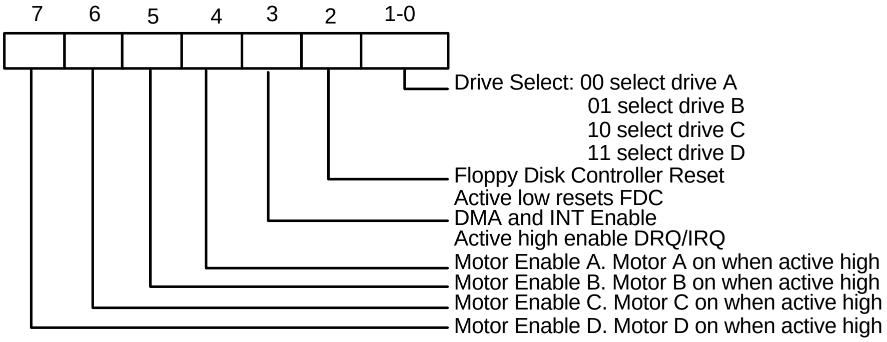
0	Drive D has been selected
1	Drive D has not been selected

$\overline{\text{DSC}}$ (Bit 0):

0	Drive C has been selected
1	Drive C has not been selected

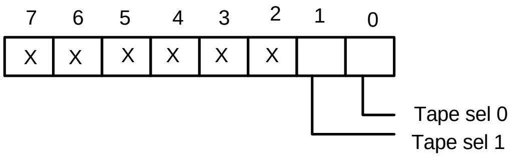
2.2.3 Digital Output Register (DO Register) (Write base address + 2)

The Digital Output Register is a write-only register controlling drive motors, drive selection, DRQ/IRQ enable, and FDC resetting. All the bits in this register are cleared by the MR pin. The bit definitions are as follows:

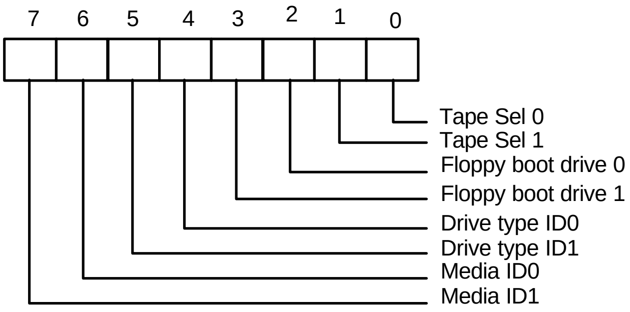

7
6
5
4
3
2
1-0
Drive Select: 00 select drive A
01 select drive B
10 select drive C
11 select drive D
Floppy Disk Controller Reset
Active low resets FDC
DMA and INT Enable
Active high enable DRQ/IRQ
Motor Enable A. Motor A on when active high
Motor Enable B. Motor B on when active high
Motor Enable C. Motor C on when active high
Motor Enable D. Motor D on when active high

2.2.4 Tape Drive Register (TD Register) (Read base address + 3)

This register is used to assign a particular drive number to the tape drive support mode of the data separator. This register also holds the media ID, drive type, and floppy boot drive information of the floppy disk drive. In normal floppy mode, this register includes only bit 0 and 1. The bit definitions are as follows:


7
6
5
4
3
2
1
0
X
X
X
X
X
X
Tape sel 0
Tape sel 1

If three mode FDD function is enabled (EN3MODE = 1 in Logical Device 0 CRF0 bit:0), the bit definitions are as follows:


7
6
5
4
3
2
1
0
Tape Sel 0
Tape Sel 1
Floppy boot drive 0
Floppy boot drive 1
Drive type ID0
Drive type ID1
Media ID0
Media ID1

Media ID1 Media ID0 (Bit 7, 6):

These two bits are read only. These two bits reflect the value of Logical Device 0 CRF1 bit 4,5.

Drive type ID1 Drive type ID0 (Bit 5, 4):

These two bits reflect two of the bits of Logical Device 0 CRF2. Which two bits are reflected depends on the last drive selected in the DO REGISTER.

Floppy Boot drive 1, 0 (Bit 3, 2):

These two bits reflect the value of Logical Device 0 CRF1 bit 7,6.

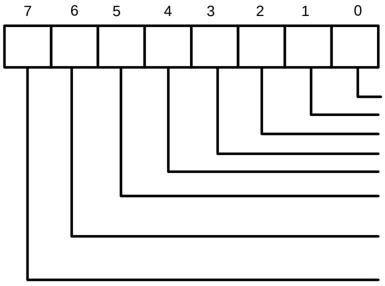
Tape Sel 1, Tape Sel 0 (Bit 1, 0):

These two bits assign a logical drive number to the tape drive. Drive 0 is not available as a tape drive and is reserved as the floppy disk boot drive.

TAPE SEL 1	TAPE SEL 0	DRIVE SELECTED
0	0	None
0	1	1
1	0	2
1	1	3

2.2.5 Main Status Register (MS Register) (Read base address + 4)

The Main Status Register is used to control the flow of data between the microprocessor and the controller. The bit definitions for this register are as follows:



FDD 0 Busy, (D0B = 1), FDD number 0 is in the SEEK mode.

FDD 1 Busy, (D1B = 1), FDD number 1 is in the SEEK mode.

FDD 2 Busy, (D2B = 1), FDD number 2 is in the SEEK mode.

FDD 3 Busy, (D3B = 1), FDD number 3 is in the SEEK mode.

FDC Busy, (CB). A read or write command is in the process when CB = HIGH.

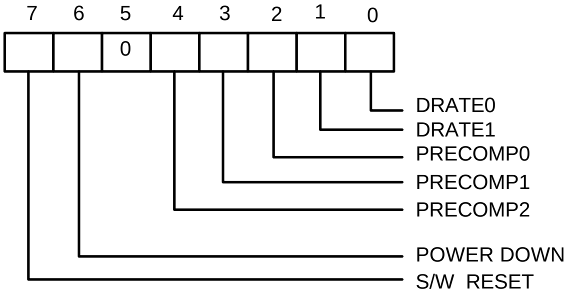
Non-DMA mode, the FDC is in the non-DMA mode, this bit is set only during the execution phase in non-DMA mode.
Transition to LOW state indicates execution phase has ended.

DATA INPUT/OUTPUT, (DIO). If DIO= HIGH then transfer is from Data Register to the processor.
If DIO = LOW then transfer is from processor to Data Register.

Request for Master (RQM). A high on this bit indicates Data Register is ready to send or receive data to or from the processor.

2.2.6 Data Rate Register (DR Register) (Write base address + 4)

The Data Rate Register is used to set the transfer rate and write precompensation. The data rate of the FDC is programmed by the CC REGISTER for PC-AT and PS/2 Model 30 and PS/2 mode, and not by the DR REGISTER. The real data rate is determined by the most recent write to either of the DR REGISTER or CC REGISTER.


7
6
5
4
3
2
1
0
0
DRATE0
DRATE1
PRECOMP0
PRECOMP1
PRECOMP2
POWER DOWN
S/W RESET

S/W RESET (Bit 7):

This bit is the software reset bit.

POWER-DOWN (Bit 6):

0 FDC in normal mode
1 FDC in power-down mode

PRECOMP2 PRECOMP1 PRECOMP0 (Bit 4, 3, 2):

These three bits select the value of write precompensation. The following tables show the precompensation values for the combination of these bits.

PRECOMP	**PRECOMPENSATION DELAY**	
2 1 0	250K - 1 Mbps	2 Mbps Tape drive
0 0 0	Default Delays	Default Delays
0 0 1	41.67 nS	20.8 nS
0 1 0	83.34 nS	41.17 nS
0 1 1	125.00 nS	62.5nS
1 0 0	166.67 nS	83.3 nS
1 0 1	208.33 nS	104.2 nS
1 1 0	250.00 nS	125.00 nS
1 1 1	0.00 nS (disabled)	0.00 nS (disabled)

DATA RATE	DEFAULT PRECOMPENSATION DELAYS
250 KB/S	125 nS
300 KB/S	125 nS
500 KB/S	125 nS
1 MB/S	41.67nS
2 MB/S	20.8 nS

DRATE1 DRATE0 (Bit 1, 0):
These two bits select the data rate of the FDC and reduced write current control.

00 500 KB/S (MFM), 250 KB/S (FM), $\overline{\text{RWC}}$ = 1

01 300 KB/S (MFM), 150 KB/S (FM), $\overline{\text{RWC}}$ = 0

10 250 KB/S (MFM), 125 KB/S (FM), $\overline{\text{RWC}}$ = 0

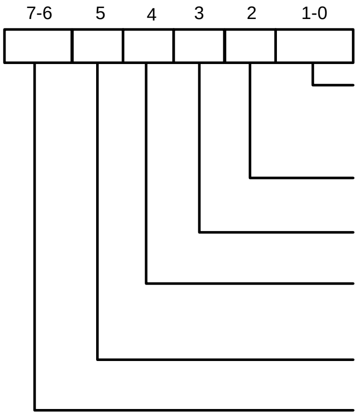
11 1 MB/S (MFM), Illegal (FM), $\overline{\text{RWC}}$ = 1

The 2 MB/S data rate for Tape drive is only supported by setting 01 to DRATE1 and DRATE0 bits, as well as setting 10 to DRT1 and DRT0 bits which are two of the Configure Register CRF4 or CRF5 bits in logic device 0. Please refer to the function description of CRF4 or CRF5 and data rate table for individual data rates setting.

2.2.7 FIFO Register (R/W base address + 5)

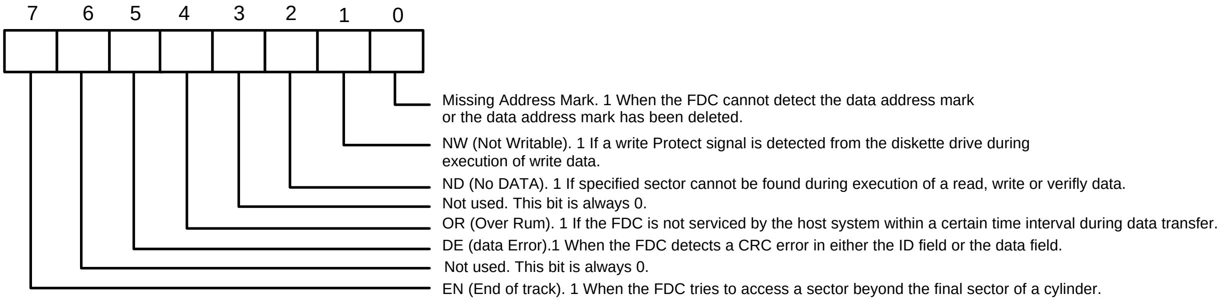
The Data Register consists of four status registers in a stack with only one register presented to the data bus at a time. This register stores data, commands, and parameters and provides diskette-drive status information. Data bytes are passed through the data register to program or obtain results after a command. In the W83977TF, this register defaults to FIFO disabled mode after reset. The FIFO can change its value and enable its operation through the CONFIGURE command.

Status Register 0 (ST0)



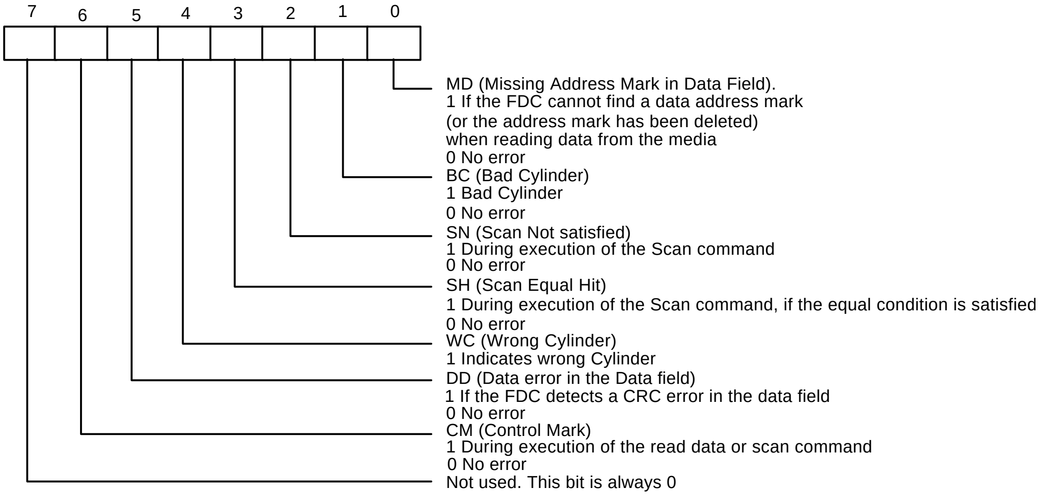
US1, US0 Drive Select:
00 Drive A selected
01 Drive B selected
10 Drive C selected
11 Drive D selected
HD Head address:
1 Head selected
0 Head selected
NR Not Ready:
1 Drive is not ready
0 Drive is ready
EC Equipment Check:
1 When a fault signal is received from the FDD or the track
0 signal fails to occur after 77 step pulses
0 No error
SE Seek end:
1 seek end
0 seek error
IC Interrupt Code:
00 Normal termination of command
01 Abnormal termination of command
10 Invalid command issue
11 Abnormal termination because the ready signal from FDD changed state during command executio

Status Register 1 (ST1)



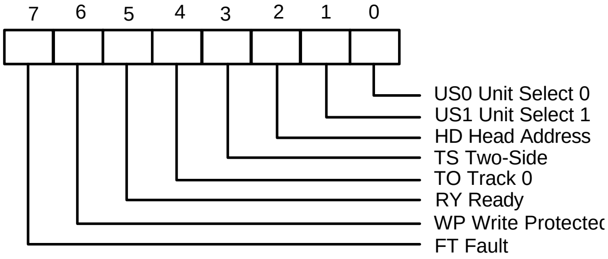
Missing Address Mark. 1 When the FDC cannot detect the data address mark
or the data address mark has been deleted.
NW (Not Writable). 1 If a write Protect signal is detected from the diskette drive during
execution of write data.
ND (No DATA). 1 If specified sector cannot be found during execution of a read, write or verifly data.
Not used. This bit is always 0.
OR (Over Rum). 1 If the FDC is not serviced by the host system within a certain time interval during data transfer.
DE (data Error).1 When the FDC detects a CRC error in either the ID field or the data field.
Not used. This bit is always 0.
EN (End of track). 1 When the FDC tries to access a sector beyond the final sector of a cylinder.

Status Register 2 (ST2)



MD (Missing Address Mark in Data Field).
1 If the FDC cannot find a data address mark
(or the address mark has been deleted)
when reading data from the media
0 No error
BC (Bad Cylinder)
1 Bad Cylinder
0 No error
SN (Scan Not satisfied)
1 During execution of the Scan command
0 No error
SH (Scan Equal Hit)
1 During execution of the Scan command, if the equal condition is satisfied
0 No error
WC (Wrong Cylinder)
1 Indicates wrong Cylinder
DD (Data error in the Data field)
1 If the FDC detects a CRC error in the data field
0 No error
CM (Control Mark)
1 During execution of the read data or scan command
0 No error
Not used. This bit is always 0

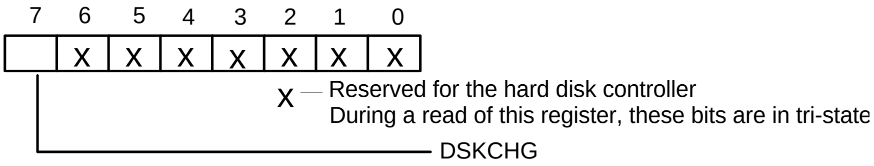
Status Register 3 (ST3)



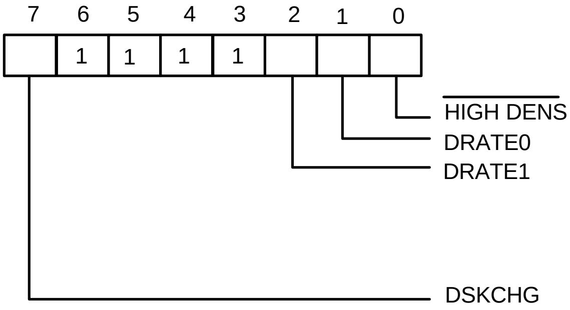
US0 Unit Select 0
US1 Unit Select 1
HD Head Address
TS Two-Side
TO Track 0
RY Ready
WP Write Protectec
FT Fault

2.2.8 Digital Input Register (DI Register) (Read base address + 7)

The Digital Input Register is an 8-bit read-only register used for diagnostic purposes. In a PC/XT or AT only Bit 7 is checked by the BIOS. When the register is read, Bit 7 shows the complement of $\overline{\text{DSKCHG}}$, while other bits of the data bus remain in tri-state. Bit definitions are as follows:


7
6
5
4
3
2
1
0
X
X
X
X
X
X
X
X — Reserved for the hard disk controller
During a read of this register, these bits are in tri-state
DSKCHG

In the PS/2 mode, the bit definitions are as follows:


7
6
5
4
3
2
1
0
1
1
1
1
$\overline{\text{HIGH DENS}}$
DRATE0
DRATE1
DSKCHG

DSKCHG (Bit 7):

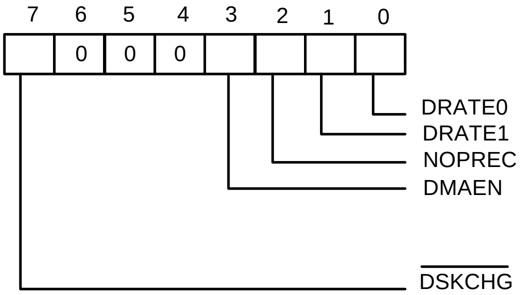
This bit indicates the complement of the $\overline{\text{DSKCHG}}$ input.

Bit 6-3: These bits are always a logic 1 during a read.

DRATE1 DRATE0 (Bit 2, 1):
These two bits select the data rate of the FDC. Refer to the DR register bits 1 and 0 for the settings corresponding to the individual data rates.

$\overline{\text{HIGH DENS}}$ (Bit 0):
0 500 KB/S or 1 MB/S data rate (high density FDD)
1 250 KB/S or 300 KB/S data rate

In the PS/2 Model 30 mode, the bit definitions are as follows:


7
6
5
4
3
2
1
0
0
0
0
DRATE0
DRATE1
NOPREC
DMAEN
$\overline{\text{DSKCHG}}$

DSKCHG (Bit 7):

This bit indicates the status of $\overline{\text{DSKCHG}}$ input.

Bit 6-4: These bits are always a logic 1 during a read.

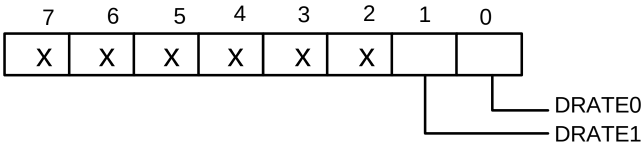
DMAEN (Bit 3):
This bit indicates the value of DO REGISTER bit 3.

NOPREC (Bit 2):
This bit indicates the value of CC REGISTER NOPREC bit.

DRATE1 DRATE0 (Bit 1, 0):
These two bits select the data rate of the FDC.

2.2.9 Configuration Control Register (CC Register) (Write base address + 7)

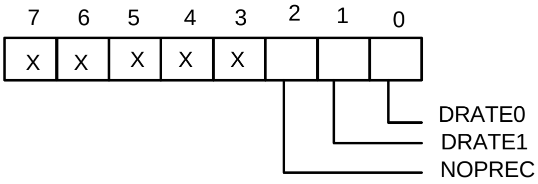
This register is used to control the data rate. In the PC/AT and PS/2 mode, the bit definitions are as follows:



X: Reserved

Bit 7-2: Reserved. These bits should be set to 0.

DRATE1 DRATE0 (Bit 1, 0):
These two bits select the data rate of the FDC.
In the PS/2 Model 30 mode, the bit definitions are as follows:



X: Reserved

Bit 7-3: Reserved. These bits should be set to 0.

NOPREC (Bit 2):
This bit indicates no precompensation. It has no function and can be set by software.

DRATE1 DRATE0 (Bit 1, 0):
These two bits select the data rate of the FDC.

3. UART PORT

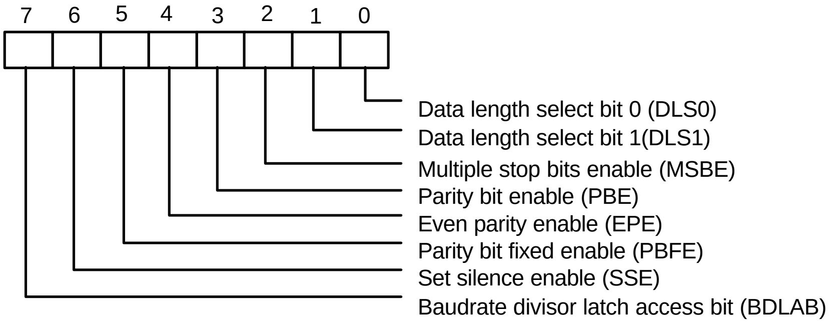
3.1 Universal Asynchronous Receiver/Transmitter (UART A, UART B)

The UARTs are used to convert parallel data into serial format on the transmit side and convert serial data to parallel format on the receiver side. The serial format, in order of transmission and reception, is a start bit, followed by five to eight data bits, a parity bit (if programmed) and one, one and half (five-bit format only) or two stop bits. The UARTs are capable of handling divisors of 1 to 65535 and producing a 16x clock for driving the internal transmitter logic. Provisions are also included to use this 16x clock to drive the receiver logic. The UARTs also support the MIDI data rate. Furthermore, the UARTs also include complete modem control capability and a processor interrupt system that may be software trailed to the computing time required to handle the communication link. The UARTs have a FIFO mode to reduce the number of interrupts presented to the CPU. In each UART, there are 16-byte FIFOs for both receive and transmit mode.

3.2 Register Address

3.2.1 UART Control Register (UCR) (Read/Write)

The UART Control Register controls and defines the protocol for asynchronous data communications, including data length, stop bit, parity, and baud rate selection.


7
6
5
4
3
2
1
0
Data length select bit 0 (DLS0)
Data length select bit 1(DLS1)
Multiple stop bits enable (MSBE)
Parity bit enable (PBE)
Even parity enable (EPE)
Parity bit fixed enable (PBFE)
Set silence enable (SSE)
Baudrate divisor latch access bit (BDLAB)

Bit 7: BDLAB. When this bit is set to a logical 1, designers can access the divisor (in 16-bit binary format) from the divisor latches of the baudrate generator during a read or write operation. When this bit is reset, the Receiver Buffer Register, the Transmitter Buffer Register, or the Interrupt Control Register can be accessed.

Bit 6: SSE. A logical 1 forces the Serial Output (SOUT) to a silent state (a logical 0). Only IRTX is affected by this bit; the transmitter is not affected.

Bit 5: PBFE. When PBE and PBFE of UCR are both set to a logical 1,

(1) if EPE is logical 1, the parity bit is fixed as logical 0 to transmit and check.

(2) if EPE is logical 0, the parity bit is fixed as logical 1 to transmit and check.

TABLE 3-1 UART Register Bit Map

			Bit Number							
Register Address Base			0	1	2	3	4	5	6	7
+ 0 BDLAB = 0	**Receiver Buffer Register (Read Only)**	**RBR**	RX Data Bit 0	RX Data Bit 1	RX Data Bit 2	RX Data Bit 3	RX Data Bit 4	RX Data Bit 5	RX Data Bit 6	RX Data Bit 7
+ 0 BDLAB = 0	**Transmitter Buffer Register (Write Only)**	**TBR**	TX Data Bit 0	TX Data Bit 1	TX Data Bit 2	TX Data Bit 3	TX Data Bit 4	TX Data Bit 5	TX Data Bit 6	TX Data Bit 7
+ 1 BDLAB = 0	**Interrupt Control Register**	**ICR**	RBR Data Ready Interrupt Enable (ERDRI)	TBR Empty Interrupt Enable (ETBREI)	USR Interrupt Enable (EUSRI)	HSR Interrupt Enable (EHSRI)	0	0	0	0
+ 2	**Interrupt Status Register (Read Only)**	**ISR**	"0" if Interrupt Pending	Interrupt Status Bit (0)	Interrupt Status Bit (1)	Interrupt Status Bit (2)**	0	0	FIFOs Enabled **	FIFOs Enabled **
+ 2	**UART FIFO Control Register (Write Only)**	**UFR**	FIFO Enable	RCVR FIFO Reset	XMIT FIFO Reset	DMA Mode Select	Reserved	Reversed	RX Interrupt Active Level (LSB)	RX Interrupt Active Level (MSB)
+ 3	**UART Control Register**	**UCR**	Data Length Select Bit 0 (DLS0)	Data Length Select Bit 1 (DLS1)	Multiple Stop Bits Enable (MSBE)	Parity Bit Enable (PBE)	Even Parity Enable (EPE)	Parity Bit Fixed Enable PBFE)	Set Silence Enable (SSE)	Baudrate Divisor Latch Access Bit (BDLAB)
+ 4	**Handshake Control Register**	**HCR**	Data Terminal Ready (DTR)	Request to Send (RTS)	Loopback RI Input	IRQ Enable	Internal Loopback Enable	0	0	0
+ 5	**UART Status Register**	**USR**	RBR Data Ready (RDR)	Overrun Error (OER)	Parity Bit Error (PBER)	No Stop Bit Error (NSER)	Silent Byte Detected (SBD)	TBR Empty (TBRE)	TSR Empty (TSRE)	RX FIFO Error Indication (RFEI) **
+ 6	**Handshake Status Register**	**HSR**	CTS Toggling (TCTS)	DSR Toggling (TDSR)	RI Falling Edge (FERI)	DCD Toggling (TDCD)	Clear to Send (CTS)	Data Set Ready (DSR)	Ring Indicator (RI)	Data Carrier Detect (DCD)
+ 7	**User Defined Register**	**UDR**	Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
+ 0 BDLAB = 1	**Baudrate Divisor Latch Low**	**BLL**	Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
+ 1 BDLAB = 1	**Baudrate Divisor Latch High**	**BHL**	Bit 8	Bit 9	Bit 10	Bit 11	Bit 12	Bit 13	Bit 14	Bit 15

*: Bit 0 is the least significant bit. The least significant bit is the first bit serially transmitted or received.

**: These bits are always 0 in 16450 Mode.

Bit 4: EPE. This bit describes the number of logic 1's in the data word bits and parity bit only when bit 3 is programmed. When this bit is set, an even number of logic 1's are sent or checked. When the bit is reset, an odd number of logic 1's are sent or checked.

Bit 3: PBE. When this bit is set, the position between the last data bit and the stop bit of the SOUT will be stuffed with the parity bit at the transmitter. For the receiver, the parity bit in the same position as the transmitter will be detected.

Bit 2: MSBE. This bit defines the number of stop bits in each serial character that is transmitted or received.

(1) If MSBE is set to a logical 0, one stop bit is sent and checked.

(2) If MSBE is set to a logical 1, and data length is 5 bits, one and a half stop bits are sent and checked.

(3) If MSBE is set to a logical 1, and data length is 6, 7, or 8 bits, two stop bits are sent and checked.

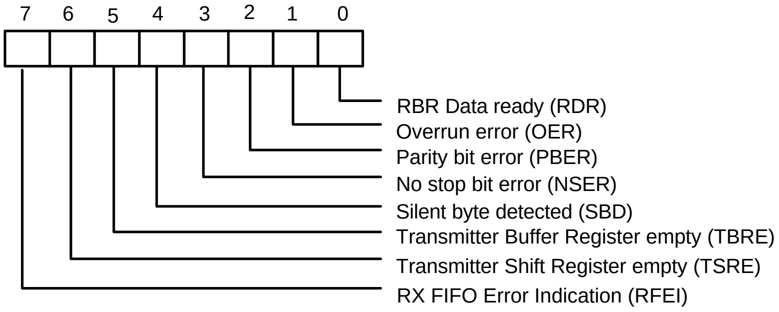
Bits 0 and 1: DLS0, DLS1. These two bits define the number of data bits that are sent or checked in each serial character.

TABLE 3-2 WORD LENGTH DEFINITION

DLS1	DLS0	DATA LENGTH
0	0	5 bits
0	1	6 bits
1	0	7 bits
1	1	8 bits

3.2.2 UART Status Register (USR) (Read/Write)

This 8-bit register provides information about the status of the data transfer during communication.


7
6
5
4
3
2
1
0
RBR Data ready (RDR)
Overrun error (OER)
Parity bit error (PBER)
No stop bit error (NSER)
Silent byte detected (SBD)
Transmitter Buffer Register empty (TBRE)
Transmitter Shift Register empty (TSRE)
RX FIFO Error Indication (RFEI)

Bit 7: RFEI. In 16450 mode, this bit is always set to a logic 0. In 16550 mode, this bit is set to a logic 1 when there is at least one parity bit error, no stop bit error or silent byte detected in the FIFO. In 16550 mode, this bit is cleared by reading from the USR if there are no remaining errors left in the FIFO.

Bit 6: TSRE. In 16450 mode, when TBR and TSR are both empty, this bit will be set to a logical 1. In 16550 mode, if the transmit FIFO and TSR are both empty, it will be set to a logical 1. Other thanthese two cases, this bit will be reset to a logical 0.

Bit 5: TBRE. In 16450 mode, when a data character is transferred from TBR to TSR, this bit will be set to a logical 1. If ETREI of ICR is a logical 1, an interrupt will be generated to notify the CPU to write the next data. In 16550 mode, this bit will be set to a logical 1 when the transmit FIFO is empty. It will be reset to a logical 0 when the CPU writes data into TBR or FIFO.

Bit 4: SBD. This bit is set to a logical 1 to indicate that received data are kept in silent state for a full word time, including start bit, data bits, parity bit, and stop bits. In 16550 mode, it indicates the same condition for the data on top of the FIFO. When the CPU reads USR, it will clear this bit to a logical 0.

Bit 3: NSER. This bit is set to a logical 1 to indicate that the received data have no stop bit. In 16550 mode, it indicates the same condition for the data on top of the FIFO. When the CPU reads USR, it will clear this bit to a logical 0.

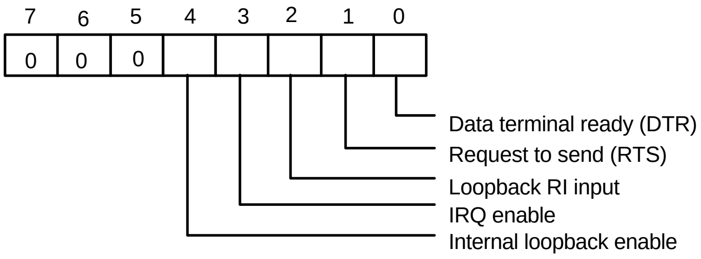
Bit 2: PBER. This bit is set to a logical 1 to indicate that the parity bit of received data is wrong. In 16550 mode, it indicates the same condition for the data on top of the FIFO. When the CPU reads USR, it will clear this bit to a logical 0.

Bit 1: OER. This bit is set to a logical 1 to indicate received data have been overwritten by the next received data before they were read by the CPU. In 16550 mode, it indicates the same condition instead of FIFO full. When the CPU reads USR, it will clear this bit to a logical 0.

Bit 0: RDR. This bit is set to a logical 1 to indicate received data are ready to be read by the CPU in the RBR or FIFO. After no data are left in the RBR or FIFO, the bit will be reset to a logical 0.

3.2.3 Handshake Control Register (HCR) (Read/Write)

This register controls the pins of the UART used for handshaking peripherals such as modem, and controls the diagnostic mode of the UART.



Bit 4: When this bit is set to a logical 1, the UART enters diagnostic mode by an internal loopback, as follows:

(1) SOUT is forced to logical 1, and SIN is isolated from the communication link instead of the TSR.

(2) Modem output pins are set to their inactive state.

(3) Modem input pins are isolated from the communication link and connect internally as DTR (bit 0 of HCR) → $\overline{\text{DSR}}$, RTS (bit 1 of HCR) → $\overline{\text{CTS}}$, Loopback RI input (bit 2 of HCR) → $\overline{\text{RI}}$ and IRQ enable (bit 3 of HCR) → $\overline{\text{DCD}}$.

Aside from the above connections, the UART operates normally. This method allows the CPU to test the UART in a convenient way.

Bit 3: The UART interrupt output is enabled by setting this bit to a logic 1. In the diagnostic mode this bit is internally connected to the modem control input $\overline{\text{DCD}}$.

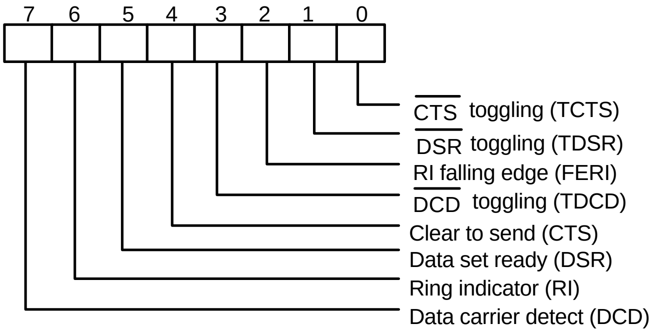
Bit 2: This bit is used only in the diagnostic mode. In the diagnostic mode this bit is internally connected to the modem control input $\overline{\text{RI}}$.

Bit 1: This bit controls the $\overline{\text{RTS}}$ output. The value of this bit is inverted and output to $\overline{\text{RTS}}$.

Bit 0: This bit controls the $\overline{\text{DTR}}$ output. The value of this bit is inverted and output to $\overline{\text{DTR}}$.

3.2.4 Handshake Status Register (HSR) (Read/Write)

This register reflects the current state of four input pins for handshake peripherals such as a modem and records changes on these pins.



Bit 7: This bit is the opposite of the $\overline{\text{DCD}}$ input. This bit is equivalent to bit 3 of HCR in loopback mode.

Bit 6: This bit is the opposite of the $\overline{\text{RI}}$ input. This bit is equivalent to bit 2 of HCR in loopback mode.

Bit 5: This bit is the opposite of the $\overline{\text{DSR}}$ input. This bit is equivalent to bit 0 of HCR in loopback mode.

Bit 4: This bit is the opposite of the $\overline{\text{CTS}}$ input. This bit is equivalent to bit 1 of HCR in loopback mode.

Bit 3: TDCD. This bit indicates that the $\overline{\text{DCD}}$ pin has changed state after HSR was read by the CPU.

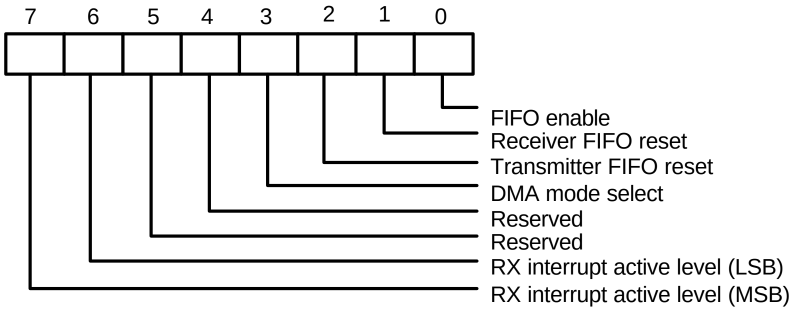
Bit 2: FERI. This bit indicates that the $\overline{\text{RI}}$ pin has changed from low to high state after HSR was read by the CPU.

Bit 1: TDSR. This bit indicates that the $\overline{\text{DSR}}$ pin has changed state after HSR was read by the CPU.

Bit 0: TCTS. This bit indicates that the $\overline{\text{CTS}}$ pin has changed state after HSR was read.

3.2.5 UART FIFO Control Register (UFR) (Write only)

This register is used to control the FIFO functions of the UART.



Bit 6, 7: These two bits are used to set the active level for the receiver FIFO interrupt. For example, if the interrupt active level is set as 4 bytes, once there are more than 4 data characters in the receiver FIFO, the interrupt will be activated to notify the CPU to read the data from the FIFO.

TABLE 3-3 FIFO TRIGGER LEVEL

BIT 7	BIT 6	RX FIFO INTERRUPT ACTIVE LEVEL (BYTES)
0	0	01
0	1	04
1	0	08
1	1	14

Bit 4, 5: Reserved

Bit 3: When this bit is programmed to logic 1, the DMA mode will change from mode 0 to mode 1 if UFR bit 0 = 1.

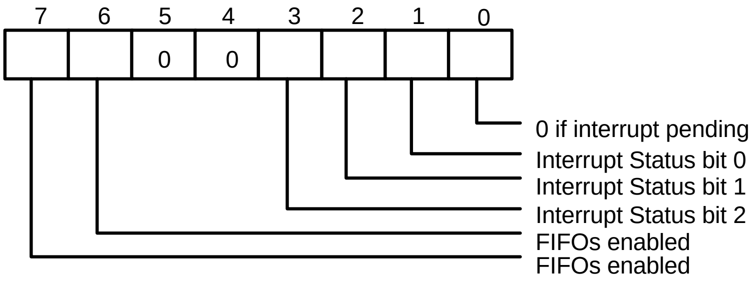
Bit 2: Setting this bit to a logical 1 resets the TX FIFO counter logic to initial state. This bit will clear to a logical 0 by itself after being set to a logical 1.

Bit 1: Setting this bit to a logical 1 resets the RX FIFO counter logic to initial state. This bit will clear to a logical 0 by itself after being set to a logical 1.

Bit 0: This bit enables the 16550 (FIFO) mode of the UART. This bit should be set to a logical 1 before other bits of UFR are programmed.

3.2.6 Interrupt Status Register (ISR) (Read only)

This register reflects the UART interrupt status, which is encoded by different interrupt sources into 3 bits.



Bit 7, 6: These two bits are set to a logical 1 when UFR bit 0 = 1.

Bit 5, 4: These two bits are always logic 0.

Bit 3: In 16450 mode, this bit is 0. In 16550 mode, both bit 3 and 2 are set to a logical 1 when a time-out interrupt is pending.

Bit 2, 1: These two bits identify the priority level of the pending interrupt, as shown in the table below.

Bit 0: This bit is a logical 1 if there is no interrupt pending. If one of the interrupt sources has occurred, this bit will be set to a logical 0.

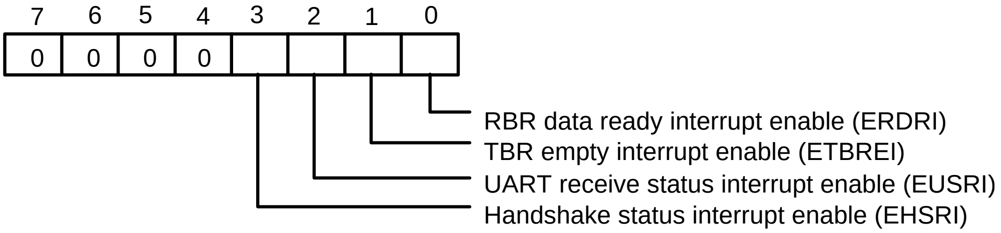
TABLE 3-4 INTERRUPT CONTROL FUNCTION

ISR				INTERRUPT SET AND FUNCTION			
Bit 3	Bit 2	Bit 1	Bit 0	Interrupt priority	Interrupt Type	Interrupt Source	Clear Interrupt
0	0	0	1	-	-	No Interrupt pending	-
0	1	1	0	First	UART Receive Status	1. OER = 1 2. PBER =1 3. NSER = 1 4. SBD = 1	Read USR
0	1	0	0	Second	RBR Data Ready	1. RBR data ready 2. FIFO interrupt active level reached	1. Read RBR 2. Read RBR until FIFO data under active level
1	1	0	0	Second	FIFO Data Timeout	Data present in RX FIFO for 4 characters period of time since last access of RX FIFO.	Read RBR
0	0	1	0	Third	TBR Empty	TBR empty	1. Write data into TBR 2. Read ISR (if priority is third)
0	0	0	0	Fourth	Handshake status	1. TCTS = 1 2. TDSR = 1 3. FERI = 1 4. TDCD = 1	Read HSR

** Bit 3 of ISR is enabled when bit 0 of UFR is logical 1.

3.2.7 Interrupt Control Register (ICR) (Read/Write)

This 8-bit register allows the five types of controller interrupts to activate the interrupt output signal separately. The interrupt system can be totally disabled by resetting bits 0 through 3 of the Interrupt Control Register (ICR). A selected interrupt can be enabled by setting the appropriate bits of this register to a logical 1.


7
6
5
4
3
2
1
0
0
0
0
0
RBR data ready interrupt enable (ERDRI)
TBR empty interrupt enable (ETBREI)
UART receive status interrupt enable (EUSRI)
Handshake status interrupt enable (EHSRI)

Bit 7-4: These four bits are always logic 0.

Bit 3: EHSRI. Setting this bit to a logical 1 enables the handshake status register interrupt.

Bit 2: EUSRI. Setting this bit to a logical 1 enables the UART status register interrupt.

Bit 1: ETBREI. Setting this bit to a logical 1 enables the TBR empty interrupt.

Bit 0: ERDRI. Setting this bit to a logical 1 enables the RBR data ready interrupt.

3.2.8 Programmable Baud Generator (BLL/BHL) (Read/Write)

Two 8-bit registers, BLL and BHL, compose a programmable baud generator that uses 24 MHz to generate a 1.8461 MHz frequency and divides it by a divisor from 1 to 2^{16} -1. The output frequency of the baud generator is the baud rate multiplied by 16, and this is the base frequency for the transmitter and receiver. The table in the next page illustrates the use of the baud generator with a frequency of 1.8461 MHz. In high-speed UART mode (refer to CR0C bit7 and CR0C bit6), the programmable baud generator directly uses 24 MHz and the same divisor as the normal speed divisor. In high-speed mode, the data transmission rate can be as high as 1.5M bps.

3.2.9 User-defined Register (UDR) (Read/Write)

This is a temporary register that can be accessed and defined by the user.

TABLE 3-5 BAUD RATE TABLE

BAUD RATE FROM DIFFERENT PRE-DIVIDER				
Pre-Div: 13 1.8461M Hz	Pre-Div:1.625 14.769M Hz	Pre-Div: 1.0 24M Hz	Decimal divisor used to generate 16X clock	Error Percentage between desired and actual
50	400	650	**2304**	**
75	600	975	**1536**	**
110	880	1430	**1047**	0.18%
134.5	1076	1478.5	**857**	0.099%
150	1200	1950	**768**	**
300	2400	3900	**384**	**
600	4800	7800	**192**	**
1200	9600	15600	**96**	**
1800	14400	23400	**64**	**
2000	16000	26000	**58**	0.53%
2400	19200	31200	**48**	**
3600	28800	46800	**32**	**
4800	38400	62400	**24**	**
7200	57600	93600	**16**	**
9600	76800	124800	**12**	**
19200	153600	249600	**6**	**
38400	307200	499200	**3**	**
57600	460800	748800	**2**	**
115200	921600	1497600	**1**	**

** The percentage error for all baud rates, except where indicated otherwise, is 0.16%.

Note. Pre-Divisor is determined by CRF0 of UART A and B.

4. INFRARED (IR) PORT

The Infrared (IR) function provides point-to-point (or multi-point to multi-point) wireless communication which can operate under various transmission protocols including IrDA 1.0 SIR, SHARP ASK-IR. IR port shares the same port with UART B port in W83977TF. Please refer to section 11.5 for configuration information.

5. PARALLEL PORT

5.1 Printer Interface Logic

The parallel port of the W83977TF makes possible the attachment of various devices that accept eight bits of parallel data at standard TTL level. The W83977TF supports an IBM XT/AT compatible parallel port (SPP), bi-directional parallel port (BPP), Enhanced Parallel Port (EPP), Extended Capabilities Parallel Port (ECP), Extension FDD mode (EXTFDD), Extension 2FDD mode (EXT2FDD) on the parallel port. Refer to the configuration registers for more information on disabling, power-down, and on selecting the mode of operation.

Table 5-1 shows the pin definitions for different modes of the parallel port.

TABLE 5-1-1 PARALLEL PORT CONNECTOR AND PIN DEFINITIONS

HOST CONNECTOR	PIN NUMBER OF W83977TF	PIN ATTRIBUTE	SPP	EPP	ECP
1	36	O	nSTB	nWrite	nSTB, HostClk^2
2-9	31-26, 24-23	I/O	PD<0:7>	PD<0:7>	PD<0:7>
10	22	I	nACK	Intr	nACK, PeriphClk^2
11	21	I	BUSY	nWait	BUSY, PeriphAck^2
12	19	I	PE	PE	PEerror, nAckReverse^2
13	18	I	SLCT	Select	SLCT, Xflag^2
14	35	O	nAFD	nDStrb	nAFD, HostAck^2
15	34	I	nERR	nError	nFault^1, nPeriphRequest^2
16	33	O	nINIT	nInit	nINIT^1, nReverseRqst^2
17	32	O	nSLIN	nAStrb	nSLIN^1 , ECPMode^2

Notes:

n<name > : Active Low

1. Compatible Mode

2. High Speed Mode

3. For more information, refer to the IEEE 1284 standard.

TABLE 5-1-2 PARALLEL PORT CONNECTOR AND PIN DEFINITIONS

HOST CONNECTOR	PIN NUMBER OF W83977TF	PIN ATTRIBUTE	SPP	PIN ATTRIBUTE	EXT2FDD	PIN ATTRIBUTE	EXTFDD
1	36	O	nSTB	---	---	---	---
2	31	I/O	PD0	I	$\overline{\text{INDEX2}}$	I	$\overline{\text{INDEX2}}$
3	30	I/O	PD1	I	$\overline{\text{TRAK02}}$	I	$\overline{\text{TRAK02}}$
4	29	I/O	PD2	I	$\overline{\text{WP2}}$	I	$\overline{\text{WP2}}$
5	28	I/O	PD3	I	$\overline{\text{RDATA2}}$	I	$\overline{\text{RDATA2}}$
6	27	I/O	PD4	I	$\overline{\text{DSKCHG2}}$	I	$\overline{\text{DSKCHG2}}$
7	26	I/O	PD5	---	---	---	---
8	24	I/O	PD6	OD	$\overline{\text{MOA2}}$	---	---
9	23	I/O	PD7	OD	$\overline{\text{DSA2}}$	---	---
10	22	I	nACK	OD	$\overline{\text{DSB2}}$	OD	$\overline{\text{DSB2}}$
11	21	I	BUSY	OD	$\overline{\text{MOB2}}$	OD	$\overline{\text{MOB2}}$
12	19	I	PE	OD	$\overline{\text{WD2}}$	OD	$\overline{\text{WD2}}$
13	18	I	SLCT	OD	$\overline{\text{WE2}}$	OD	$\overline{\text{WE2}}$
14	35	O	nAFD	OD	$\overline{\text{RWC2}}$	OD	$\overline{\text{RWC2}}$
15	34	I	nERR	OD	$\overline{\text{HEAD2}}$	OD	$\overline{\text{HEAD2}}$
16	33	O	nINIT	OD	$\overline{\text{DIR2}}$	OD	$\overline{\text{DIR2}}$
17	32	O	nSLIN	OD	$\overline{\text{STEP2}}$	OD	$\overline{\text{STEP2}}$

5.2 Enhanced Parallel Port (EPP)

TABLE 5-2 PRINTER MODE AND EPP REGISTER ADDRESS

A2	A1	A0	REGISTER	NOTE
0	0	0	Data port (R/W)	1
0	0	1	Printer status buffer (Read)	1
0	1	0	Printer control latch (Write)	1
0	1	0	Printer control swapper (Read)	1
0	1	1	EPP address port (R/W)	2
1	0	0	EPP data port 0 (R/W)	2
1	0	1	EPP data port 1 (R/W)	2
1	1	0	EPP data port 2 (R/W)	2
1	1	1	EPP data port 2 (R/W)	2

Notes:

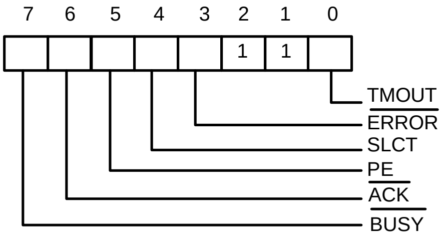
1. These registers are available in all modes.
2. These registers are available only in EPP mode.

5.2.1 Data Swapper

The system microprocessor can read the contents of the printer's data latch by reading the data swapper.

5.2.2 Printer Status Buffer

The system microprocessor can read the printer status by reading the address of the printer status buffer. The bit definitions are as follows:



Bit 7: This signal is active during data entry, when the printer is off-line during printing, when the print head is changing position, or during an error state. When this signal is active, the printer is busy and cannot accept data.

Bit 6: This bit represents the current state of the printer's $\overline{\text{ACK}}$ signal. A 0 means the printer has received a character and is ready to accept another. Normally, this signal will be active for approximately 5 microseconds before $\overline{\text{BUSY}}$ stops.

Bit 5: Logical 1 means the printer has detected the end of paper.

Bit 4: Logical 1 means the printer is selected.

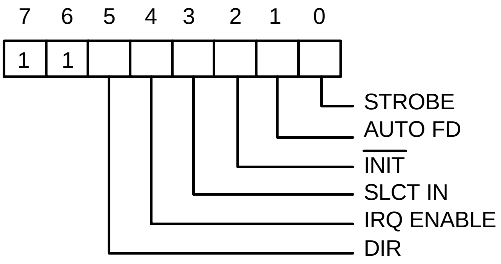
Bit 3: Logical 0 means the printer has encountered an error condition.

Bit 1, 2: These two bits are not implemented and are logic one during a read of the status register.

Bit 0: This bit is valid in EPP mode only. It indicates that a 10 µS time-out has occurred on the EPP bus. A logic 0 means that no time-out error has occurred; a logic 1 means that a time-out error has been detected. Writing a logic 1 to this bit will clear the time-out status bit; writing a logic 0 has no effect.

5.2.3 Printer Control Latch and Printer Control Swapper

The system microprocessor can read the contents of the printer control latch by reading the printer control swapper. Bit definitions are as follows:



Bit 7, 6: These two bits are a logic one during a read. They can be written.

Bit 5: Direction control bit

When this bit is a logic 1, the parallel port is in input mode (read); when it is a logic 0, the parallel port is in output mode (write). This bit can be read and written. In SPP mode, this bit is invalid and fixed at zero.

Bit 4: A 1 in this position allows an interrupt to occur when $\overline{\text{ACK}}$ changes from low to high.

Bit 3: A 1 in this bit position selects the printer.

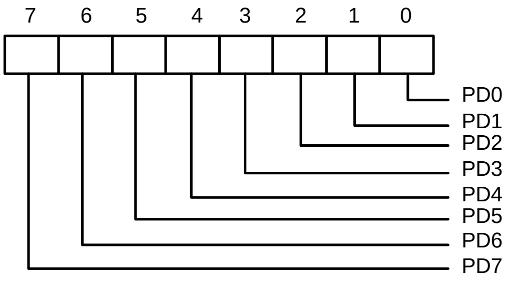
Bit 2: A 0 starts the printer (50 microsecond pulse, minimum).

Bit 1: A 1 causes the printer to line-feed after a line is printed.

Bit 0: A 0.5 microsecond minimum high active pulse clocks data into the printer. Valid data must be present for a minimum of 0.5 microseconds before and after the strobe pulse.

5.2.4 EPP Address Port

The address port is available only in EPP mode. Bit definitions are as follows:

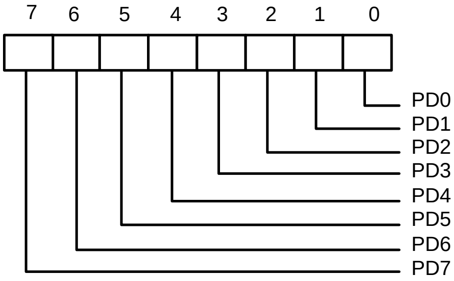


The contents of DB0-DB7 are buffered (non-inverting) and output to ports PD0-PD7 during a write operation. The leading edge of $\overline{IOW}$ causes an EPP address write cycle to be performed, and the trailing edge of $\overline{IOW}$ latches the data for the duration of the EPP write cycle.

PD0-PD7 ports are read during a read operation. The leading edge of $\overline{IOR}$ causes an EPP address read cycle to be performed and the data to be output to the host CPU.

5.2.5 EPP Data Port 0-3

These four registers are available only in EPP mode. Bit definitions of each data port are as follows:



When accesses are made to any EPP data port, the contents of DB0-DB7 are buffered (non-inverting) and output to the ports PD0-PD7 during a write operation. The leading edge of $\overline{IOW}$ causes an EPP data write cycle to be performed, and the trailing edge of $\overline{IOW}$ latches the data for the duration of the EPP write cycle.

During a read operation, ports PD0-PD7 are read, and the leading edge of $\overline{IOR}$ causes an EPP read cycle to be performed and the data to be output to the host CPU.

5.2.6 Bit Map of Parallel Port and EPP Registers

REGISTER	7	6	5	4	3	2	1	0
Data Port (R/W)	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
Status Buffer (Read)	$\overline{BUSY}$	$\overline{ACK}$	PE	SLCT	$\overline{ERROR}$	1	1	TMOUT
Control Swapper (Read)	1	1	1	IRQEN	SLIN	$\overline{INIT}$	$\overline{AUTOFD}$	$\overline{STROBE}$
Control Latch (Write)	1	1	DIR	IRQ	SLIN	$\overline{INIT}$	$\overline{AUTOFD}$	$\overline{STROBE}$
EPP Address Port R/W)	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
EPP Data Port 0 (R/W)	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
EPP Data Port 1 (R/W)	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0

EPP Data Port 2 (R/W)	PD7	PD6	PD 5	PD4	PD3	PD2	PD1	PD0
EPP Data Port 3 (R/W)	PD7	PD6	PD 5	PD4	PD3	PD2	PD1	PD0

5.2.7 EPP Pin Descriptions

EPP NAME	TYPE	EPP DESCRIPTION
nWrite	O	Denotes an address or data read or write operation.
PD<0:7>	I/O	Bi-directional EPP address and data bus.
Intr	I	Used by peripheral device to interrupt the host.
nWait	I	Inactive to acknowledge that data transfer is completed. Active to indicate that the device is ready for the next transfer.
PE	I	Paper end; same as SPP mode.
Select	I	Printer selected status; same as SPP mode.
nDStrb	O	This signal is active low. It denotes a data read or write operation.
nError	I	Error; same as SPP mode.
nInits	O	This signal is active low. When it is active, the EPP device is reset to its initial operating mode.
nAStrb	O	This signal is active low. It denotes an address read or write operation.

5.2.8 EPP Operation

When the EPP mode is selected in the configuration register, the standard and bi-directional modes are also available. The PDx bus is in the standard or bi-directional mode when no EPP read, write, or address cycle is currently being executed. In this condition all output signals are set by the SPP Control Port and the direction is controlled by DIR of the Control Port.

A watchdog timer is required to prevent system lockup. The timer indicates that more than 10 µS have elapsed from the start of the EPP cycle to the time $\overline{\text{WAIT}}$ is deasserted. The current EPP cycle is aborted when a time-out occurs. The time-out condition is indicated in Status bit 0.

5.2.8.1 EPP Operation

The EPP operates on a two-phase cycle. First, the host selects the register within the device for subsequent operations. Second, the host performs a series of read and/or write byte operations to the selected register. Four operations are supported on the EPP: Address Write, Data Write, Address Read, and Data Read. All operations on the EPP device are performed asynchronously.

5.2.8.2 EPP Version 1.9 Operation

The EPP read/write operation can be completed under the following conditions:

a. If the nWait is active low, when the read cycle (nWrite inactive high, nDStrb/nAStrb active low) or write cycle (nWrite active low, nDStrb/nAStrb active low) starts, the read/write cycle proceeds normally and will be completed when nWait goes inactive high.

b. If nWait is inactive high, the read/write cycle will not start. It must wait until nWait changes to active low, at which time it will start as described above.

5.2.8.3 EPP Version 1.7 Operation

The EPP read/write cycle can start without checking whether nWait is active or inactive. Once the read/write cycle starts, however, it will not terminate until nWait changes from active low to inactive high.

5.3 Extended Capabilities Parallel (ECP) Port

This port is software and hardware compatible with existing parallel ports, so it may be used as a standard printer mode if ECP is not required. It provides an automatic high burst-bandwidth channel that supports DMA for ECP in both the forward (host to peripheral) and reverse (peripheral to host) directions.

Small FIFOs are used in both forward and reverse directions to improve the maximum bandwidth requirement. The size of the FIFO is 16 bytes. The ECP port supports an automatic handshake for the standard parallel port to improve compatibility mode transfer speed.

The ECP port supports run-length-encoded (RLE) decompression (required) in hardware. Compression is accomplished by counting identical bytes and transmitting an RLE byte that indicates how many times the next byte is to be repeated. Hardware support for compression is optional.

For more information about the ECP Protocol, refer to the Extended Capabilities Port Protocol and ISA Interface Standard.

5.3.1 ECP Register and Mode Definitions

NAME	ADDRESS	I/O	ECP MODES	FUNCTION
data	Base+000h	R/W	000-001	Data Register
ecpAFifo	Base+000h	R/W	011	ECP FIFO (Address)
dsr	Base+001h	R	All	Status Register
dcr	Base+002h	R/W	All	Control Register
cFifo	Base+400h	R/W	010	Parallel Port Data FIFO
ecpDFifo	Base+400h	R/W	011	ECP FIFO (DATA)
tFifo	Base+400h	R/W	110	Test FIFO
cnfgA	Base+400h	R	111	Configuration Register A
cnfgB	Base+401h	R/W	111	Configuration Register B
ecr	Base+402h	R/W	All	Extended Control Register

Note: The base addresses are specified by CR60 and 61, which are determined by configuration register or hardware setting.

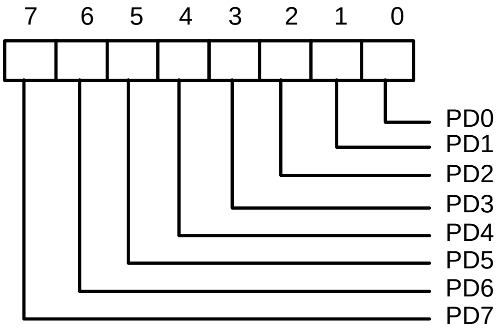
MODE	DESCRIPTION
000	SPP mode
001	PS/2 Parallel Port mode
010	Parallel Port Data FIFO mode
011	ECP Parallel Port mode
100	EPP mode (If this option is enabled in the CRF0 to select ECP/EPP mode)
101	Reserved
110	Test mode
111	Configuration mode

Note: The mode selection bits are bit 7-5 of the Extended Control Register.

5.3.2 Data and ecpAFifo Port

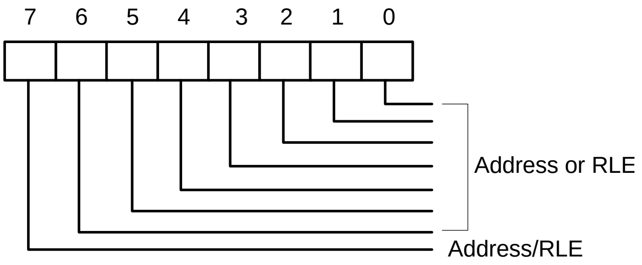
Modes 000 (SPP) and 001 (PS/2) (Data Port)

During a write operation, the Data Register latches the contents of the data bus on the rising edge of the input. The contents of this register are output to the PD0-PD7 ports. During a read operation, ports PD0-PD7 are read and output to the host. The bit definitions are as follows:


7
6
5
4
3
2
1
0
PD0
PD1
PD2
PD3
PD4
PD5
PD6
PD7

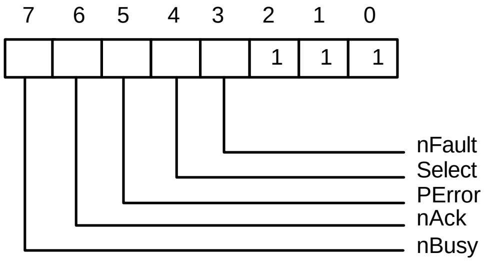
Mode 011 (ECP FIFO-Address/RLE)

A data byte written to this address is placed in the FIFO and tagged as an ECP Address/RLE. The hardware at the ECP port transmits this byte to the peripheral automatically. The operation of this register is defined only for the forward direction. The bit definitions are as follows:


7
6
5
4
3
2
1
0
Address or RLE
Address/RLE

5.3.3 Device Status Register (DSR)

These bits are at low level during a read of the Printer Status Register. The bits of this status register are defined as follows:


7
6
5
4
3
2
1
0
1
1
1
nFault
Select
PError
nAck
nBusy

Bit 7: This bit reflects the complement of the Busy input.

Bit 6: This bit reflects the nAck input.

Bit 5: This bit reflects the PError input.

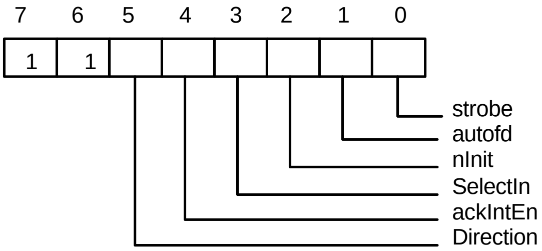
Bit 4: This bit reflects the Select input.

Bit 3: This bit reflects the nFault input.

Bit 2-0: These three bits are not implemented and are always logic one during a read.

5.3.4 Device Control Register (DCR)

The bit definitions are as follows:



Bit 6, 7: These two bits are logic one during a read and cannot be written.

Bit 5: This bit has no effect and the direction is always out if mode = 000 or mode = 010. Direction is valid in all other modes.

0 the parallel port is in output mode.
1 the parallel port is in input mode.

Bit 4: Interrupt request enable. When this bit is set to a high level, it may be used to enable interrupt requests from the parallel port to the CPU due to a low to high transition on the $\overline{\text{ACK}}$ input.

Bit 3: This bit is inverted and output to the $\overline{\text{SLIN}}$ output.

0 The printer is not selected.
1 The printer is selected.

Bit 2: This bit is output to the $\overline{\text{INIT}}$ output.

Bit 1: This bit is inverted and output to the $\overline{\text{AFD}}$ output.

Bit 0: This bit is inverted and output to the $\overline{\text{STB}}$ output.

5.3.5 cFifo (Parallel Port Data FIFO) Mode = 010

This mode is defined only for the forward direction. The standard parallel port protocol is used by a hardware handshake to the peripheral to transmit bytes written or DMAed from the system to this FIFO. Transfers to the FIFO are byte aligned.

5.3.6 ecpDFifo (ECP Data FIFO) Mode = 011

When the direction bit is 0, bytes written or DMAed from the system to this FIFO are transmitted by a hardware handshake to the peripheral using the ECP parallel port protocol. Transfers to the FIFO are byte aligned.

When the direction bit is 1, data bytes from the peripheral are read under automatic hardware handshake from ECP into this FIFO. Reads or DMAs from the FIFO will return bytes of ECP data to the system.

5.3.7 tFifo (Test FIFO Mode) Mode = 110

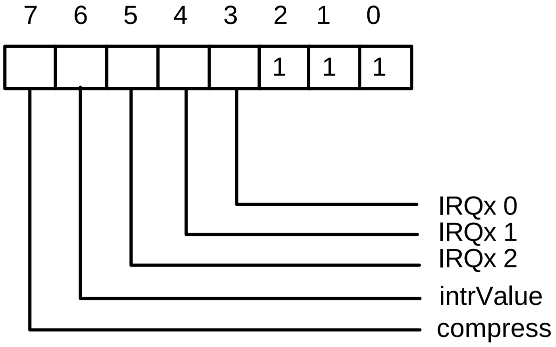
Data bytes may be read, written, or DMAed to or from the system to this FIFO in any direction. Data in the tFIFO will not be transmitted to the parallel port lines. However, data in the tFIFO may be displayed on the parallel port data lines.

5.3.8 cnfgA (Configuration Register A) Mode = 111

This register is a read-only register. When it is read, 10H is returned. This indicates to the system that this is an 8-bit implementation.

5.3.9 cnfgB (Configuration Register B) Mode = 111

The bit definitions are as follows:



Bit 7: This bit is read-only. It is at low level during a read. This means that this chip does not support hardware RLE compression.

Bit 6: Returns the value on the ISA IRQ line to determine possible conflicts.

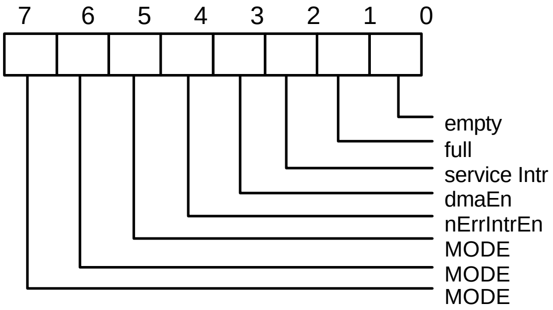
Bit 5-3: Reflect the IRQ resource assigned for ECP port.

cnfgB[5:3]	IRQ resource
000	reflect other IRQ resources selected by PnP register (default)
001	IRQ7
010	IRQ9
011	IRQ10
100	IRQ11
101	IRQ14
110	IRQ15
111	IRQ5

Bit 2-0: These five bits are at high level during a read and can be written.

5.3.10 ecr (Extended Control Register) Mode = all

This register controls the extended ECP parallel port functions. The bit definitions are follows:



Bit 7-5: These bits are read/write and select the mode.

000	Standard Parallel Port mode. The FIFO is reset in this mode.
001	PS/2 Parallel Port mode. This is the same as 000 except that direction may be used to tri-state the data lines and reading the data register returns the value on the data lines and not the value in the data register.
010	Parallel Port FIFO mode. This is the same as 000 except that bytes are written or DMAed to the FIFO. FIFO data are automatically transmitted using the standard parallel port protocol. This mode is useful only when direction is 0.
011	ECP Parallel Port Mode. When the direction is 0 (forward direction), bytes placed into the ecpDFifo and bytes written to the ecpAFifo are placed in a single FIFO and auto transmitted to the peripheral using ECP Protocol. When the direction is 1 (reverse direction), bytes are moved from the ECP parallel port and packed into bytes in the ecpDFifo.
100	Selects EPP Mode. In this mode, EPP is activated if the EPP mode is selected.
101	Reserved.
110	Test Mode. The FIFO may be written and read in this mode, but the data will not be transmitted on the parallel port.
111	Configuration Mode. The confgA and confgB registers are accessible at 0x400 and 0x401 in this mode.

Bit 4: Read/Write (Valid only in ECP Mode)

1 Disables the interrupt generated on the asserting edge of nFault.

0 Enables an interrupt pulse on the high to low edge of nFault. If nFault is asserted (interrupt) an interrupt will be generated and this bit is written from a 1 to 0.

Bit 3: Read/Write

1 Enables DMA.

0 Disables DMA unconditionally.

Bit 2: Read/Write

1 Disables DMA and all of the service interrupts.

0 Enables one of the following cases of interrupts. When one of the service interrupts has occurred, the serviceIntr bit is set to a 1 by hardware. This bit must be reset to 0 to re-enable the interrupts. Writing a 1 to this bit will not cause an interrupt.

(a) dmaEn = 1: During DMA this bit is set to a 1 when terminal count is reached.

(b) dmaEn = 0 direction = 0: This bit is set to 1 whenever there are writeIntr Threshold or more bytes free in the FIFO.

(c) dmaEn = 0 direction = 1: This bit is set to 1 whenever there are readIntr Threshold or more valid bytes to be read from the FIFO.

Bit 1: Read only

0 The FIFO has at least 1 free byte.

1 The FIFO cannot accept another byte or the FIFO is completely full.

Bit 0: Read only

0 The FIFO contains at least 1 byte of data.

1 The FIFO is completely empty.

5.3.11 Bit Map of ECP Port Registers

	D7	D6	D5	D4	D3	D2	D1	D0	NOTE
data	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0	
ecpAFifo	Addr/RLE	Address or RLE field							2
dsr	nBusy	nAck	PError	Select	nFault	1	1	1	1
dcr	1	1	Directio	ackIntEn	SelectIn	nInit	autofd	strobe	1
cFifo	Parallel Port Data FIFO								2
ecpDFifo	ECP Data FIFO								2
tFifo	Test FIFO								2
cnfgA	0	0	0	1	0	0	0	0	
cnfgB	compress	intrValue	1	1	1	1	1	1	
ecr	MODE			nErrIntrEn	dmaEn	serviceIntr	full	empty	

Notes:

1. These registers are available in all modes.
2. All FIFOs use one common 16-byte FIFO.

5.3.12 ECP Pin Descriptions

NAME	TYPE	DESCRIPTION
nStrobe (HostClk)	O	The nStrobe registers data or address into the slave on the asserting edge during write operations. This signal handshakes with Busy.
PD<7:0>	I/O	These signals contains address or data or RLE data.
nAck (PeriphClk)	I	This signal indicates valid data driven by the peripheral when asserted. This signal handshakes with nAutoFd in reverse.
Busy (PeriphAck)	I	This signal deasserts to indicate that the peripheral can accept data. It indicates whether the data lines contain ECP command information or data in the reverse direction. When in reverse direction, normal data are transferred when Busy (PeriphAck) is high and an 8-bit command is transferred when it is low.
PError (nAckReverse)	I	This signal is used to acknowledge a change in the direction of the transfer (asserted = forward). The peripheral drives this signal low to acknowledge nReverseRequest. The host relies upon nAckReverse to determine when it is permitted to drive the data bus.
Select (Xflag)	I	Indicates printer on line.
nAutoFd (HostAck)	O	Requests a byte of data from the peripheral when it is asserted. This signal indicates whether the data lines contain ECP address or data in the forward direction. When in forward direction, normal data are transferred when nAutoFd (HostAck) is high and an 8-bit command is transferred when it is low.
nFault (nPeriphRequest)	I	Generates an error interrupt when it is asserted. This signal is valid only in the forward direction. The peripheral is permitted (but not required) to drive this pin low to request a reverse transfer during ECP Mode.
nInit (nReverseRequest)	O	This signal sets the transfer direction (asserted = reverse, deasserted = forward). This pin is driven low to place the channel in the reverse direction.
nSelectIn (ECPMode)	O	This signal is always deasserted in ECP mode.

5.3.13 ECP Operation

The host must negotiate on the parallel port to determine if the peripheral supports the ECP protocol before ECP operation. After negotiation, it is necessary to initialize some of the port bits. The following are required:

(a) Set direction = 0, enabling the drivers.
(b) Set strobe = 0, causing the nStrobe signal to default to the deasserted state.
(c) Set autoFd = 0, causing the nAutoFd signal to default to the deasserted state.
(d) Set mode = 011 (ECP Mode)

ECP address/RLE bytes or data bytes may be sent automatically by writing the ecpAFifo or ecpDFifo, respectively.

5.3.13.1 Mode Switching

Software will execute P1284 negotiation and all operations prior to a data transfer phase under programmed I/O control (mode 000 or 001). Hardware provides an automatic control line handshake, moving data between the FIFO and the ECP port only in the data transfer phase (mode 011 or 010).

If the port is in mode 000 or 001 it may switch to any other mode. If the port is not in mode 000 or 001 it can only be switched into mode 000 or 001. The direction can be changed only in mode 001.

When in extended forward mode, the software should wait for the FIFO to be empty before switching back to mode 000 or 001. In ECP reverse mode the software waits for all the data to be read from the FIFO before changing back to mode 000 or 001.

5.3.13.2 Command/Data

ECP mode allows the transfer of normal 8-bit data or 8-bit commands. In the forward direction, normal data are transferred when HostAck is high and an 8-bit command is transferred when HostAck is low. The most significant bits of the command indicate whether it is a run-length count (for compression) or a channel address.

In the reverse direction, normal data are transferred when PeriphAck is high and an 8-bit command is transferred when PeriphAck is low. The most significant bit of the command is always zero.

5.3.13.3 Data Compression

The W83977TF supports run length encoded (RLE) decompression in hardware and can transfer compressed data to a peripheral. Note that the odd (RLE) compression in hardware is not supported. In order to transfer data in ECP mode, the compression count is written to the ecpAFifo and the data byte is written to the ecpDFifo.

5.3.14 FIFO Operation

The FIFO threshold is set in configuration register 5. All data transfers to or from the parallel port can proceed in DMA or Programmed I/O (non-DMA) mode, as indicated by the selected mode. The FIFO is used by selecting the Parallel Port FIFO mode or ECP Parallel Port Mode. After a reset, the FIFO is disabled.

5.3.15 DMA Transfers

DMA transfers are always to or from the ecpDFifo, tFifo, or CFifo. The DMA uses the standard PC DMA services. The ECP requests DMA transfers from the host by activating the PDRQ pin. The DMA will empty or fill the FIFO using the appropriate direction and mode. When the terminal count in the DMA controller is reached, an interrupt is generated and serviceIntr is asserted, which will disable the DMA.

5.3.16 Programmed I/O (NON-DMA) Mode

The ECP or parallel port FIFOs can also be operated using interrupt driven programmed I/O. Programmed I/O transfers are to the ecpDFifo at 400H and ecpAFifo at 000H or from the ecpDFifo located at 400H, or to/from the tFifo at 400H. The host must set the direction, state, dmaEn = 0 and serviceIntr = 0 in the programmed I/O transfers.

The ECP requests programmed I/O transfers from the host by activating the IRQ pin. The programmed I/O will empty or fill the FIFO using the appropriate direction and mode.

5.4 Extension FDD Mode (EXTFDD)

In this mode, the W83977TF changes the printer interface pins to FDC input/output pins, allowing the user to install a second floppy disk drive (FDD B) through the DB-25 printer connector. The pin assignments for the FDC input/output pins are shown in Table 5-1.

After the printer interface is set to EXTFDD mode, the following occur:

(1) Pins $\overline{\text{MOB}}$ and $\overline{\text{DSB}}$ will be forced to inactive state.

(2) Pins $\overline{\text{DSKCHG}}$, $\overline{\text{RDATA}}$, $\overline{\text{WP}}$, $\overline{\text{TRAK0}}$, $\overline{\text{INDEX}}$ will be logically ORed with pins PD4-PD0 to serve as input signals to the FDC.

(3) Pins PD4-PD0 each will have an internal resistor of about 1K ohm to serve as pull-up resistor for FDD open drain/collector output.

(4) If the parallel port is set to EXTFDD mode after the system has booted DOS or another operating system, a warm reset is needed to enable the system to recognize the extension floppy drive.

5.5 Extension 2FDD Mode (EXT2FDD)

In this mode, the W83977TF changes the printer interface pins to FDC input/output pins, allowing the user to install two external floppy disk drives through the DB-25 printer connector to replace internal floppy disk drives A and B. The pin assignments for the FDC input/output pins are shown in Table5-1.

After the printer interface is set to EXTFDD mode, the following occur:

(1) Pins $\overline{\text{MOA}}$, $\overline{\text{DSA}}$, $\overline{\text{MOB}}$, and $\overline{\text{DSB}}$ will be forced to inactive state.

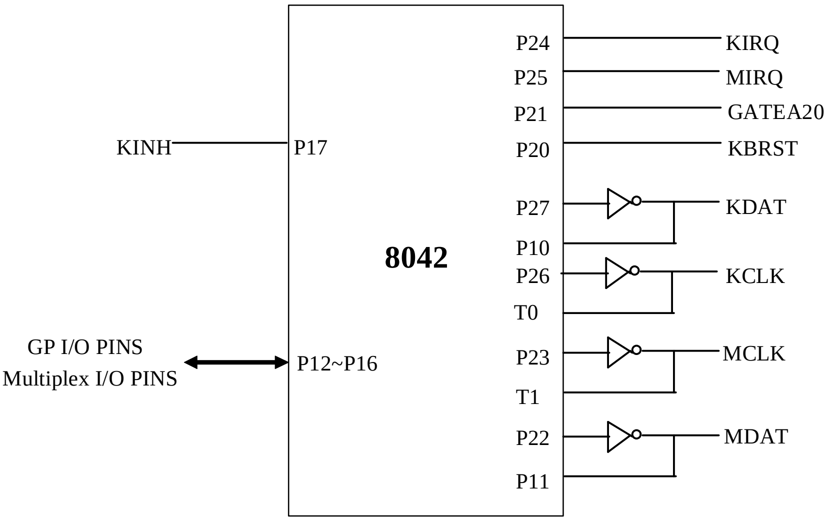
(2) Pins $\overline{\text{DSKCHG}}$, $\overline{\text{RDATA}}$, $\overline{\text{WP}}$, $\overline{\text{TRAK0}}$, and $\overline{\text{INDEX}}$ will be logically ORed with pins PD4-PD0 to serve as input signals to the FDC.

(3) Pins PD4-PD0 each will have an internal resistor of about 1K ohm to serve as pull-up resistor for FDD open drain/collector output.

(4) If the parallel port is set to EXT2FDD mode after the system has booted DOS or another operating system, a warm reset is needed to enable the system to recognize the extension floppy drive.

6. KEYBOARD CONTROLLER

The KBC (8042 with licensed KB BIOS) circuit of W83977TF is designed to provide the functions needed to interface a CPU with a keyboard and/or a PS/2 mouse, and can be used with IBM®-compatible personal computers or PS/2-based systems. The controller receives serial data from the keyboard or PS/2 mouse, checks the parity of the data, and presents the data to the system as a byte of data in its output buffer. Then, the controller will assert an interrupt to the system when data are placed in its output buffer. The keyboard and PS/2 mouse are required to acknowledge all data transmissions. No transmission should be sent to the keyboard or PS/2 mouse until an acknowledge is received for the previous data byte.



Keyboard and Mouse Interface

6.1 Output Buffer

The output buffer is an 8-bit read-only register at I/O address 60H (Default, PnP programmable I/O address LD5-CR60 and LD5-CR61). The keyboard controller uses the output buffer to send the scan code received from the keyboard and data bytes required by commands to the system. The output buffer can only be read when the output buffer full bit in the register is "1".

6.2 Input Buffer

The input buffer is an 8-bit write-only register at I/O address 60H or 64H (Default, PnP programmable I/O address LD5-CR60, LD5-CR61, LD5-CR62, and LD5-CR63). Writing to address 60H sets a flag to indicate a data write; writing to address 64H sets a flag to indicate a command write. Data written to I/O address 60H is sent to keyboard (unless the keyboard controller is expecting a data byte) through the controller's input buffer only if the input buffer full bit in the status register is 0 .

6.3 Status Register

The status register is an 8-bit read-only register at I/O address 64H (Default, PnP programmable I/O address LD5-CR62 and LD5-CR63), that holds information about the status of the keyboard controller and interface. It may be read at any time.

BIT	BIT FUNCTION	DESCRIPTION
0	Output Buffer Full	0: Output buffer empty 1: Output buffer full
1	Input Buffer Full	0: Input buffer empty 1: Input buffer full
2	System Flag	This bit may be set to 0 or 1 by writing to the system flag bit in the command byte of the keyboard controller. It defaults to 0 after a power-on reset.
3	Command/Data	0: Data byte 1: Command byte
4	Inhibit Switch	0: Keyboard is inhibited 1: Keyboard is not inhibited
5	Auxiliary Device Output Buffer	0: Auxiliary device output buffer empty 1: Auxiliary device output buffer full
6	General Purpose Time-out	0: No time-out error 1: Time-out error
7	Parity Error	0: Odd parity 1: Even parity (error)

6.4 Commands

<table>
<tr><th>COMMAND</th><th>FUNCTION</th></tr>
<tr><td>20h</td><td>Read Command Byte of Keyboard Controller</td></tr>
<tr><td>60h</td><td>Write Command Byte of Keyboard Controller
<table>
<tr><th>BIT</th><th>BIT DEFINITION</th></tr>
<tr><td>7</td><td>Reserved</td></tr>
<tr><td>6</td><td>IBM Keyboard Translate Mode</td></tr>
<tr><td>5</td><td>Disable Auxiliary Device</td></tr>
<tr><td>4</td><td>Disable Keyboard</td></tr>
<tr><td>3</td><td>Reserve</td></tr>
<tr><td>2</td><td>System Flag</td></tr>
<tr><td>1</td><td>Enable Auxiliary Interrupt</td></tr>
<tr><td>0</td><td>Enable Keyboard Interrupt</td></tr>
</table></td></tr>
<tr><td>A4h</td><td>Test Password
Returns 0Fah if Password is loaded
Returns 0F1h if Password is not loaded</td></tr>
</table>

6.4 Commands, continued

<table>
<tr><th>COMMAND</th><th>FUNCTION</th></tr>
<tr><td>A5h</td><td>Load Password
Load Password until a "0" is received from the system</td></tr>
<tr><td>A6h</td><td>Enable Password
Enable the checking of keystrokes for a match with the password</td></tr>
<tr><td>A7h</td><td>Disable Auxiliary Device Interface</td></tr>
<tr><td>A8h</td><td>Enable Auxiliary Device Interface</td></tr>
<tr><td>A9h</td><td>Interface Test
<table>
<tr><th>BIT</th><th>BIT DEFINITION</th></tr>
<tr><td>00</td><td>No Error Detected</td></tr>
<tr><td>01</td><td>Auxiliary Device "Clock" line is stuck low</td></tr>
<tr><td>02</td><td>Auxiliary Device "Clock" line is stuck high</td></tr>
<tr><td>03</td><td>Auxiliary Device "Data" line is stuck low</td></tr>
<tr><td>04</td><td>Auxiliary Device "Data" line is stuck low</td></tr>
</table></td></tr>
<tr><td>AAh</td><td>Self-test
Returns 055h if self test succeeds</td></tr>
<tr><td>ABh</td><td>Interface Test
<table>
<tr><th>BIT</th><th>BIT DEFINITION</th></tr>
<tr><td>00</td><td>No Error Detected</td></tr>
<tr><td>01</td><td>Keyboard "Clock" line is stuck low</td></tr>
<tr><td>02</td><td>Keyboard "Clock" line is stuck high</td></tr>
<tr><td>03</td><td>Keyboard "Data" line is stuck low</td></tr>
<tr><td>04</td><td>Keyboard "Data" line is stuck high</td></tr>
</table></td></tr>
<tr><td>ADh</td><td>Disable Keyboard Interface</td></tr>
<tr><td>AEh</td><td>Enable Keyboard Interface</td></tr>
<tr><td>C0h</td><td>Read Input Port(P1) and send data to the system</td></tr>
<tr><td>C1h</td><td>Continuously puts the lower four bits of Port1 into STATUS register</td></tr>
<tr><td>C2h</td><td>Continuously puts the upper four bits of Port1 into STATUS register</td></tr>
<tr><td>D0h</td><td>Send Port2 value to the system</td></tr>
<tr><td>D1h</td><td>Only set/reset GateA20 line based on the system data bit 1</td></tr>
<tr><td>D2h</td><td>Send data back to the system as if it came from Keyboard</td></tr>
<tr><td>D3h</td><td>Send data back to the system as if it came from Auxiliary Device</td></tr>
<tr><td>D4h</td><td>Output next received byte of data from system to Auxiliary Device</td></tr>
<tr><td>E0h</td><td>Reports the status of the test inputs</td></tr>
<tr><td>FXh</td><td>Pulse only RC(the reset line) low for 6µS if Command byte is even</td></tr>
</table>

6.5 Hardware GATEA20/Keyboard Reset Control Logic

The KBC implements a hardware control logic to speed-up GATEA20 and KBRESET. This control logic is controlled by LD5-CRF0 as follows:

6.5.1 KB Control Register (Logic Device 5, CR-F0)

BIT	7	6	5	4	3	2	1	0
NAME	KCLKS1	KCLKS0	Reserved	Reserved	Reserved	P92EN	HGA20	HKBRST

KCLKS1, KCLKS0

This 2 bits are for the KBC clock rate selection.

= 0 0	KBC clock input is 6 Mhz
= 0 1	KBC clock input is 8 Mhz
= 1 0	KBC clock input is 12 Mhz
= 1 1	KBC clock input is 16 Mhz

P92EN (Port 92 Enable)

A "1" on this bit enables Port 92 to control GATEA20 and KBRESET.

A "0" on this bit disables Port 92 functions.

HGA20 (Hardware GATE A20)

A "1" on this bit selects hardware GATEA20 control logic to control GATE A20 signal.

A "0" on this bit disables hardware GATEA20 control logic function.

HKBRST (Hardware Keyboard Reset)

A "1" on this bit selects hardware KB RESET control logic to control KBRESET signal.

A "0" on this bit disables hardware KB RESET control logic function.

When the KBC receives data that follows a "D1" command, the hardware control logic sets or clears GATE A20 according to the received data bit 1. Similarly, the hardware control logic sets or clears KBRESET depending on the received data bit 0. When the KBC receives a "FE" command, the KBRESET is pulse low for 6µS(Min.) with 14µS(Min.) delay.

GATEA20 and KBRESET are controlled by either the software control or the hardware control logic and they are mutually exclusive. Then, GATEA20 and KBRESET are merged along with Port92 when P92EN bit is set.

6.5.2 Port 92 Control Register (Default Value = 0x24)

BIT	7	6	5	4	3	2	1	0
NAME	Res. (0)	Res. (0)	Res. (1)	Res. (0)	Res. (0)	Res. (1)	SGA20	PLKBRST

SGA20 (Special GATE A20 Control)

A "1" on this bit drives GATE A20 signal to high.

A "0" on this bit drives GATE A20 signal to low.

PLKBRST (Pull-Low KBRESET)

A "1" on this bit causes KBRESET to drive low for 6µS(Min.) with 14µS(Min.) delay. Before issuing another keyboard reset command, the bit must be cleared.

6.6 OnNow / Security Keyboard and Mouse Wake-Up

---- Programmable Keyboard / Mouse Wake-Up Functions

Winbond's unique programmable keyboard/ mouse wake-up functions provide the system diversified methods for either OnNow wake-up application, or security control application. The keyboard or mouse can wake up the system by producing a panel switch low pulse on $\overline{\text{PANSWOUT}}$ pin, and connect it to chipset (for example Intel^{TM} chipset TX, LX PIIX4) panel switch input. The wake-up conditions can be programmed as pre-determined or any keys/buttons. To implement this function, a 32.768KHz crystal must be installed between XTAL1 and XTAL2, or a 32.768KHz clock to be connected to XTAL1 and leave XTAL2 open. The VSB pin must be connected to +5V VSB of ATX power supply, and an external battery should be installed on VBAT pin to store the data (the passwords and wake-up status which had been set already) when power fails.

6.6.1 Keyboard Wake-Up Function

The keyboard wake-up function is enable by setting LD-0A CR-E0 bit 6. The pre-determined keys data are stored in registers, and they can be access by an indirection method. At first, write their index address to LD-0A CR-E1, then access them by reading/writing LD-0A CR-E2. A zero data is written to the register means the comparison of this register will be ignored. The pre-programmed keys may be 1 to 5 keys with various combinations. If LD-0A CR-E0 bit 0 is set, the system will be waken up after any key struck.

6.6.2 Keyboard Password Wake-Up Function

To implement this function, the bit 7 of LD-0A CR-E0 must be set, and panel switch input is connected to $\overline{\text{PANSWIN}}$ pin. Thus $\overline{\text{PANSWIN}}$ is blocked to $\overline{\text{PANSWOUT}}$, by setting LD-0A CR-E0 properly and make only keyboard can wake up the system with preset keys (password).

6.6.3 Mouse Wake-Up Function

The mouse wake-up function is activated by setting bit 5 of LD-0A CR-E0. If bit 1 of LD-0A CR-E0 is set, any movement or button clicking will make up the system. Otherwise, the mouse can wake up the system only by clicking its button twice successively with the mouse unmoved. The bit 4 of LD-0A CR-E0 determines which button (left or right) to perform wake-up function.

7. GENERAL PURPOSE I/O

W83977TF provides 23 Input/Output ports that can be individually configured to perform a simple basic I/O function or a pre-defined alternate function. Those 23 GP I/O ports are divided into three groups, the first group contains 8 ports, the second group contains only 7 ports, and the third group contains 8 ports. Each port in first group corresponds to a configuration register in logical device 7, the second group in logical device 8, and the third group in logical device 9. Users can select those I/O ports functions by independently programming those configuration registers. Figure 7.1, 7.2, and 7.3 respectively show the GP I/O port's structure of logical device 7, 8, and 9. Right after Power-on reset, those ports default to perform basic I/O functions.

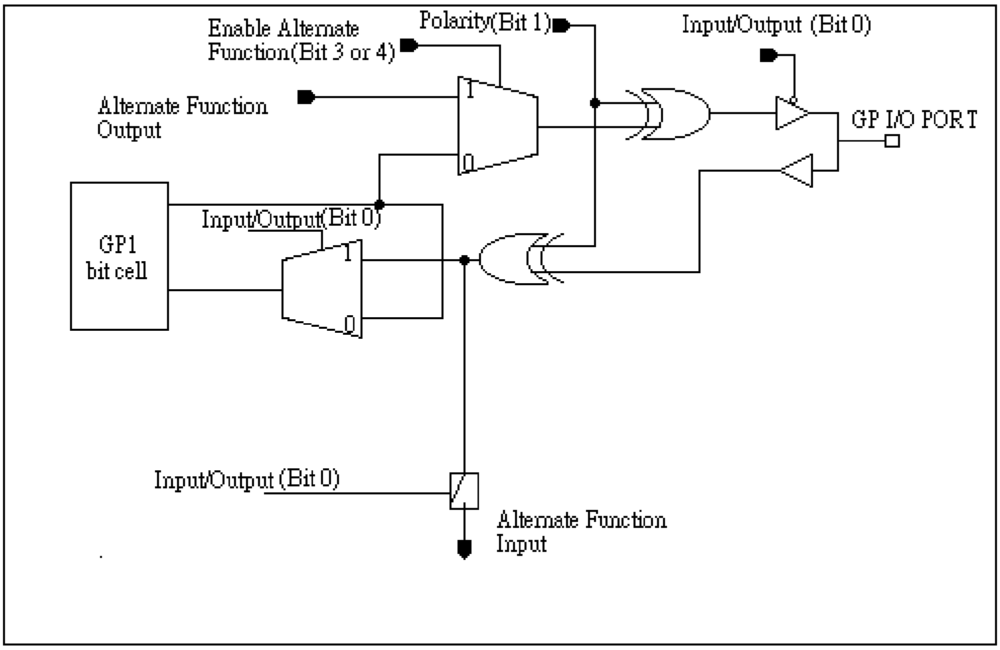

Enable Alternate
Function(Bit 3 or 4)
Polarity(Bit 1)
Input/Output (Bit 0)
Alternate Function
Output
1
0
GP I/O PORT
GP1
bit cell
Input/Output(Bit 0)
1
0
Input/Output (Bit 0)
Alternate Function
Input

Figure 7.1

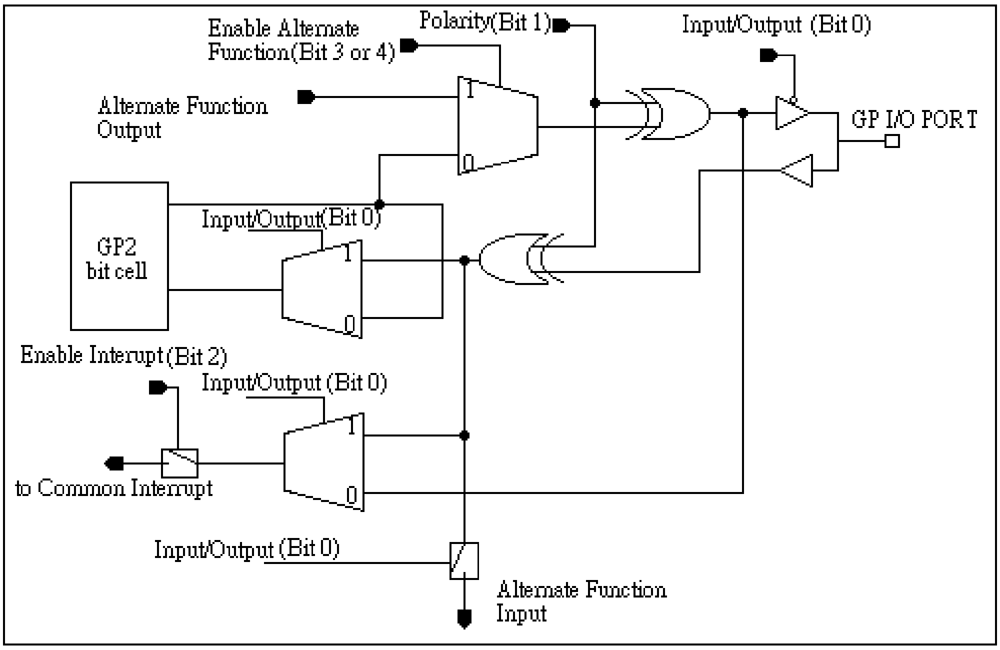

Enable Alternate
Function(Bit 3 or 4)
Polarity(Bit 1)
Input/Output (Bit 0)
Alternate Function
Output
1
0
GP I/O PORT
GP2
bit cell
Input/Output(Bit 0)
1
0
Enable Interupt(Bit 2)
Input/Output (Bit 0)
1
0
to Common Interrupt
Input/Output (Bit 0)
Alternate Function
Input

Figure 7.2

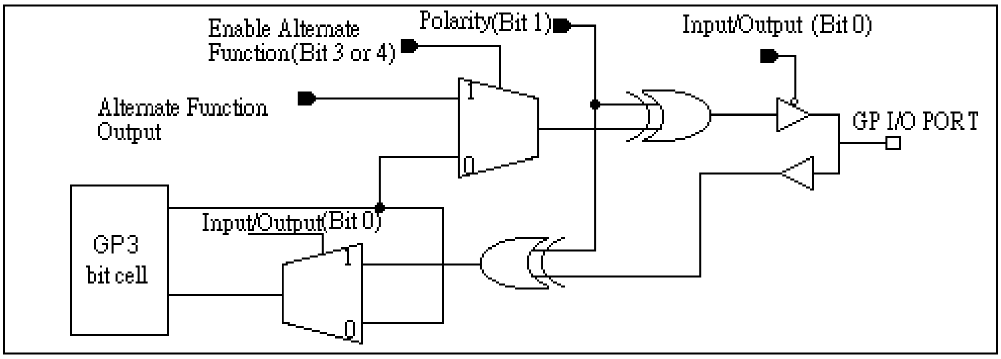

Enable Alternate
Function(Bit 3 or 4)
Polarity(Bit 1)
Input/Output (Bit 0)
Alternate Function
Output
1
0
GP I/O PORT
GP3
bit cell
Input/Output(Bit 0)
1
0

Figure 7.3

7.1 Basic I/O functions

The Basic I/O functions of W83977TF provide several I/O operations including driving a logic value to output port, latching a logic value from input port, inverting the input/output logic value, and steering Common Interrupt (only available in the second group of the GP I/O port). Common Interrupt is the ORed function of all interrupt channels in the second group of the GP I/O ports, and it also connects to a 1ms debounce filter which can reject a noise of 1 ms pulse width or less. There are three 8-bit registers (GP1, GP2, and GP3) which are directly connected to those GP I/O ports. Each GP I/O port is represented as a bit in one of three 8-bit registers. Only 6 bits of GP2 are implemented. Table 7.1.1 shows their combinations of Basic I/O functions, and Table 7.1.2 shows the register bit assignments of GP1, GP2, and GP3.

Table 7.1.1

I/O BIT 0 = OUTPUT 1 = INPUT	**ENABLE INT BIT 0 = DISABLE 1 = ENABLE**	**POLARITY BIT 0 = NON INVERT 1 = INVERT**	**BASIC I/O OPERATIONS**
0	0	0	Basic non-inverting output
0	0	1	Basic inverting output
0	1	0	Non-inverted output bit value of GP2 drive to Common Interrupt
0	1	1	Inverted output bit value of GP2 drive to Common Interrupt
1	0	0	Basic non-inverting input
1	0	1	Basic inverting input
1	1	0	Non-inverted input drive to Common Interrupt
1	1	1	Inverted input drive to Common Interrupt

Table 7.1.2

GP I/O PORT ACCESSED REGISTER	REGISTER BIT ASSIGNMENT	GP I/O PORT
GP1	BIT 0	GP10
	BIT 1	GP11
	BIT 2	GP12
	BIT 3	GP13
	BIT 4	GP14
	BIT 5	GP15
	BIT 6	GP16
	BIT 7	GP17
GP2	BIT 0	GP20
	BIT 1	GP21
	BIT 2	GP22
	BIT 3	GP23
	BIT 4	GP24
	BIT 5	GP25
	BIT 6	GP26
GP3	BIT 0	GP30
	BIT 1	GP31
	BIT 2	GP32
	BIT 3	GP33
	BIT 4	GP34
	BIT 5	GP35
	BIT 6	GP36
	BIT 7	GP37

7.2 Alternate I/O Functions

W83977TF provides several alternate functions which are scattered among the GP I/O ports. Table 7.2.1 shows their assignments. Polarity bit can also be set to alter their polarity.

Table 7.2.1

GP I/O PORT	ALTERNATE FUNCTION
GP10	Interrupt Steering
GP11	Interrupt Steering
GP12	Watch Dog Timer Output/IRRX input
GP13	Power LED output/IRTX output
GP14	General Purpose Address Decoder/Keyboard Inhibit(P17)
GP15	General Purpose Write Strobe/ 8042 P12
GP16	Watch Dog Timer Output
GP17	Power LED output
GP20	Keyboard Reset (8042 P20)
GP21	8042 P13
GP22	8042 P14
GP23	8042 P15
GP24	8042 P16
GP25	GATE A20 (8042 P21)
GP30	Interrupt Steering
GP31	Interrupt Steering
GP32	General Purpose Address Decoder
GP33	General Purpose Address Decoder
GP34	Watch Dog Timer Output

7.2.1 Interrupt Steering

GP10, GP11, GP30, and GP31 can be programmed to map their own interrupt channels. The selection of IRQ channel can be done in configuration registers CR70 and CR72 of logical device 7 and logical device 9. Each interrupt channel also has its own 1 ms debounce filter that is used to reject any noise whose width is equal to or less than 1 ms.

7.2.2 Watch Dog Timer Output

Watch Dog Timer contains a one minute resolution down counter, CRF2 of Logical Device 8, and two watch Dog control registers, WDT_CTRL0 and WDT_CTRL1 of Logical Device 8. The down counter can be programmed within the range from 1 to 255 minutes. Writing any new non-zero value to CRF2 or reset signal coming from a Mouse interrupt or Keyboard interrupt (CRF2 also contains non-zero value) will cause the Watch Dog Timer to reload and start to count down from the new value. As the counter reaches zero, (1) Watch Dog Timer time-out occurs and the bit 0 of WDT_CTRL1 will be set to logic 1; (2) Watch Dog interrupt output is asserted if the interrupt is enable in CR72 of logical device 8; and (3) Power LED starts to toggle output if the bit 3 of WDT_CTRL0 is enabled. WDT_CTRL1 also can be accessed through GP2 I/O base address + 1.

7.2.3 Power LED

The Power LED function provides 1 Hertz rate toggle pulse output with 50 percent duty cycle. Table 7.2.2 shows how to enable Power LED.

Table 7.2.2

WDT_CTRL1 BIT[1]	WDT_CTRL0 BIT[3]	WDT_CTRL1 BIT[0]	POWER LED STATE
1	X	X	1 Hertz Toggle pulse
0	0	X	Continuous high or low *
0	1	0	Continuous high or low *
0	1	1	1 Hertz Toggle pulse

* Note: Continuous high or low depends on the polarity bit of GP13 or GP17 configuration registers.

7.2.4 General Purpose Address Decoder

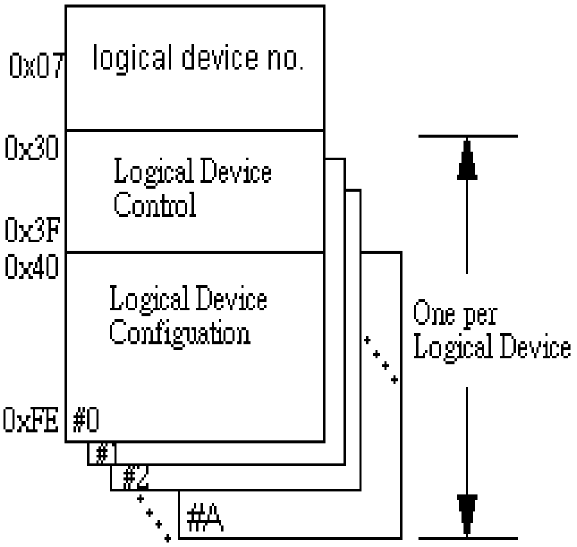
General Purpose Address Decoder provides two address decode as AEN equal to logic 0. The address base is stored at CR62, CR63 of logical device 7 for GP14 and at CR62-65 of logical device 9 for GP32 and GP33. The decoding output is normally active low. Users can alter its polarity through the polarity bit of the GP14, GP32, and GP33's configuration register.

7.2.5 General Purpose Write Strobe

General Purpose Write Strobe is an address decoder that performs like General Purpose Address Decoder, but it has to be qualified by $\overline{\text{IOW}}$ and AEN. Its output is normally active low. Users can alter its polarity through the polarity bit of the GP15's configuration register.

8. PLUG AND PLAY CONFIGURATION

The W83977TF uses Compatible PNP protocol to access configuration registers for setting up different types of configurations. In W83977TF, there are nine Logical Devices (from Logical Device 0 to Logical Device A with the exception of logical device 4 and 6 for compatibility) which correspond to nine individual functions: FDC (logical device 0), PRT (logical device 1), UART1 (logical device 2), UART2 (logical device 3), KBC (logical device 5), GPIO1 (logical device 7), GPIO2 (logical device 8), GPIO3 (logical device 9), and ACPI ((logical device A). Each Logical Device has its own configuration registers (above CR30). Host can access those registers by writing an appropriate logical device number into logical device select register at CR7.



8.1 Compatible PnP

8.1.1 Extended Function Registers

In Compatible PnP, there are two ways to enter Extended Function and read or write the configuration registers. HEFRAS (CR26 bit 6) can be used to select one out of these two methods of entering the Extended Function mode as follows:

HEFRAS	address and value
0	write 87h to the location 3F0h twice
1	write 87h to the location 370h twice

After Power-on reset, the value on $\overline{\text{RTSA}}$ (pin 43) is latched by HEFRAS of CR26. In Compatible PnP, a specific value (87h) must be written twice to the Extended Functions Enable Register (I/O port address 3F0h or 370h). Secondly, an index value (02h, 07h-FFh) must be written to the Extended Functions Index Register (I/O port address 3F0h or 370h same as Extended Functions Enable Register) to identify which configuration register is to be accessed. The designer can then access the desired configuration register through the Extended Functions Data Register (I/O port address 3F1h or 371h).

After programming of the configuration register is finished, an additional value (AAh) should be written to EFERs to exit the Extended Function mode to prevent unintentional access to those configuration registers. The designer can also set bit 5 of CR26 (LOCKREG) to high to protect the configuration registers against accidental accesses.

The configuration registers can be reset to their default or hardware settings only by a cold reset (pin MR = 1). A warm reset will not affect the configuration registers.

8.1.2 Extended Functions Enable Registers (EFERs)

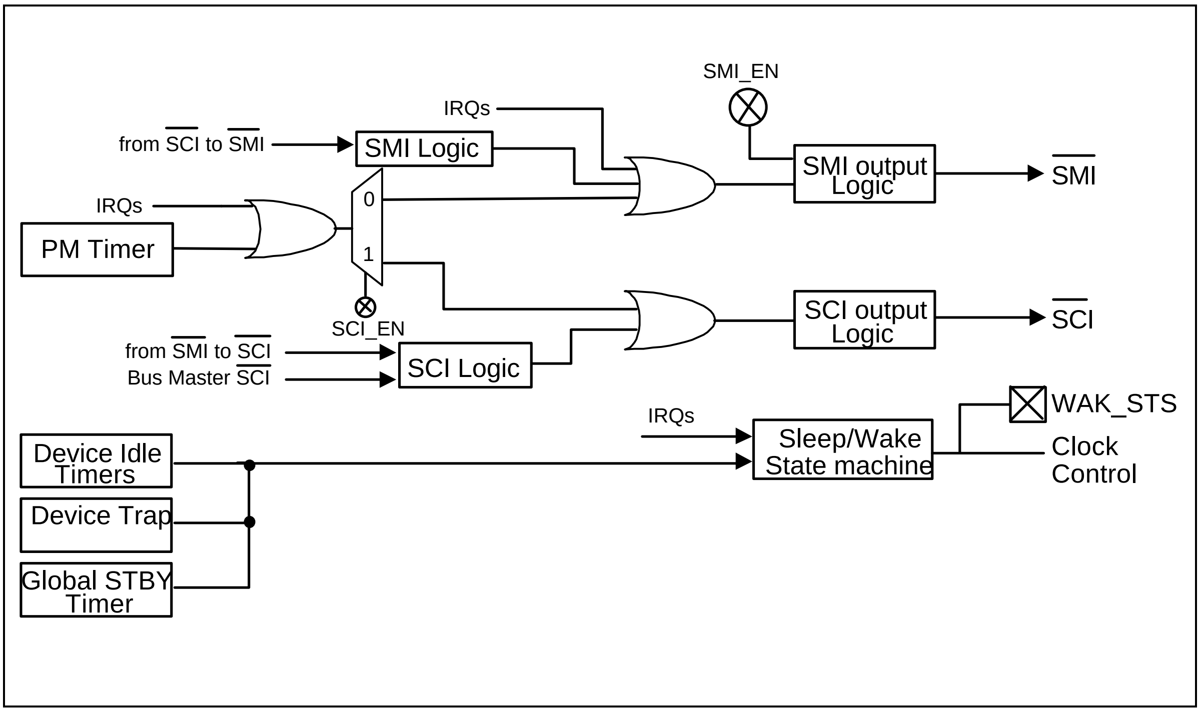
After a power-on reset, the W83977TF enters the default operating mode. Before the W83977TF enters the extended function mode, a specific value must be programmed into the Extended Function Enable Register (EFER) so that the extended function register can be accessed. The Extended Function Enable Registers are write-only registers. On a PC/AT system, their port addresses are 3F0h or 370h (as described in previous section).

8.1.3 Extended Function Index Registers (EFIRs), Extended Function Data Registers(EFDRs)

After the extended function mode is entered, the Extended Function Index Register (EFIR) must be loaded with an index value (02h, 07h-FEh) to access Configuration Register 0 (CR0), Configuration Register 7 (CR07) to Configuration Register FE (CRFE), and so forth through the Extended Function Data Register (EFDR). The EFIRs are write-only registers with port address 3F0h or 370h (as described in section 8.1.1) on PC/AT systems; the EFDRs are read/write registers with port address 3F1h or 371h (as described in section 8.1.1) on PC/AT systems.

9. ACPI REGISTERS FEATURES

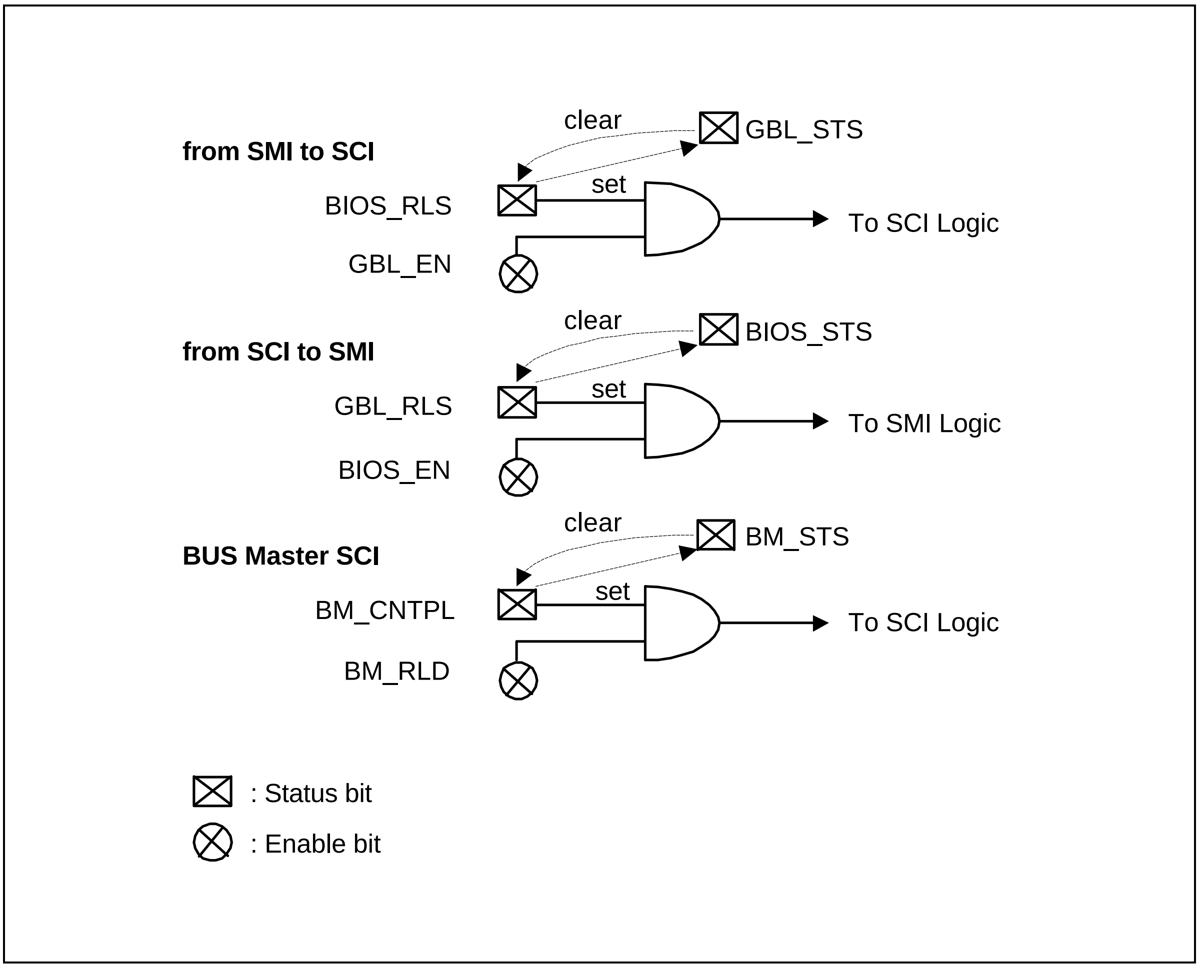
W83977TF supports both ACPI and legacy power managements. The switch logic of the power managment block generates an SMI interrupt in the legacy mode and an SCI interrupt in the ACPI mode. For the legacy mode, the SMI_EN bit is used. If it is set, it routes the power management events to the SMI interrupt logic. For the ACPI mode, the SCI_EN bit is used. If it is set, it route the power management events to the SCI interrupt logic. The SMI_EN bit is located in the configuration register block of Device A and the SCI_EN bit is located in the PM1 register block. See the following figure for illustration.


SMI_EN
IRQs
from SCI to SMI
SMI Logic
SMI output Logic
SMI
IRQs
PM Timer
0
1
SCI_EN
SCI output Logic
SCI
from SMI to SCI
Bus Master SCI
SCI Logic
IRQs
Sleep/Wake State machine
WAK_STS
Clock Control
Device Idle Timers
Device Trap
Global STBY Timer

The SMI interrupt is routed to pin SMI, which is dedicated for the SMI interrupt output. Another way to output the SMI interrupt is to route to pin IRQSER, which is the signal pin in the Serial IRQ mode. The SCI interrupt can be routed to pin SCI, which is dedicated for the SCI function. Or it can be routed to one interrupt request pin, which is selected through CR70.bit3 - 0 of logical device 9. Another way is to output the SCI interrupt to pin IRQSER if serial IRQ mode is enabled.

9.1 SMI to SCI/SCI to SMI and Bus Master

The following figure illustrates the process of generating an interrupt from $\overline{\mathrm{SMI}}$ to $\overline{\mathrm{SCI}}$ or from $\overline{\mathrm{SCI}}$ to $\overline{\mathrm{SMI}}$.


clear
GBL_STS
from SMI to SCI
set
BIOS_RLS
To SCI Logic
GBL_EN
clear
BIOS_STS
from SCI to SMI
set
GBL_RLS
To SMI Logic
BIOS_EN
clear
BM_STS
BUS Master SCI
set
BM_CNTPL
To SCI Logic
BM_RLD
: Status bit
: Enable bit

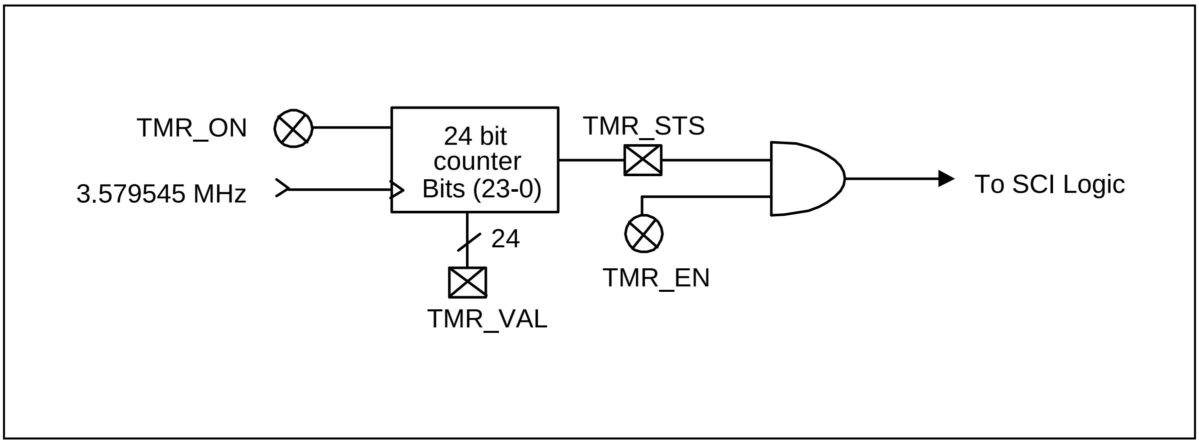
For the BIOS software to raise an event to the ACPI software, BIOS_RLS, GBL_EN, and GBL_STS bits are involved. GBL_EN is the enable bit and the GBL_STS is the status bit. Both are controlled by the ACPI software. If BIOS_RLS is set by the BIOS software and GBL_EN is set by the ACPI software, an $\overline{\mathrm{SCI}}$ interrupt is raised. Writing a 1 to BIOS_RLS sets it to logic 1 and also sets GBL_STS to logic 1. Writing a 0 to BIOS_RLS has no effect. Wrinting a 1 to GBL_STS clears it to logic 0 and also clears BIOS_RLS to logic 0. Writing a 0 to GBL_STS has no effect.

For the ACPI software to raise an event to the BIOS software, GBL_RLS, BIOS_EN, and BIOS_STS bits are involved. BIOS_EN is the enable bit and the BIOS_STS is the status bit. Both are controlled by the BIOS software. If GBL_RLS is set by the ACPI software and BIOS_EN is set by the BIOS software, an $\overline{\text{SMI}}$ is raised. Writing a 1 to GBL_RLS sets it to logic 1 and also sets BIOS_STS to logic 1. Writing a 0 to GBL_RLS has no effect. Wrinting a 1 to BIOS_STS clears it to logic 0 and also clears GBL_RLS to logic 0. Writing a 0 to BIOS_STS has no effect.

For the bus master to raise an event to the ACPI software, BM_CNTRL, BM_RLD, and BM_STS bits are involved. Both BM_RLD and BM_STS are controlled by the ACPI software. If BM_CNTRL is set by the BIOS software and BM_RLD is set by the ACPI software, an $\overline{\text{SCI}}$ interrupt is raised. Writing a 1 to BM_CNTRL sets it to logic 1 and also sets BM_STS to logic 1. Writing a 0 to BM_CNTRL has no effect. Wrinting a 1 to BM_STS clears it to logic 0 and also clears BM_CNTRL to logic 0. Writing a 0 to BM_STS has no effect.

9.2 Power Management Timer

In the ACPI specification, it requires a power management timer. The power management timer is a 24-bit fixed rate free running up-count timer that runs off a 3.579545MHZ clock. The power management timer corresponds to status bit (TMR_STS) and enable bit (TMR_EN). The TMR_STS bit is set any time the last bit of the timer (bit 23) goes from 0 to 1 or from 1 to 0. If the TMR_EN bit is set, the setting of the TMR_STS bit will generate an $\overline{\text{SCI}}$ interrupt. Three registers are used to read the timer value which are located in the PM1 register block. The power management timer has one enabel bit (TMR_ON) to turn ii on or off. The TMR_ON is located in GPE register block. If it is cleared to 0, the power management timer function would not work. There are no timer reset requirements, except that the timer should function after power-up. See the following figure for illustration.



9.3 ACPI Registers (ACPIRs)

The ACPI register model consists of the fixed register blocks that perform the ACPI functuions. A register block may be a event register block which deals with ACPI events or a control register block which deals with control features. The order in the event register block is a status register followed by an enable register.

Each event register, if implemented, contains two two register: a status register and an enable register, of 16 bits wide each. The status register indicates which event triggers the ACPI System Control Interrupt ($\overline{\text{SCI}}$). When the hardware event occurs, the corresponding status bit will be set. However, the corresponding enable bit is also required to be set before an $\overline{\text{SCI}}$ interrupt could be raised. If the enable bit is not set, the software can examine the state of the hardware event by reading the status bit without generating an $\overline{\text{SCI}}$ interrupt.

Any status bit, unless otherwise noted, can only be set by specific hardware event. It is cleared by writing a 1 to its bit position and writing a 0 has no effect. Except some special status bits, every status bit has the corresponding enable bit on the same bit position in the enable register. Those status bits which have no corresponding enable bit are read for special purpose. Reverved or unimplemented enable bits always return zero, and writing to these bits should has no effect.

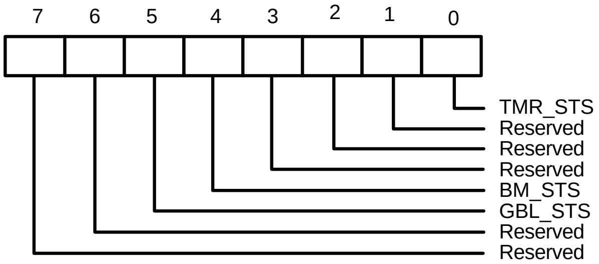
The control bit in the control register provides some special control function over the hardware event, or some special control over $\overline{\text{SCI}}$ event. Reserved or unimplemented control bits always return zero, and writing to those bits should has no effect.

Table 9-1 (sec. 9.3.21) lists the PM1 register block and its registers. The base address of PM1 register block is named as PM1a_EVT_BLK in the ACPI specification and is specified in CR60, 61 of logical device A.

Table 9-2 (sec. 9.3.21) lists the GPE register block and its registers. The base address of general-purpose event block GPE0 is named as GPE0_BLK in the ACPI specification and is specified in CR62, 63 of logical device A. The base address of general-purpose event block GPE1 is named as GPE1_BLK in the ACPI specification and is specified in CR64, 65 of logical device A.

9.3.1 Power Management 1 Status Register 1 (PM1STS1)

Register Location:	<CR60, 61> System I/O Space
Default Value:	00h
Attribute:	Read/write
Size:	8 bits



Bit	Name	Description
0	TMR_STS	This bit is the timer carry status bit. This bit is set anytime the bit 23 of the 24-bit counter changes (whenever the MSB changes from low to high or high to low). When TMR_EN and TMR_STS are set, a power magement event is raised. This bit is only set by hardware and can only be cleared by writing a 1 to this bit position. Writing a 0 has no effect.
1-3	Reserved	Reserved.
4	BM_STS	This is the bus master status bit. Writing a 1 to BM_CNTRL also sets BM_STS. Writing a 1 clears this bit and also clears BM_CNTRL. Writing a 0 has no effect.
5	GBL_STS	This is the global status bit. This bit is set when the BIOS wants the attention of the $\overline{\mathrm{SCI}}$ handler. BIOS sets this bit by setting BIOS_RLS and can only be cleared by writing a 1 to this bit position. Writing a 1 to this bit position also clears BIOS_RLS. Writing a 0 has no effect.
6-7	Reserved	Reserved. These bits always return zeros.

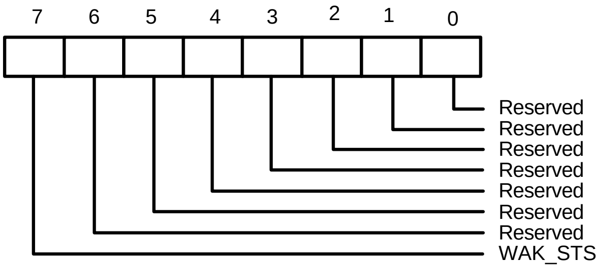
9.3.2 Power Management 1 Status Register 2 (PM1STS2)

Register Location: <CR60, 61> + 1H System I/O Space

Default Value: 00h

Attribute: Read/write

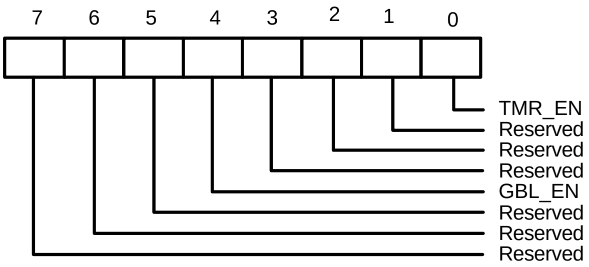
Size: 8 bits



Bit	Name	Description
0-6	Reserved	Reserved.
7	WAK_STS	This bit is set when the system is in the sleeping state and an enabled resume event occurs. Upon setting this bit, the sleeping/working state machine will transition the system to the working state. This bit is only set by hardware and is cleared by writing a 1 to this bit position or by the sleeping/working state machine automatically when the global standby timer expires. Writing a 0 has no effect. When the WAK_STS is cleared and all devices are in sleeping state, the whole chip enters the sleeping state.

9.3.3 Power Management 1 Enable Register 1(PM1EN1)

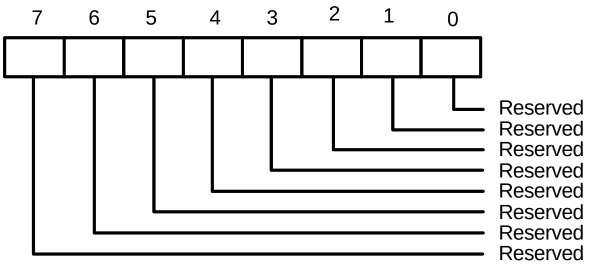
Register Location: <CR60, 61> + 2H System I/O Space
Default Value: 00h
Attribute: Read/write
Size: 8 bits


7
6
5
4
3
2
1
0
TMR_EN
Reserved
Reserved
Reserved
GBL_EN
Reserved
Reserved
Reserved

Bit	Name	Description
0	TMR_EN	This is the timer carry interrupt enable bit. When this bit is set then an $\overline{\text{SCI}}$ event is generated whenever the TMR_STS bit is set. When this bit is reset then no interrupt is generated even when the TMR_STS bit is set.
1-4	Reserved	Reserved. These bits always return a value of zero.
5	GBL_EN	The global enable bit. When both the GBL_EN bit and the GBL_STS bit are set, an $\overline{\text{SCI}}$ interrupt is raised.
6-7	Reserved	Reserved.

9.3.4 Power Management 1 Enable Register 2 (PM1EN2)

Register Location: <CR60, 61> + 3H System I/O Space
Default Value: 00h
Attribute: Read/write
Size: 8 bits


7
6
5
4
3
2
1
0
Reserved
Reserved
Reserved
Reserved
Reserved
Reserved
Reserved
Reserved

Bit	Name	Description
0-7	Reserved	Reserved. These bits always return zeros.

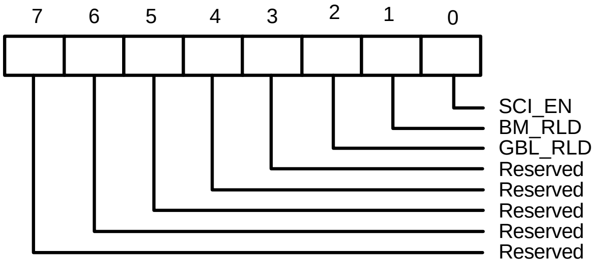
9.3.5 Power Management 1 Control Register 1 (PM1CTL1)

Register Location: <CR60, 61> + 4H System I/O Space

Default Value: 00h

Attribute: Read/write

Size: 8 bits


7
6
5
4
3
2
1
0
SCI_EN
BM_RLD
GBL_RLD
Reserved
Reserved
Reserved
Reserved
Reserved

Bit	Name	Description
0	SCI_EN	Select whether the power management event triggers an $\overline{\text{SCI}}$ or an $\overline{\text{SMI}}$ interrupt. When this bit is set, then the power management events will generate an $\overline{\text{SCI}}$ interrupt. When this bit is reset and SMI_EN bit is set, then the power management events will generate an $\overline{\text{SMI}}$ interrupt.
1	BM_RLD	This is the bus master reload enable bit. If this bit is set and BM_CNTRL is set, an $\overline{\text{SCI}}$ interrupt is raised.
2	GBL_RLS	The global release bit. This bit is used by the ACPI software to raise an event to the BIOS software. The BIOS software has a corresponding enable and status bit to control its ability to receive the ACPI event. Setting GBL_RLS sets BIOS_STS, and it generates an $\overline{\text{SMI}}$ interrupt if BIOS_EN is also set.
3-7	Reserved	Reserved. These bits always return zeros.

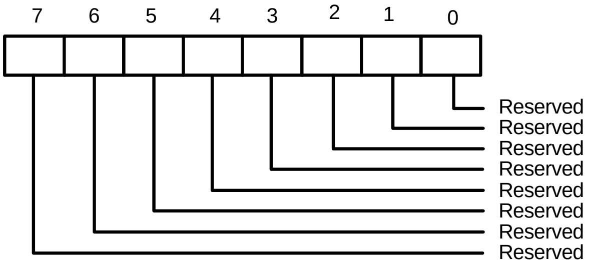
9.3.6 Power Management 1 Control Register 2 (PM1CTL2)

Register Location: <CR60, 61> + 5H System I/O Space

Default Value: 00h

Attribute: Read/write

Size: 8 bits


7
6
5
4
3
2
1
0
Reserved
Reserved
Reserved
Reserved
Reserved
Reserved
Reserved
Reserved

Bit	Name	Description
0-7	Reserved	Reserved. These bits always return zeros.

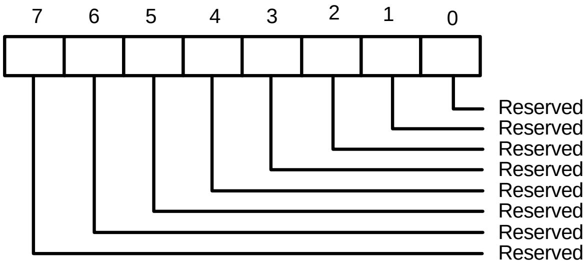
9.3.7 Power Management 1 Control Register 3 (PM1CTL3)

Register Location: <CR60, 61> + 6H System I/O Space

Default Value: 00h

Attribute: Read/write

Size: 8 bits


7
6
5
4
3
2
1
0
Reserved
Reserved
Reserved
Reserved
Reserved
Reserved
Reserved
Reserved

Bit	Name	Description
0-7	Reserved	Reserved. These bits always return zeros.

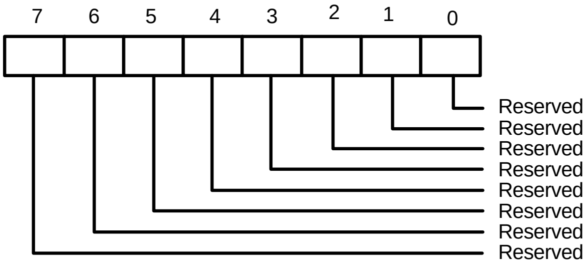
9.3.8 Power Management 1 Control Register 4 (PM1CTL4)

Register Location: <CR60, 61> + 7H System I/O Space

Default Value: 00h

Attribute: Read/write

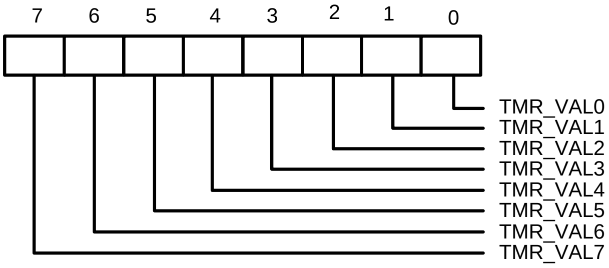
Size: 8 bits


7
6
5
4
3
2
1
0
Reserved
Reserved
Reserved
Reserved
Reserved
Reserved
Reserved
Reserved

Bit	Name	Description
0-7	Reserved	Reserved. These bits always return zeros.

9.3.9 Power Management 1 Timer 1 (PM1TMR1)

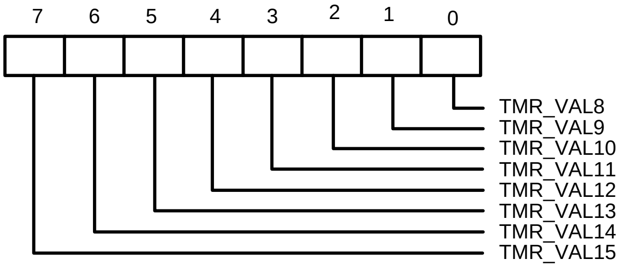
Register Location:	<CR60, 61> + 8H System I/O Space
Default Value:	00h
Attribute:	Read only
Size:	8 bits


7
6
5
4
3
2
1
0
TMR_VAL0
TMR_VAL1
TMR_VAL2
TMR_VAL3
TMR_VAL4
TMR_VAL5
TMR_VAL6
TMR_VAL7

Bit	Name	Description
0-7	TMR_VAL	This read-only field returns the running count of the power management timer. This is a 24-bit counter that runs off of a 3.579545 MHZ clock, and counts in the working state. The timer is reset and then continues counting until the CLKIN input the the chip is stopped. If the clock is restarted without a MR reset, then the counter will resume counting from where it stopped. The TMR_STS bit is set any time the last bit of the timer (bit 23) goes from 0 to 1 or from 1 to 0. If the TMR_EN bit is set, the setting of the TMR_STS bit will generate an $\overline{\text{SCI}}$ interrupt.

9.3.10 Power Management 1 Timer 2 (PM1TMR2)

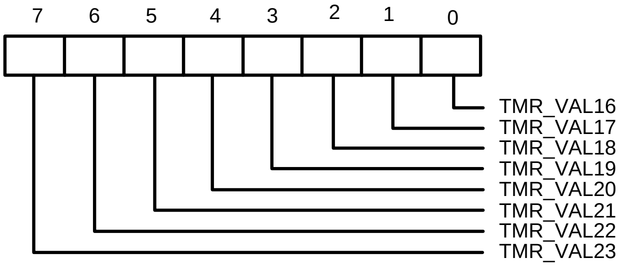
Register Location:	<CR60, 61> + 9H System I/O Space
Default Value:	00h
Attribute:	Read only
Size:	8 bits


7
6
5
4
3
2
1
0
TMR_VAL8
TMR_VAL9
TMR_VAL10
TMR_VAL11
TMR_VAL12
TMR_VAL13
TMR_VAL14
TMR_VAL15

Bit	Name	Description
0-7	TMR_VAL	This read-only field returns the running count of the power management timer. This is a 24-bit counter that runs off of a 3.579545 MHZ clock, and counts in the working state. The timer is reset and then continues counting until the CLKIN input the the chip is stopped. If the clock is restarted without a MR reset, then the counter will resume counting from where it stopped. The TMR_STS bit is set any time the last bit of the timer (bit 23) goes from 0 to 1 or from 1 to 0. If the TMR_EN bit is set, the setting of the TMR_STS bit will generate an $\overline{\text{SCI}}$ interrupt.

9.3.11 Power Management 1 Timer 3 (PM1TMR3)

Register Location:	<CR60, 61> + AH System I/O Space
Default Value:	00h
Attribute:	Read only
Size:	8 bits



Bit	Name	Description
0-7	TMR_VAL	This read-only field returns the running count of the power management timer. This is a 24-bit counter that runs off of a 3.579545 MHZ clock, and counts in the working state. The timer is reset and then continues counting until the CLKIN input the the chip is stopped. If the clock is restarted without a MR reset, then the counter will resume counting from where it stopped. The TMR_STS bit is set any time the last bit of the timer (bit 23) goes from 0 to 1 or from 1 to 0. If the TMR_EN bit is set, the setting of the TMR_STS bit will generate an $\overline{\text{SCI}}$ interrupt.

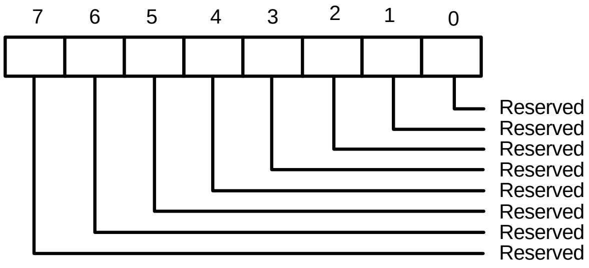
9.3.12 Power Management 1 Timer 4 (PM1TMR4)

Register Location: <CR60, 61> + BH System I/O Space

Default Value: 00h

Attribute: Read only

Size: 8 bits


7
6
5
4
3
2
1
0
Reserved
Reserved
Reserved
Reserved
Reserved
Reserved
Reserved
Reserved

Bit	Name	Description
0-7	Reserved	Reserved. These bits always return zeros.

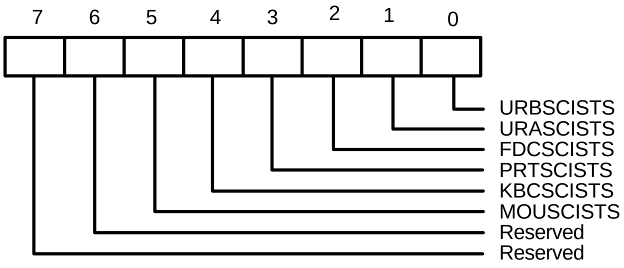
9.3.13 General Purpose Event 0 Status Register 1 (GP0STS1)

Register Location: <CR62, 63> System I/O Space

Default Value: 00h

Attribute: Read/write

Size: 8 bits

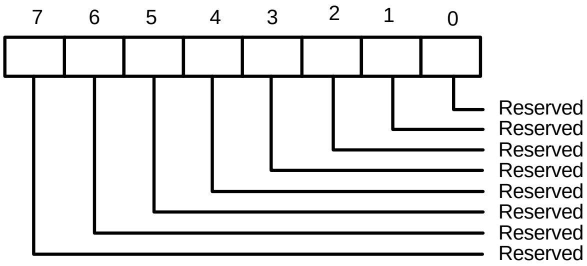

7
6
5
4
3
2
1
0
URBSCISTS
URASCISTS
FDCSCISTS
PRTSCISTS
KBCSCISTS
MOUSCISTS
Reserved
Reserved

These bits indicate the status of the $\overline{\text{SCI}}$ input, which is set when the device's IRQ is raised. If the corresponding enable bit in the $\overline{\text{SCI}}$ interrupt enable register (in GP0EN1) is set, an $\overline{\text{SCI}}$ interrupt is raised and routed to the output pin. Wrinting a 1 clears the bit, and wrinting a 0 has no effect. If the bit is not cleared, new IRQ to the $\overline{\text{SCI}}$ logic input is ignored and no $\overline{\text{SCI}}$ interrupt will be raised.

Bit	Name	Description
0	URBSCISTS	UART B $\overline{\text{SCI}}$ status, which is set by the UART B IRQ.
1	URASCISTS	UART A $\overline{\text{SCI}}$ status, which is set by the UART A IRQ.
2	FDCSCISTS	FDC $\overline{\text{SCI}}$ status, which is set by the FDC IRQ.
3	PRTSCISTS	PRT $\overline{\text{SCI}}$ status, which is set by the printer port IRQ.
4	KBCSCISTS	KBC $\overline{\text{SCI}}$ status, which is set by the KBC IRQ.
5	MOUSCISTS	MOUSE $\overline{\text{SCI}}$ status, which is set by the MOUSE IRQ.
6-7	Reserved	Reserved.

9.3.14 General Purpose Event 0 Status Register 2 (GP0STS2)

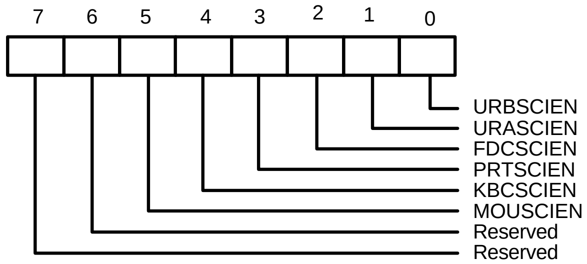
Register Location:	<CR62, 63> + 1H System I/O Space
Default Value:	00h
Attribute:	Read/write
Size:	8 bits



Bit	Name	Description
0-7	Reserved	Reserved. These bits always return zeros.

9.3.15 General Purpose Event 0 Enable Register 1 (GP0EN1)

Register Location: <CR62, 63> + 2H System I/O Space
Default Value: 00h
Attribute: Read/write
Size: 8 bits



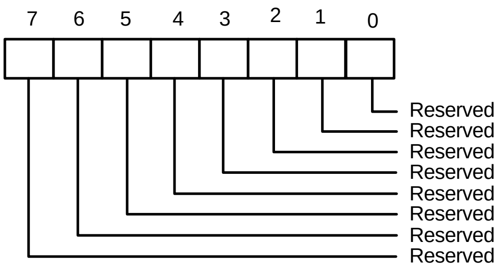
These bits are used to enable the device's IRQ sources into the $\overline{\text{SCI}}$ logic. The $\overline{\text{SCI}}$ logic output for the IRQs is as follows:

SCI logic output = (URBSCIEN and URBSCISTS) or (URASCIEN and URASCISTS) or (FDCSCIEN and FDCSCISTS) or (PRTSCIEN and PRTSCISTS) or (KBCSCIEN and KBCSCISTS) or (MOUSCIEN and MOUSCISTS)

Bit	Name	Description
0	URBSCIEN	UART B $\overline{\text{SCI}}$ enable, which controls the UART B IRQ.
1	URASCIEN	UART A $\overline{\text{SCI}}$ enable, which controls the UART A IRQ.
2	FDCSCIEN	FDC $\overline{\text{SCI}}$ enable, which controls the FDC IRQ.
3	PRTSCIEN	printer port $\overline{\text{SCI}}$ enable, which controls the printer port IRQ.
4	KBCSCIEN	KBC $\overline{\text{SCI}}$ enable, which controls the KBC IRQ.
5	MOUSCIEN	MOUSE $\overline{\text{SCI}}$ enable, which controls the MOUSE IRQ.
6-7	Reserved	Reserved.

9.3.16 General Purpose Event 0 Enable Register 2 (GP0EN2)

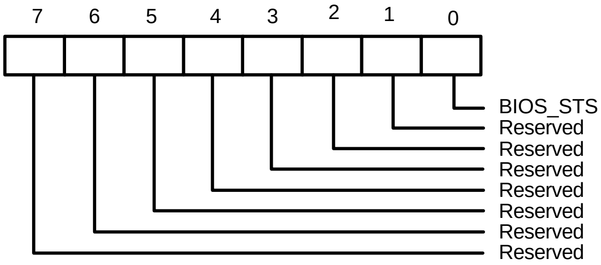
Register Location: <CR62, 63> + 3H System I/O Space
Default Value: 00h
Attribute: Read/write
Size: 8 bits


7
6
5
4
3
2
1
0
Reserved
Reserved
Reserved
Reserved
Reserved
Reserved
Reserved
Reserved

Bit	Name	Description
0-7	Reserved	Reserved. These bits always return zeros.

9.3.17 General Purpose Event 1 Status Register 1 (GP1STS1)

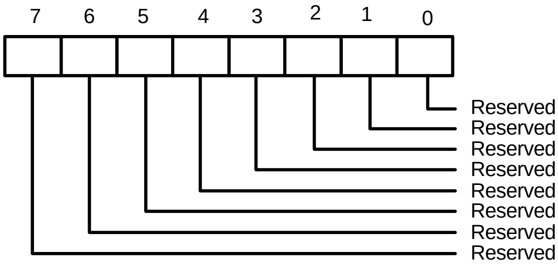
Register Location: <CR64, 65> System I/O Space
Default Value: 00h
Attribute: Read/write
Size: 8 bits


7
6
5
4
3
2
1
0
BIOS_STS
Reserved
Reserved
Reserved
Reserved
Reserved
Reserved
Reserved

Bit	Name	Description
0	BIOS_STS	The BIOS status bit. This bit is set when GBL_RLS is set. If BIOS_EN is set, setting GBL_RLS will raise an $\overline{\text{SMI}}$ event. Writing a 1 to its bit location clears BIOS_STS and also clears GBL_RLS. Writing a 0 has no effect.
1-7	Reserved	Reserved.

9.3.18 General Purpose Event 1 Status Register 2 (GP1STS2)

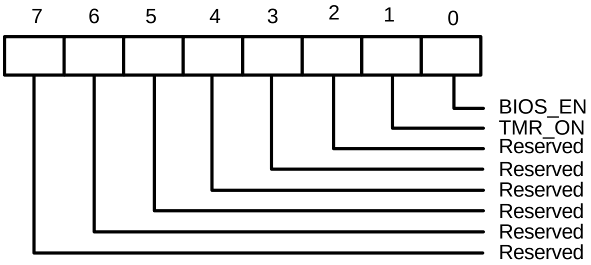
Register Location: <CR64, 65> + 1H System I/O Space
Default Value: 00h
Attribute: Read/write
Size: 8 bits


7
6
5
4
3
2
1
0
Reserved
Reserved
Reserved
Reserved
Reserved
Reserved
Reserved
Reserved

Bit	Name	Description
0-7	Reserved	Reserved. These bits always return zeros.

9.3.19 General Purpose Event 1 Enable Register 1 (GP1EN1)

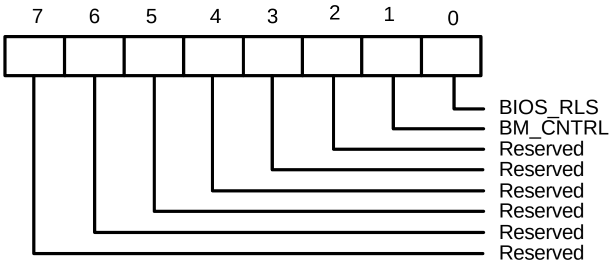
Register Location: <CR64, 65> + 2H System I/O Space
Default Value: 00h
Attribute: Read/write
Size: 8 bits


7
6
5
4
3
2
1
0
BIOS_EN
TMR_ON
Reserved
Reserved
Reserved
Reserved
Reserved
Reserved

Bit	Name	Description
0	BIOS_EN	This bit is raise the $\overline{SMI}$ event. When this bit is set and the ACPI software writes a 1 to the GBL_RLS bit, an $\overline{SMI}$ event is raised on the $\overline{SMI}$ logic output.
1	TMR_ON	This bit is used to turn on the power management timer. 1 = timer on; 0 = timer off.
2-7	Reserved	Reserved.

9.3.20 General Purpose Event 1 Enable Register 2 (GP1EN2)

Register Location: <CR64, 65> + 3H System I/O Space
Default Value: 00h
Attribute: Read/write
Size: 8 bits



Bit	Name	Description
0	BIOS_RLS	The BIOS release bit. This bit is used by the BIOS software to raise an event to the ACPI software. The ACPI software has a corresponding enable and status bit to control its ability to receive the ACPI event. Setting BIOS_RLS sets GBL_STS, and it generates an $\overline{\text{SCI}}$ interrupt if GBL_EN is also set. Writing a 1 to its bit position sets this bit and also sets the BM_STS bit. Writing a 0 has no effect. This bit is cleared by writing a 1 to the GBL_STS bit.
1	BM_CNTRL	This bit is used to set the BM_STS bit and if the BM_RLD bit is also set, then an SCI interrupt is generated. Writing a 1 sets BM_CNTRL to 1 and also sets BM_STS. Writing a 0 has no effect. Wrinting a 1 to BM_STS clears BM_STS and also clears BM_CNTRL.
2-7	Reserved	Reserved.

9.3.21 Bit Map Configuration Registers

Table 9-1: Bit Map of PM1 Register Block

Register	Address	Power-On Reset Value	D7	D6	D5	D4	D3	D2	D1	D0
PM1STS1	<CR60,61>	0000 0000	0	0	GBL_STS	BM_STS	0	0	0	TMR_STS
PM1STS2	<CR60,61> +1H	0000 0000	WAK_STS	0	0	0	0	0	0	0
PM1EN1	<CR60,61> +2H	0000 0000	0	0	GBL_EN	0	0	0	0	TMR_EN
PM1EN2	<CR60,61> +3H	0000 0000	0	0	0	0	0	0	0	0
PM1CTL1	<CR60,61> +4H	0000 0000	0	0	0	0	0	GBL_RLS	BM_RLD	SCI_EN
PM1CTL2	<CR60,61> +5H	0000 0000	0	0	0	0	0	0	0	0
PM1CTL3	<CR60,61> +6H	0000 0000	0	0	0	0	0	0	0	0
PM1CTL4	<CR60,61> +7H	0000 0000	0	0	0	0	0	0	0	0
PM1TMR1	<CR60,61> +8H	0000 0000	TMR_VAL7	TMR_VAL6	TMR_VAL5	TMR_VAL4	TMR_VAL3	TMR_VAL2	TMR_VAL1	TMR_VAL0
PM1TMR2	<CR60,61> +9H	0000 0000	TMR_VAL15	TMR_VAL14	TMR_VAL13	TMR_VAL12	TMR_VAL11	TMR_VAL10	TMR_VAL9	TMR_VAL8
PM1TMR3	<CR60,61> +AH	0000 0000	TMR_VAL23	TMR_VAL22	TMR_VAL21	TMR_VAL20	TMR_VAL19	TMR_VAL18	TMR_VAL17	TMR_VAL16
PM1TMR4	<CR60,61> +BH	0000 0000	0	0	0	0	0		0	0

Table 9-2: Bit Map of GPE Register Block

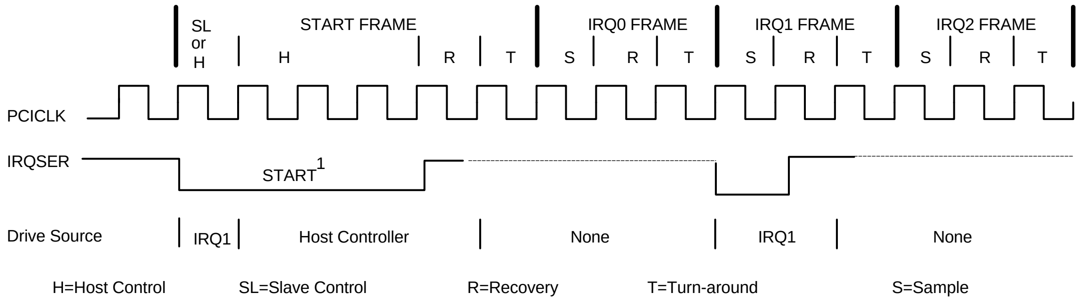
Register	Address	Power-On Reset Value	D7	D6	D5	D4	D3	D2	D1	D0
GP0STS1	<CR62,63>	0000 0000	0	0	MOUSCISTS	KBCSCISTS	PRTSCISTS	FDCSCISTS	URASCISTS	URBSCISTS
GP0STS2	<CR62,63> +1H	0000 0000	0	0	0	0	0	0	0	0
GP0EN1	<CR62,63> +2H	0000 0000	0	0	MOUSCIEN	KBCSCIEN	PRTSCIEN	FDCSCIEN	URASCIEN	URBSCIEN
GP0EN2	<CR62,63> +3H	0000 0000	0	0	0	0	0	0	0	0
GP1STS1	<CR64,65>	0000 0000	0	0	0	0	0	0	0	BIOS_STS
GP1STS2	<CR64,65> +1H	0000 0000	0	0	0	0	0	0	0	0
GP1EN1	<CR64,65> +2H	0000 0000	0	0	0	0	0	0	TMR_ON	BIOS_EN
GP1EN2	<CR64,65> +3H	0000 0000	0	0	0	0	0	0	BM_CNTRL	BIOS_RLS

10. SERIAL IRQ

W83977TF supports a serial IRQ scheme. This allow a signal line to be used to report the legacy ISA interrupt rerquests. Because more than one device may need to share the signal serial IRQ signal line, an open drain signal scheme is used. The clock source is the PCI clock. The serial interrupt is transfered on the IRQSER signal, one cycle consisting of three frames types: a start frame, several IRQ/Data frame, and one Stop frame. The serial interrupt scheme adheres to the *Serial IRQ Specification for PCI System, Version 6.0.*

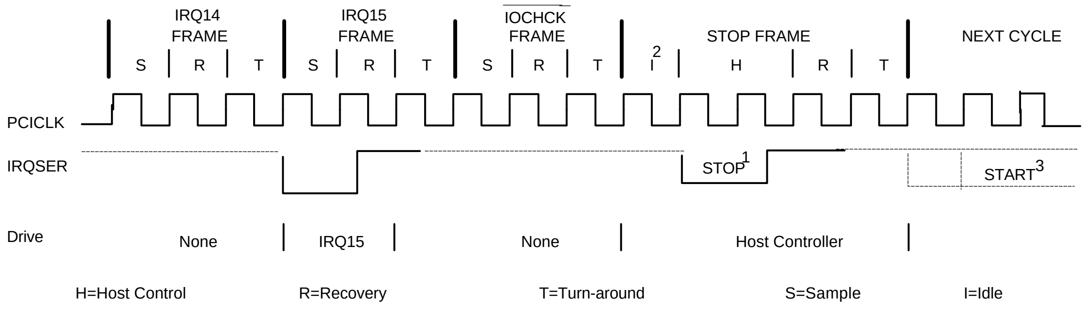
Timing Diagrams For IRQSER Cycle

Start Frame timing with source sampled a low pulse on IRQ1


SL or H
START FRAME
H
R
T
IRQ0 FRAME
S
R
T
IRQ1 FRAME
S
R
T
IRQ2 FRAME
S
R
T
PCICLK
IRQSER
START1
Drive Source
IRQ1
Host Controller
None
IRQ1
None
H=Host Control
SL=Slave Control
R=Recovery
T=Turn-around
S=Sample

1. Start Frame pulse can be 4-8 clocks wide.

Stop Frame Timing with Host using 17 IRQSER sampling period



1. Stop pulse is 2 clocks wide for Quiet mode, 3 clocks wide for Continuous mode.
2. There may be none, one or more Idle states during the Stop Frame.
3. The next IRQSER cycle's Start Frame pulse may or may not start immediately after the turn-around clock of the Stip Frame.

10.1 Start Frame

There are two modes of operation for the IRQSER Start frame: Quiet mode and Continuous mode.

In the Quiet mode, the peripheral drives the SERIRQ signal active low for one clock, and then tri-states it. This brings all the states machines of the peripherals from idle to active states. The host controller will then take over driving IRQSER signal low in the next clock and will continue driving the IRQSER low for programmable 3 to 7 clock periods. This makes the total number of clocks low for 4 to 8 clock periods. After these clocks, the host controller will drive the IRQSER high for one clock and then tri-states it.

In the Continuous mode, only the host controller initiates the START frame to update IRQ/Data line information. The host controller drives the IRQSER signal low for 4 to 8 clock periods. Upon a reset, the IRQSER signal is defaulted to the Continuous mode for the host controller to initiate the first Start frame.

10.2 IRQ/Data Frame

Once the start frame has been initiated, all the peripherals must start counting frames based on the rsing edge of the start pulse. Each IRQ/Data Frame is three clocks: Sample phase, Recovery phase, and Turn-around phase.

During the Sample phase, the peripheral drives SERIRQ low if the corresponding IRQ is active. If the corresponding IRQ is inactive, then IRQSER must be left tri-stated. During the Recovery phase, the peripheral device drives the IRQSER high. During the Turn-around phase, the peripheral device left the IRQSER tri-stated.

The IRQ/Data Frame has a number of specific order, as shown in Table 10-1.

10.3 Stop Frame

After all IRQ/Data Frames have completed, the host controller will terminate IRQSER by a Stop frame. Only the host controller can initiate the Stop frame by driving IRQSER low for 2 or 3 clocks. If the Stop Frame is low for 2 clocks, the next IRQSER cycle's Sample mode is the Quiet mode. If the Stop Frame is low for 3 clocks, the next IRQSER cycle's Sample mode is the Continuous mode.

Table 10-1 IRQSER Sampling periods

IRQ/Data Frame	Signal Sampled	# of clocks past Start
1	IRQ0	2
2	IRQ1	5
3	$\overline{\text{SMI}}$	8
4	IRQ3	11
5	IRQ4	14
6	IRQ5	17
7	IRQ6	20
8	IRQ7	23
9	IRQ8	26
10	IRQ9	29
11	IRQ10	32
12	IRQ11	35
13	IRQ12	38
14	IRQ13	41
15	IRQ14	44
16	IRQ15	47
17	$\overline{\text{IOCHCK}}$	50
18	$\overline{\text{INTA}}$	53
19	$\overline{\text{INTB}}$	56
20	$\overline{\text{INTC}}$	59
21	$\overline{\text{INTD}}$	62
32:22	Unassigned	95

10.4 Reset and Initialization

After MR reset, IRQSER Slaves are put into the Continuous(Idle) mode. The Host Controller is responsible for starting the initial IRQSER Cycle to collect system's IRQ/Data default values. The system then follows with the Continuous/Quiet mode protocol (Stop Frame pulse width) for subsequent IRQSER cycles. It's the Host Controller's responsibility to provide the default values to 8259's and other system logic before the first IRQSER cycle is performed. For IRQSER system suspend, insertion, or removal application, the Host controller should be programmed into Continuous(Idle) mode first. This is to guarantee IRQSER bus in the Idle state before the system configuration changes.

11. CONFIGURATION REGISTER

11.1 Chip (Global) Control Register

CR02 (Default 0x00)

Bit 7 - 1: Reserved.
Bit 0: SWRST --> Soft Reset.

CR07

Bit 7 - 0: LDNB7 - LDNB0 --> Logical Device Number Bit 7 - 0

CR20

Bit 7 - 0: DEVIDB7 - DEBIDB0 --> Device ID Bit 7 - Bit 0 = 0x97 (read only).

CR21

Bit 7 - 0: DEVREVB7 - DEBREVB0 --> Device Rev Bit 7 - Bit 0 = 0x73 (read only).

CR22 (Default 0xff)

Bit 7 - 6: Reserved.
Bit 5: URBPWD
= 0 Power down
= 1 No Power down
Bit 4: URAPWD
= 0 Power down
= 1 No Power down
Bit 3: PRTPWD
= 0 Power down
= 1 No Power down
Bit 2, 1: Reserved.
Bit 0: FDCPWD
= 0 Power down
= 1 No Power down

CR23 (Default 0xFE)

Bit 7 - 1: Reserved.
Bit 0: IPD (Immediate Power Down). When set to 1, it will put the whole chip into power down mode immediately.

CR24 (Default 0b1s000s0s)

Bit 7: EN16SA
= 0 12 bit Address Qualification
= 1 16 bit Address Qualification
Bit 6: EN48
= 0 The clock input on Pin 1 should be 24 Mhz.
= 1 The clock input on Pin 1 should be 48 Mhz.
The corresponding power-on setting pin is SOUTB (pin 53).

Bit 5 - 3: Reserved.

Bit 2: ENKBC
= 0 KBC is disabled after hardware reset.
= 1 KBC is enabled after hardware reset.

This bit is read only, and set/reset by power-on setting pin. The corresponding power-on setting pin is SOUTA (pin 46).

Bit 1: Reserved

Bit 0: $\overline{\text{PNPCSV}}$
= 0 The Compatible PnP address select registers have default values.
= 1 The Compatible PnP address select registers have no default value.

When trying to make a change to this bit, new value of $\overline{\text{PNPCSV}}$ must be complementary to the old one to make an effective change. For example, the user must set $\overline{\text{PNPCSV}}$ to 0 first and then reset it to 1 to reset these PnP registers if the present value of $\overline{\text{PNPCSV}}$ is 1. The corresponding power-on setting pin is NDTRA (pin 44).

CR25 (Default 0x00)

Bit 7 - 6: Reserved
Bit 5: URBTRI
Bit 4: URATRI
Bit 3: PRTTRI
Bit 2 - 1 : Reserved
Bit 0: FDCTRI.

CR26 (Default 0b0s000000)

Bit 7: SEL4FDD
= 0 Select two FDD mode.
= 1 Select four FDD mode.

Bit 6: HEFRAS

These two bits define how to enable Configuration mode. The corresponding power-on setting pin is NRTSA (pin 43).

HEFRAS Address and Value
= 0 Write 87h to the location 3F0h twice.
= 1 Write 87h to the location 370h twice.

Bit 5: LOCKREG
= 0 Enable R/W Configuration Registers.
= 1 Disable R/W Configuration Registers.

Bit 4: Reserved.

Bit 3: DSFDLGRQ
= 0 Enable FDC legacy mode on IRQ and DRQ selection, then DO register bit 3 is effective on selecting IRQ
= 1 Disable FDC legacy mode on IRQ and DRQ selection, then DO register bit 3 is not effective on selecting IRQ

Bit 2: DSPRLGRQ

= 0 Enable PRT legacy mode on IRQ and DRQ selection, then DCR bit 4 is effective on selecting IRQ

= 1 Disable PRT legacy mode on IRQ and DRQ selection, then DCR bit 4 is not effective on selecting IRQ

Bit 1: DSUALGRQ

= 0 Enable UART A legacy mode IRQ selecting, then MCR bit 3 is effective on selecting IRQ

= 1 Disable UART A legacy mode IRQ selecting, then MCR bit 3 is not effective on selecting IRQ

Bit 0: DSUBLGRQ

= 0 Enable UART B legacy mode IRQ selecting, then MCR bit 3 is effective on selecting IRQ

= 1 Disable UART B legacy mode IRQ selecting, then MCR bit 3 is not effective on selecting IRQ

CR28 (Default 0x00)

Bit 7 - 5: Reserved.

Bit 4: IRQ Sharing selection.

= 0 Disable IRQ Sharing

= 1 Enable IRQ Sharing

Bit 3:Reserved

Bit 2 - 0: PRTMODS2 - PRTMODS0

= 0xx Parallel Port Mode

= 100 Reserved

= 101 External FDC Mode

= 110 Reserved

= 111 External two FDC Mode

CR2A (Default 0x00)

Bit 7: PIN57S

= 0 KBRST

= 1 GP12

Bit 6: PIN56S

= 0 GA20

= 1 GP11

Bit 5 - 4: PIN40S1, PIN40S0

= 00 Reserved

= 01 GP24

= 10 8042 P13

= 11 Reserved

Bit 3 - 2: Reserved.

Bit 1 - 0: PIN3S1, PIN3S0

= 00 DRVDEN1

= 01 GP10

= 10 8042 P12

= 11 $\overline{\text{SCI}}$

CR2B (Default 0x00)

- Bit 7 - 6: PIN73S1, PIN73S0
  - = 00 $\overline{\text{PANSWIN}}$
  - = 01 GP23
  - = 10 Reserved
  - = 11 Reserved
- Bit 5: PIN72S
  - = 0 $\overline{\text{PANSWOUT}}$
  - = 1 GP22
- Bit 4 - 3: PIN70S1, PIN70S0
  - = 00 $\overline{\text{SMI}}$
  - = 01 GP21
  - = 10 8042 P16
  - = 11 Reserved
- Bit 2 - 1: Reserved.
- Bit 0: PIN58S
  - = 0 KBLOCK
  - = 1 GP13

CR2C (Default 0x00)

- Bit 7 - 6: PIN121S1, PIN121S0
  - = 00 DRQ0
  - = 01 GP17
  - = 10 8042 P14
  - = 11 $\overline{\text{SCI}}$
- Bit 5 - 4: PIN119S1, PIN119S0
  - = 00 NDACK0
  - = 01 GP16
  - = 10 8042 P15
  - = 11 Reserved
- Bit 3 - 2: PIN104S1, PIN104S0
  - = 00 IRQ15
  - = 01 GP15
  - = 10 WDTO
  - = 11 Reserved
- Bit 1 - 0: PIN103S1, PIN103S0
  - = 00 IRQ14
  - = 01 GP14
  - = 10 PLEDO
  - = 11 Reserved

CR2D (Default 0x00)

Test Modes: Reserved for Winbond.

CR2E (Default 0x00)

Test Modes: Reserved for Winbond.

CR2F (Default 0x00)

Test Modes: Reserved for Winbond.

11.2 Logical Device 0 (FDC)

CR30 (Default 0x01 if $\overline{\text{PNPCSV}}$ = 0 during POR, default 0x00 otherwise)

Bit 7 - 1: Reserved.

Bit 0: = 1 Activates the logical device.
= 0 Logical device is inactive.

CR60, CR 61 (Default 0x03, 0xf0 if $\overline{\text{PNPCSV}}$ = 0 during POR, default 0x00, 0x00 otherwise)

These two registers select FDC I/O base address [0x100:0xFF8] on 8 byte boundary.

CR70 (Default 0x06 if $\overline{\text{PNPCSV}}$ = 0 during POR, default 0x00 otherwise)

Bit 7 - 4: Reserved.

Bit 3 - 0: These bits select IRQ resource for FDC.

CR74 (Default 0x02 if $\overline{\text{PNPCSV}}$ = 0 during POR, default 0x04 otherwise)

Bit 7 - 3: Reserved.

Bit 2 - 0: These bits select DRQ resource for FDC.
= 0x00 DMA0
= 0x01 DMA1
= 0x02 DMA2
= 0x03 DMA3
= 0x04 - 0x07 No DMA active

CRF0 (Default 0x0E)

FDD Mode Register

Bit 7: FIPURDWN

This bit controls the internal pull-up resistors of the FDC input pins RDATA, INDEX, TRAK0, DSKCHG, and WP.
= 0 The internal pull-up resistors of FDC are turned on.(Default)
= 1 The internal pull-up resistors of FDC are turned off.

Bit 6: INTVERTZ

This bit determines the polarity of all FDD interface signals.
= 0 FDD interface signals are active low.
= 1 FDD interface signals are active high.

Bit 5: DRV2EN (PS2 mode only)

When this bit is a logic 0, this indicates that a second drive is installed and is reflected in status register A.

Bit 4: Swap Drive 0, 1 Mode
= 0 No Swap (Default)
= 1 Drive and Motor sel 0 and 1 are swapped.

Bit 3 - 2 Interface Mode
= 11 AT Mode (Default)
= 10 (Reserved)
= 01 PS/2
= 00 Model 30

Bit 1: FDC DMA Mode
= 0 Burst Mode is enabled
= 1 Non-Burst Mode (Default)

Bit 0: Floppy Mode
= 0 Normal Floppy Mode (Default)
= 1 Enhanced 3-mode FDD

CRF1 (Default 0x00)

Bit 7 - 6: Boot Floppy
= 00 FDD A
= 01 FDD B
= 10 FDD C
= 11 FDD D

Bit 5, 4: Media ID1, Media ID0. These bits will be reflected on FDC's Tape Drive Register bit 7, 6.

Bit 3 - 2: Density Select
= 00 Normal (Default)
= 01 Normal
= 10 1 (Forced to logic 1)
= 11 0 (Forced to logic 0)

Bit 1: DISFDDWR
= 0 Enable FDD write.
= 1 Disable FDD write(forces pins WE, WD stay high).

Bit 0: SWWP
= 0 Normal, use WP to determine whether the FDD is write protected or not.
= 1 FDD is always write-protected.

CRF2 (Default 0xFF)

Bit 7 - 6: FDD D Drive Type

Bit 5 - 4: FDD C Drive Type

Bit 3 - 2: FDD B Drive Type

Bit 1:0: FDD A Drive Type

When FDD is in enhanced 3-mode(CRF0.bit0=1),these bits determine SELDEN value in TABLE A of CRF4 and CRF5 as follows.

DTYPE1	DPYTE0	DRATE1	DRATE0	SELDEN
0	0	1	1	1
0	0	0	0	1
0	0	0	1	0
0	0	1	0	0
0	1	X	X	0
1	0	X	X	1
1	1	0	1	0

Note: X means don't care.

CRF4 (Default 0x00)

FDD0 Selection:

Bit 7: Reserved.

Bit 6: Precomp. Disable.

= 1 Disable FDC Precompensation.
= 0 Enable FDC Precompensation.

Bit 5: Reserved.

Bit 4 - 3: DRTS1, DRTS0: Data Rate Table select (Refer to TABLE A).

= 00 Select Regular drives and 2.88 format
= 01 Specifical application
= 10 2 Meg Tape
= 11 Reserved

Bit 2: Reserved.

Bit 1:0: DMOD0, DMOD1 : Drive Model select (Refer to TABLE B).

CRF5 (Default 0x00)

FDD1 Selection: Same as FDD0 of CRF4.

TABLE A

Drive Rate Table Select		Data Rate		Selected Data Rate		SELDEN
DRTS1	**DRTS0**	**DRATE1**	**DRATE0**	**MFM**	**FM**	**CRF0 bit 0=0**
0	0	1	1	1Meg	---	1
		0	0	500K	250K	1
		0	1	300K	150K	0
		1	0	250K	125K	0
0	1	1	1	1Meg	---	1
		0	0	500K	250K	1
		0	1	500K	250K	0
		1	0	250K	125K	0
1	0	1	1	1Meg	---	1
		0	0	500K	250K	1
		0	1	2Meg	---	0
		1	0	250K	125K	0

Note:Refer to CRF2 for SELDEN value in the cases when CRF0, bit0=1.

TABLE B

DMOD0	DMOD1	DRVDEN0(pin 2)	DRVDEN1(pin 3)	DRIVE TYPE
0	0	SELDEN	DRATE0	4/2/1 MB 3.5”“ 2/1 MB 5.25” 2/1.6/1 MB 3.5” (3-MODE)
0	1	DRATE1	DRATE0	
1	0	$\overline{\text{SELDEN}}$	DRATE0	
1	1	DRATE0	DRATE1	

11.3 Logical Device 1 (Parallel Port)

CR30 (Default 0x01 if $\overline{\text{PNPCSV}}$ = 0 during POR, default 0x00 otherwise)

Bit 7 - 1: Reserved.

Bit 0:

= 1 Activates the logical device.

= 0 Logical device is inactive.

CR60, CR 61 (Default 0x03, 0x78 if $\overline{\text{PNPCSV}}$ = 0 during POR, default 0x00, 0x00 otherwise)

These two registers select Parallel Port I/O base address.

[0x100:0xFFC] on 4 byte boundary (EPP not supported) or

[0x100:0xFF8] on 8 byte boundary (all modes supported, EPP is only available when the base address is on 8 byte boundary).

CR70 (Default 0x07 if $\overline{\text{PNPCSV}}$ = 0 during POR, default 0x00 otherwise)

Bit 7 - 4: Reserved.

Bit [3:0]: These bits select IRQ resource for Parallel Port.

CR74 (Default 0x04)

Bit 7 - 3: Reserved.

Bit 2 - 0: These bits select DRQ resource for Parallel Port.

0x00=DMA0
0x01=DMA1
0x02=DMA2
0x03=DMA3
0x04 - 0x07= No DMA active

CRF0 (Default 0x3F)

Bit 7: PP Interrupt Type:

Not valid when the parallel port is in the printer Mode (100) or the standard & Bi-directional Mode (000).

= 1 Pulsed Low, released to high-Z .

= 0 IRQ follows nACK when parallel port in EPP Mode or [Printer, SPP, EPP] under ECP.

Bit [6:3]: ECP FIFO Threshold.

Bit 2 - 0 Parallel Port Mode

= 100 Printer Mode (Default)

= 000 Standard and Bi-direction (SPP) mode

= 001 EPP - 1.9 and SPP mode

= 101 EPP - 1.7 and SPP mode

= 010 ECP mode

= 011 ECP and EPP - 1.9 mode

= 111 ECP and EPP - 1.7 mode.

11.4 Logical Device 2 (UART A)¢)

CR30 (Default 0x01 if $\overline{\text{PNPCSV}}$ **= 0 during POR, default 0x00 otherwise)**

Bit 7 - 1: Reserved.

Bit 0:

= 1 Activates the logical device.

= 0 Logical device is inactive.

CR60, CR 61 (Default 0x03, 0xF8 if $\overline{\text{PNPCSV}}$ **= 0 during POR, default 0x00, 0x00 otherwise)**

These two registers select Serial Port 1 I/O base address [0x100:0xFF8] on 8 byte boundary.

CR70 (Default 0x04 if $\overline{\text{PNPCSV}}$ **= 0 during POR, default 0x00 otherwise)**

Bit 7 - 4: Reserved.

Bit 3 - 0: These bits select IRQ resource for Serial Port 1.

CRF0 (Default 0x00)

Bit 7 - 2: Reserved.

Bit 1 - 0: SUACLKB1, SUACLKB0

= 00 UART A clock source is 1.8462 Mhz (24MHz/13)

= 01 UART A clock source is 2 Mhz (24MHz/12)

= 10 UART A clock source is 24 Mhz (24MHz/1)

= 11 UART A clock source is 14.769 Mhz (24MHz/1.625)

11.5 Logical Device 3 (UART B)

CR30 (Default 0x01 if $\overline{\text{PNPCSV}}$ **= 0 during POR, default 0x00 otherwise)**

Bit 7 - 1: Reserved.

Bit 0:

= 1 Activates the logical device.

= 0 Logical device is inactive.

CR60, CR 61 (Default 0x02, 0xF8 if $\overline{\text{PNPCSV}}$ **= 0 during POR, default 0x00, 0x00 otherwise)**

These two registers select Serial Port 2 I/O base address [0x100:0xFF8] on 8 byte boundary.

CR70 (Default 0x03 if $\overline{\text{PNPCSV}}$ **= 0 during POR, default 0x00 otherwise)**

Bit 7 - 4: Reserved.

Bit [3:0]: These bits select IRQ resource for Serial Port 2.

CRF0 (Default 0x00)

Bit 7 - 4: Reserved.

Bit 3: RXW4C

= 0 No reception delay when SIR is changed from TX mode to RX mode.

= 1 Reception delays 4 characters-time (40 bit-time) when SIR is changed from TX mode to RX mode.

Bit 2: TXW4C

= 0 No transmission delay when SIR is changed from RX mode to TX mode.

= 1 Transmission delays 4 characters-time (40 bit-time) when SIR is changed from RX mode to TX mode.

Bit 1 - 0: SUBCLKB1, SUBCLKB0

= 00 UART B clock source is 1.8462 Mhz (24MHz/13)

= 01 UART B clock source is 2 Mhz (24MHz/12)

= 10 UART B clock source is 24 Mhz (24MHz/1)

= 11 UART B clock source is 14.769 Mhz (24MHz/1.625)

CRF1 (Default 0x00)

Bit 7: Reserved.

Bit 6: IRLOCSEL. IR I/O pins' location select.

= 0 Through SINB/SOUTB.

= 1 Through IRRX/IRTX.

Bit 5: IRMODE2. IR function mode selection bit 2.

Bit 4: IRMODE1. IR function mode selection bit 1.

Bit 3: IRMODE0. IR function mode selection bit 0.

IR MODE	IR FUNCTION	IRTX	IRRX
00X	Disable	tri-state	high
010*	IrDA	Active pulse 1.6 µS	Demodulation into SINB/IRRX
011*	IrDA	Active pulse 3/16 bit time	Demodulation into SINB/IRRX
100	ASK-IR	Inverting IRTX/SOUTB pin	routed to SINB/IRRX
101	ASK-IR	Inverting IRTX/SOUTB & 500 KHZ clock	routed to SINB/IRRX
110	ASK-IR	Inverting IRTX/SOUTB	Demodulation into SINB/IRRX
111*	ASK-IR	Inverting IRTX/SOUTB & 500 KHZ clock	Demodulation into SINB/IRRX

Note: The notation is normal mode in the IR function.

Bit 2: HDUPLX. IR half/full duplex function select.

= 0 The IR function is Full Duplex.

= 1 The IR function is Half Duplex.

Bit 1: TX2INV.

= 0 the SOUTB pin of UART B function or IRTX pin of IR function in normal condition.

= 1 inverse the SOUTB pin of UART B function or IRTX pin of IR function.

Bit 0: RX2INV.

= 0 the SINB pin of UART B function or IRRX pin of IR function in normal condition.

= 1 inverse the SINB pin of UART B function or IRRX pin of IR function

11.6 Logical Device 5 (KBC)

CR30 (Default 0x01 if PENKBC= 1 during POR, default 0x00 otherwise)

Bit 7 - 1: Reserved.

Bit 0:

= 1 Activates the logical device.

= 0 Logical device is inactive.

CR60, CR 61 (Default 0x00, 0x60 if PENKBC= 1 during POR, default 0x00 otherwise)

These two registers select the first KBC I/O base address [0x100:0xFFF] on 1 byte boundary.

CR62, CR 63 (Default 0x00, 0x64 if PENKBC= 1 during POR, default 0x00 otherwise)

These two registers select the second KBC I/O base address [0x100:0xFFF] on 1 byte boundary.

CR70 (Default 0x01 if PENKBC= 1 during POR, default 0x00 otherwise)

Bit 7 - 4: Reserved.

Bit [3:0]: These bits select IRQ resource for KINT (keyboard).

CR72 (Default 0x0C if PENKBC= 1 during POR, default 0x00 otherwise)

Bit 7 - 4: Reserved.

Bit [3:0]: These bits select IRQ resource for MINT (PS2 Mouse)

CRF0 (Default 0x83)

Bit 7 - 6: KBC clock rate selection

= 00 Select 6MHz as KBC clock input.

= 01 Select 8MHz as KBC clock input.

= 10 Select 12Mhz as KBC clock input.

= 11 Select 16Mhz as KBC clock input.

Bit 5 - 3: Reserved.

Bit 2: = 0 Port 92 disable.

= 1 Port 92 enable.

Bit 1: = 0 Gate20 software control.
= 1 Gate20 hardware speed up.
Bit 0: = 0 KBRST software control.
= 1 KBRST hardware speed up.

11.7 Logical Device 7 (GP I/O Port I)

CR30 (Default 0x00)

Bit 7 - 1: Reserved.
Bit 0: = 1 Activates the logical device.
= 0 Logical device is inactive.

CR60, CR 61 (Default 0x00, 0x00)

These two registers select GP1 I/O base address [0x100:0xFFF] on 1 byte boundary.

CR62, CR 63 (Default 0x00, 0x00)

These two registers select GP14 alternate function Primary I/O base address [0x100:0xFFE] on 2 byte boundary; They are available as you setting GP14 to be an alternate function (General Purpose Address Decode).

CR64, CR 65 (Default 0x00, 0x00)

These two registers select GP15 alternate function Primary I/O base address [0x100:0xFFF] on 1 byte boundary; They are available as you setting GP15 to be an alternate function (General Purpose Write Decode).

CR70 (Default 0x00)

Bit 7 - 4: Reserved.

Bit 3 - 0: These bits select IRQ resource for GP10 as you setting GP10 to be an alternate function (Interrupt Steering).

CR72 (Default 0x00)

Bit 7 - 4: Reserved.

Bit 3 - 0: These bits select IRQ resource for GP11 as you setting GP11 to be an alternate function (Interrupt Steering).

CRE0 (GP10, Default 0x01)

Bit 7 - 5: Reserved.
Bit 4: IRQ Filter Select
= 1 Debounce Filter Enabled
= 0 Debounce Filter Bypassed
Bit 3: Select Function.
= 1 Select Alternate Function: Interrupt Steering.
= 0 Select Basic I/O Function.
Bit 2: Reserved.
Bit 1: Polarity.
= 1 Invert.
= 0 No Invert.

Bit 0: In/Out selection.

= 1 Input.

= 0 Output.

CRE1 (GP11, Default 0x01)

Bit 7 - 5: Reserved.

Bit 4: IRQ Filter Select

= 1 Debounce Filter Enabled

= 0 Debounce Filter Bypassed

Bit 3: Select Function.

= 1 Select Alternate Function: Interrupt Steering.

= 0 Select Basic I/O Function.

Bit 2: Reserved.

Bit 1: Polarity.

= 1 Invert.

= 0 No Invert.

Bit 0: In/Out selection.

= 1 Input.

= 0 Output.

CRE2 (GP12, Default 0x01)

Bit 7 - 5: Reserved.

Bit 4 - 3: Select Function.

= 00 Select Basic I/O function.

= 01 Select 1st alternate function: Watch Dog Timer Output.

= 10 Reserved

= 11 Reserved

Bit 2: Reserved.

Bit 1: Polarity: 1: Invert, 0: No Invert

Bit 0: In/Out: 1: Input, 0: Output

CRE3 (GP13, Default 0x01)

Bit 7 - 5: Reserved.

Bit 4 - 3: Select Function.

= 00 Select Basic I/O function.

= 01 Select 1st alternate function: Power LED output.

= 10 Reserved

= 11 Reserved

Bit 2: Reserved.

Bit 1: Polarity: 1: Invert, 0: No Invert

Bit 0: In/Out: 1: Input, 0: Output

CRE4 (GP14, Default 0x01)

Bit 7 - 5: Reserved.
Bit 4 - 3: Select Function.
= 00 Select Basic I/O function.
= 01 Select 1st alternate function: General Purpose Address Decoder(Active Low when Bit 1 = 0, Decode two byte address).
= 10 Select 2nd alternate function: Keyboard Inhibit(P17).
= 11 Reserved
Bit 2: Reserved.
Bit 1: Polarity: 1: Invert, 0: No Invert
Bit 0: In/Out: 1: Input, 0: Output

CRE5 (GP15, Default 0x01)

Bit 7 - 5: Reserved.
Bit 4 - 3: Select Function.
= 00 Select Basic I/O function.
= 01 General Purpose Write Strobe(Active Low when Bit 1 = 0).
= 10 8042 P12.
= 11 Reserved
Bit 2: Reserved.
Bit 1: Polarity: 1: Invert, 0: No Invert
Bit 0: In/Out: 1: Input, 0: Output

CRE6 (GP16, Default 0x01)

Bit 7 - 5: Reserved.
Bit 4 - 3: Select Function.
= 00 Select Basic I/O function.
= 01 Select 1st alternate function: Watch Dog Timer Output.
= 1x Reserved
Bit 2: Reserved.
Bit 1: Polarity: 1: Invert, 0: No Invert
Bit 0: In/Out: 1: Input, 0: Output

CRE7 (GP17, Default 0x01)

Bit 7 - 4: Reserved.
Bit 4 - 3: Select Function.
= 00 Select Basic I/O function.
= 01 Select 1st alternate function: Power LED output. Please refer to TABLE C
= 1x Reserved
Bit 2: Reserved.
Bit 1: Polarity: 1: Invert, 0: No Invert
Bit 0: In/Out: 1: Input, 0: Output

TABLE C

WDT_CTRL1* BIT[1]*	WDT_CTRL0* BIT[3]	WDT_CTRL1 BIT[0]	POWER LED STATE
1	X	X	1 Hertz Toggle pulse
0	0	X	Continuous high or low*
0	1	0	Continuous high or low*
0	1	1	1 Hertz Toggle pulse

*Note: 1). Regarding to the contents of WDT_CTR1 and WDT_CTRL0, please refer to CRF3 and CRF4 in Logic Device 8.

2). Continuous high or low depends on the polarity bit of GP13 or GP17 configure registers.

CRF1 (Default 0x00)

General Purpose Read/Write Enable*

Bit 7 - 2: Reserved

Bit 1:

= 1 Enable General Purpose Write Strobe

= 0 Disable General Purpose Write Strobe

Bit 0:

= 1 Enable General Purpose Address Decode

= 0 Disable General Purpose Address Decode

*Note: If the logical device's activate bit is not set then bit 0 and 1 have no effect.

11.8 Logical Device 8 (GP I/O Port II)

CR30 (Default 0x00)

Bit 7 - 1: Reserved.

Bit 0: = 1 Activates the logical device.

= 0 Logical device is inactive.

CR60, CR 61 (Default 0x00, 0x00)

These two registers select GP2 & Watch Dog I/O base address [0x100:0xFFE] on 2 byte boundary. I/O base address + 1: Watch Dog I/O base address.

CR70 (Default 0x00)

Bit 7 - 4: Reserved.

Bit 3 - 0: These bits select IRQ resource for Common IRQ of GP20~GP26 at Logic Device 8.

CR72 (Default 0x00)

Bit 7 - 4: Reserved.

Bit 3 - 0: These bits select IRQ resource for Watch Dog.

CRE8 (GP20, Default 0x01)

Bit 7 - 5: Reserved.
Bit 4 - 3: Select Function.
= 00 Select basic I/O function
= 01 Reserved
= 10 Select alternate function: Keyboard Reset (connected to KBC P20)
= 11 Reserved
Bit 2: Int En
= 1 Enable Common IRQ
= 0 Disable Common IRQ
Bit 1: Polarity: 1: Invert, 0: No Invert
Bit 0: In/Out: 1: Input, 0: Output

CRE9 (GP21, Default 0x01)

Bit 7 - 5: Reserved

Bit 4 - 3: Select Function.
= 00 Select Basic I/O function
= 01 Reserved
= 10 Select 2nd alternate function: Keyboard P13 I/O
= 11 Reserved

Bit 2: Int En
= 1 Enable Common IRQ
= 0 Disable Common IRQ

Bit 1: Polarity: 1: Invert, 0: No Invert

Bit 0: In/Out: 1: Input, 0: Output

CREA (GP22, Default 0x01)

Bit 7 - 5: Reserved.

Bit 4 - 3: Select Function.
= 00 Select Basic I/O function.
= 01 Reserved
= 10 Select 2nd alternate function: Keyboard P14 I/O.
= 11 Reserved

Bit 2: Int En
= 1 Enable Common IRQ
= 0 Disable Common IRQ

Bit 1: Polarity: 1: Invert, 0: No Invert

Bit 0: In/Out: 1: Input, 0: Output¡@¡@

CREB (GP23, Default 0x01)

Bit 7 - 5: Reserved.

Bit 4 - 3: Select Function.

- = 00 Select Basic I/O function
- = 01 Reserved
- = 10 Select 2nd alternate function: Keyboard P15 I/O
- = 11 Reserved

Bit 2: Int En

- = 1 Enable Common IRQ
- = 0 Disable Common IRQ

Bit 1: Polarity: 1: Invert, 0: No Invert

Bit 0: In/Out: 1: Input, 0: Output¡@

CREC (GP24, Default 0x01)

Bit 7 - 5: Reserved.

Bit 4 - 3: Select Function.

- = 00 Select Basic I/O function
- = 01 Reserved
- = 10 Select 2nd alternate function: Keyboard P16 I/O
- = 11 Reserved

Bit 2: Int En

- = 1 Enable Common IRQ
- = 0 Disable Common IRQ

Bit 1: Polarity: 1: Invert, 0: No Invert

Bit 0: In/Out: 1: Input, 0: Output

CRED (GP25, Default 0x01)

Bit 7 - 4: Reserved.

Bit 3: Select Function.

- = 1 Select alternate function: GATE A20(Connect to KBC P21).
- = 0 Select basic I/O function

Bit 2: Int En

- = 1 Enable Common IRQ
- = 0 Disable Common IRQ

Bit 1: Polarity: 1: Invert, 0: No Invert

Bit 0: In/Out: 1: Input, 0: Output

CREE (GP26, Default 0x01)

Bit 7 - 3: Reserved.

Bit 2: Int En

= 1 Enable Common IRQ

= 0 Disable Common IRQ

Bit 1: Polarity: 1: Invert, 0: No Invert

Bit 0: In/Out: 1: Input, 0: Output

CRF0 (Default 0x00)

Debounce Filter Enable or Disable for General Purpose I/O Combined Interrupt. The Debounce Filter can reject a pulse with 1ms width or less.

Bit 7 - 4: Reserved

Bit 3: GP Common IRQ Filter Select

= 1 Debounce Filter Enabled

= 0 Debounce Filter Bypassed

Bit 2 - 0: Reserved

CRF1 (Reserved)

CRF2 (Default 0x00)

Watch Dog Timer Time-out value. Writing a non-zero value to this register causes the counter to load the value to Watch Dog Counter and start to count down. If the Bit2 and Bit 1 are set, any Mouse Interrupt or Keyboard Interrupt happen will also cause to reload the non-zero value to Watch Dog Counter and count down. Read this register can not access Watch Dog Timer Time-out value, but can access the current value in Watch Dog Counter.

Bit 7 - 0:

= 0x00 Time-out Disable

= 0x01 Time-out occurs after 1 minute

= 0x02 Time-out occurs after 2 minutes

= 0x03 Time-out occurs after 3 minutes

…………………………………………

= 0xFF Time-out occurs after 255 minutes

CRF3 (WDT_CTRL0, Default 0x00)

Watch Dog Timer Control Register #0

Bit 7 - 4: Reserved

Bit 3: When Time-out occurs, Enable or Disable Power LED with 1 Hz and 50% duty cycle output.

= 1 Enable

= 0 Disable

Bit 2: Mouse interrupt reset Enable or Disable

= 1 Watch Dog Timer is reset upon a Mouse interrupt

= 0 Watch Dog Timer is not affected by Mouse interrupt

Bit 1: Keyboard interrupt reset Enable or Disable

= 1 Watch Dog Timer is reset upon a Keyboard interrupt

= 0 Watch Dog Timer is not affected by Keyboard interrupt

Bit 0: Reserved.

CRF4 (WDT_CTRL1, Default 0x00)

Watch Dog Timer Control Register #1

Bit 7 - 4: Reserved

Bit 3: Enable the rising edge of Keyboard Reset(P20) to force Time-out event, R/W*

= 1 Enable

= 0 Disable

Bit 2: Force Watch Dog Timer Time-out, Write only*

= 1 Force Watch Dog Timer time-out event; this bit is self-clearing.

Bit 1: Enable Power LED 1Hz rate toggle pulse with 50% duty cycle , R/W

= 1 Enable

= 0 Disable

Bit 0: Watch Dog Timer Status, R/W

= 1 Watch Dog Timer time-out occurred.

= 0 Watch Dog Timer counting

*Note: 1). Internal logic provides an 1us Debounce Filter to reject the width of P20 pulse less than 1us.

2). The P20 signal that coming from Debounce Filter is ORed with the signal generated by the Force Time-out bit and then connect to set the Bit 0(Watch Dog Timer Status). The ORed signal is self-clearing.

11.9 Logical Device 9 (GP I/O Port III)

CR30 (Default 0x00)

Bit 7 - 1: Reserved.

Bit 0: = 1 Activates the logical device.

= 0 Logical device is inactive.

CR60, CR 61 (Default 0x00, 0x00)

These two registers select GP3 I/O base address [0x100:0xFFF] on 1 byte boundary.

CR62, CR 63 (Default 0x00, 0x00)

These two registers select GP32 alternate function Primary I/O base address [0x100:0xFFE] on 2-byte boundary; They are available as you setting GP32 to be an alternate function (General Purpose Address Decode).

CR64, CR 65 (Default 0x00, 0x00)

These two registers select GP33 alternate function Primary I/O base address [0x100:0xFFF] on 2-byte boundary; They are available as you setting GP33 to be an alternate function (General Purpose Address Decode).

CR70 (Default 0x00)

Bit 7 - 4: Reserved.

Bit 3 - 0: These bits select IRQ resource for GP30 as you setting GP30 to be an alternate function (Interrupt Steering).

CR72 (Default 0x00)

Bit 7 - 4: Reserved.

Bit 3 - 0: These bits select IRQ resource for GP31 as you setting GP31 to be an alternate function (Interrupt Steering).

CRE0 (GP30, Default 0x01)

Bit 7 - 5: Reserved.

Bit 4: IRQ Filter Select

= 1 Debounce Filter Enabled.

= 0 Debounce Filter Bypassed.

Bit 3: Select Function.

= 1 Select Alternate Function: Interrupt Steering.

= 0 Select Basic I/O Function.

Bit 2: Reserved.

Bit 1: Polarity.

= 1 Invert.

= 0 No Invert.

Bit 0: In/Out selection.

= 1 Input.

= 0 Output.

CRE1 (GP31, Default 0x01)

Bit 7 - 5: Reserved.

Bit 4: IRQ Filter Select

= 1 Debounce Filter Enabled

= 0 Debounce Filter Bypassed

Bit 3: Select Function.

= 1 Select Alternate Function: Interrupt Steering.

= 0 Select Basic I/O Function.

Bit 2: Reserved.

Bit 1: Polarity.

= 1 Invert.

= 0 No Invert.

Bit 0: In/Out selection.

= 1 Input.

= 0 Output.

CRE2 (GP32, Default 0x01)

Bit 7 - 4: Reserved.

Bit 3: Select Function.

= 1 Select Alternate Function: General Purpose Address Decode.

= 0 Select Basic I/O Function.

Bit 2: Reserved.

Bit 1: Polarity: 1: Invert, 0: No Invert

Bit 0: In/Out: 1: Input, 0: Output

CRE3 (GP33, Default 0x01)

Bit 7 - 4: Reserved.

Bit 3: Select Function.

= 1 Select Alternate Function: General Purpose Address Decode.

= 0 Select Basic I/O Function.

Bit 2: Reserved.
Bit 1: Polarity: 1: Invert, 0: No Invert
Bit 0: In/Out: 1: Input, 0: Output

CRE4 (GP34, Default 0x01)

Bit 7 - 4: Reserved.
Bit 3: Select Function.
= 1   Select Alternate Function: Watch Dog Timer output.
= 0   Select Basic I/O Function.
Bit 2: Reserved.
Bit 1: Polarity: 1: Invert, 0: No Invert
Bit 0: In/Out: 1: Input, 0: Output

CRE5 (GP35, Default 0x01)

Bit 7 - 2: Reserved.
Bit 1: Polarity: 1: Invert, 0: No Invert
Bit 0: In/Out: 1: Input, 0: Output

CRE6 (GP36, Default 0x01)

Bit 7 - 2: Reserved.
Bit 1: Polarity: 1: Invert, 0: No Invert
Bit 0: In/Out: 1: Input, 0: Output

CRE7 (GP37, Default 0x01)

Bit 7 - 2: Reserved.
Bit 1: Polarity: 1: Invert, 0: No Invert
Bit 0: In/Out: 1: Input, 0: Output

CRF1 (Default 0x00)

Bit 7 - 3: Reserved
Bit 2: SERIRQ
= 0   The IRQ system is in normal mode.
= 1   The IRQ system is in serial IRQ mode.
Bit 1:
= 1 Enable GP33 General Purpose Address Decode.
= 0 Disable GP33 General Purpose Address Decode.
Bit 0:
= 1 Enable GP32 General Purpose Address Decode.
= 0 Disable GP32 General Purpose Address Decode.

*Note: If the logical device's activate bit is not set then bit 0 and 1 have no effect.

11.10 Logical Device A (ACPI)

CR30 (Default 0x00)

Bit 7 - 1: Reserved.
Bit 0: = 1 Activates the logical device.
= 0 Logical device is inactive.

CR60, CR 61 (Default 0x00, 0x00)

These two registers select PM1 register block base address [0x100:0xFF0] on 16-byte boundary.

CR62, CR 63 (Default 0x00, 0x00)

These two registers select GPE0 register block base address [0x100:0xFFC] on 4-byte boundary.

CR64, CR 65 (Default 0x00, 0x00)

These two registers select GPE1 register block base address [0x100:0xFFC] on 4-byte boundary.

CR70 (Default 0x00)

Bit 7 - 4: Reserved.

Bit 3 - 0: These bits select IRQ resource for $\overline{\text{SCI}}$.

CRE0 (Default 0x00)

Bit 7: DIS-PANSWIN. Disable panel switch input to turn system power supply on.

= 0 $\overline{\text{PANSWIN}}$ is wire-ANDed and connected to $\overline{\text{PANSWOUT}}$.

= 1 $\overline{\text{PANSWIN}}$ is blocked and can not affect $\overline{\text{PANSWOUT}}$.

Bit 6: ENKBWAKEUP. Enable Keyboard to wake-up system via $\overline{\text{PANSWOUT}}$.
= 0 Disable Keyboard wake-up function.
= 1 Enable Keyboard wake-up function.

Bit 5: ENMSWAKEUP. Enable Mouse to wake-up system via $\overline{\text{PANSWOUT}}$.
= 0 Disable Mouse wake-up function.
= 1 Enable Mouse wake-up function.

Bit 4: MSRKEY. Select Mouse Left/Right Botton to wake-up system via $\overline{\text{PANSWOUT}}$.
= 0 Select click on Mouse Left-botton twice to wake the system up.
= 1 Select click on Mouse right-botton twice to wake the system up.
Bit 3: Reserved.
Bit 2: KB/MS Swap. Enable Keyboard/Mouse port-swap.
= 0 Keyboard/Mouse ports are not swapped.
= 1 Keyboard/Mouse ports are swapped.
Bit 1: MSXKEY. Enable any character received from Mouse to wake-up the system.
= 0 Just clicking Mouse left/right-botton twice can wake the system up.
= 1 Any character received from Mouse can wake the system up (the setting of Bit 4 is ignored).

Bit 0: KBXKEY. Enable any character received from Keyboard to wake-up the system.

= 0 Only predetermined specific key combination can wake up the system.

= 1 Any character received from Keyboard can wake up the system.

CRE1 (Default 0x00) Keyboard Wake-up Index Register

This register is used to indicate which Keyboard Wake-up Shift register or Predetermined key Register is to be read/written via CRE2.

CRE2 Keyboard Wake-up Data Register

CRE3 (Read only) Keyboard/Mouse Wake-up Status Register

Bit 7-3: Reserved.

Bit 2: PANSW_STS. The Panel switch event is caused by $\overline{\text{PANSWIN}}$. This bit is cleared by reading this register.

Bit 1: Mouse_STS. The Panel switch event is caused by Mouse wake-up event. This bit is cleared by reading this register.

Bit 0: Keyboard_STS. The Panel switch event is caused by Keyboard wake-up event. This bit is cleared by reading this register.

CRE4 This Register is reserved for test.

CRF0 (Default 0x00)

Bit 7: CHIPPME. Chip level power management enable.

= 0 disable the ACPI/Legacy and the auto power management functions

= 1 enable the ACPI/Legacy and the auto power management functions.

Bit 6 - 4: Reserved. Return zero when read.

Bit 3: PRTPME. Printer port power management enable.

= 0 disable the auto power management functions.

= 1 enable the auto power management functions provided CRF0.bit7 (CHIPPME) is also set to 1.

Bit 2: FDCPME. FDC power management enable.

= 0 disable the auto power management functions.

= 1 enable the auto power management functions provided CRF0.bit7 (CHIPPME) is also set to 1.

Bit 1: URAPME. UART A power management enable.

= 0 disable the auto power management functions.

= 1 enable the auto power management functions provided CRF0.bit7 (CHIPPME) is also set to 1.

Bit 0: URBPME. UART B power management enable.

= 0 disable the auto power management functions.

= 1 enable the auto power management functions provided CRF0.bit7 (CHIPPME) is also set to 1.

CRF1 (Default 0x00)

Bit 7 - 4: Reserved. Return zero when read.

Bit 3 - 0: Devices' idle status.

These bits indicate that the individual device's idle timer expires due to no I/O access, no IRQ, and no external input to the device. These 4 bits are controlled by the printer port, FDC, UART A, and UART B power down machines individually. Writing a 1 clears this bit, and writing a 0 has no effect. Note that: the user is not supposed to change the status while the power management function is enabled.

Bit 3: PRTIDLSTS. Printer port idle status.

= 0 printer port is now in the working state.

= 1 printer port is now in the sleeping state due to no printer port access, no IRQ, no DMA acknowledge, and no transition on BUSY, $\overline{\text{ACK}}$, PE, SLCT, and $\overline{\text{ERR}}$ pins in a preset expiry time period.

Bit 2: FDCIDLSTS. FDC idle status.

= 0 FDC is now in the working state.

= 1 FDC is now in the sleeping state due to no FDC access, no IRQ, no DMA acknowledge, and no enabling of the motor enable bits in the DOR register in a preset expiry time period.

Bit 1: URAIDLSTS. UART A idle status.

= 0 UART A is now in the working state.

= 1 UART A is now in the sleeping state due to no UART A access, no IRQ, the receiver is now waiting for a start bit, the transmitter shift register is now empty, and no transition on MODEM control input lines in a preset expiry time period.

Bit 0: URBIDLSTS. UART B idle status.

= 0 UART B is now in the working state.

= 1 UART B is now in the sleeping state due to no UART A access, no IRQ, the receiver is now waiting for a start bit, the transmitter shift register is now empty, and no transition on MODEM control input lines in a preset expiry time period.

CRF2 (Default 0x00)

Bit 7 - 4: Reserved. Return zero when read.

Bit 3 - 0: Devices' trap status.

These bits indicate that the individual device wakes up due to any I/O access, IRQ, and external input to the device. The device's idle timer reloads the preset expiry depending on which device wakes up. These 4 bits are controlled by the printer port, FDC, UART A, and UART B power down machines respectively. Writing a 1 clears this bit, and writing a 0 has no effect. Note that: the user is not supposed to change the status while power management function is enabled.

Bit 3: PRTTRAPSTS. Printer port trap status.

= 0 the printer port is now in the sleeping state.

= 1 the printer port is now in the working state due to any printer port access, any IRQ, any DMA acknowledge, and any transition on BUSY, $\overline{\text{ACK}}$, PE, SLCT, and $\overline{\text{ERR}}$ pins.

Bit 2: FDCTRAPSTS. FDC trap status.

= 0 FDC is now in the sleeping state.

= 1 FDC is now in the working state due to any FDC access, any IRQ, any DMA acknowledge, and any enabling of the motor enable bits in the DOR register.

Bit 1: URATRAPSTS. UART A trap status.

= 0 UART A is now in the sleeping state.

= 1 UART A is now in the working state due to any UART A access, any IRQ, the receiver begins receiving a start bit, the transmitter shift register begins transmitting a start bit, and any transition on MODEM control input lines.

Bit 0: URBTRAPSTS. UART B trap status.

= 0 UART B is now in the sleeping state.

= 1 UART B is now in the working state due to any UART B access, any IRQ, the receiver begins receiving a start bit, the transmitter shift register begins transmitting a start bit, and any transition on MODEM control input lines.

CRF3 (Default 0x00)

Bit 7 - 6: Reserved. Return zero when read.

Bit 5 - 0: Device's IRQ status.

These bits indicate the IRQ status of the individual device. The device's IRQ status bit is set by their source device and is cleared by writing a 1. Writing a 0 has no effect.

Bit 5: MOUIRQSTS. MOUSE IRQ status.

Bit 4: KBCIRQSTS. KBC IRQ status.

Bit 3: PRTIRQSTS. printer port IRQ status.

Bit 2: FDCIRQSTS. FDC IRQ status.

Bit 1: URAIRQSTS. UART A IRQ status.

Bit 0: URBIRQSTS. UART B IRQ status.

CRF4 (Default 0x00)

Bit 7 - 4: Reserved. Return zero when read.

Bit 3 - 0: Enable bits of the $\overline{\text{SMI}}$ generation due to the device's idleness.

These bits enable the generation of an $\overline{\text{SMI}}$ interrupt due to the expiration of the device's idle timer. These 4 bits control the printer port, FDC, UART A, and UART B $\overline{\text{SMI}}$ logics respectively.

Bit 3: PRTIDLEN.

= 0 disable the generation of an $\overline{\text{SMI}}$ interrupt due to printer port's idleness.

= 1 enable the generation of an $\overline{\text{SMI}}$ interrupt due to printer port's idleness.

Bit 2: FDCIDLEN.

= 0 disable the generation of an $\overline{\text{SMI}}$ interrupt due to FDC's idleness.

= 1 enable the generation of an $\overline{\text{SMI}}$ interrupt due to FDC's idleness.

Bit 1: URAIDLEN.

= 0 disable the generation of an $\overline{\text{SMI}}$ interrupt due to UART A's idleness.

= 1 enable the generation of an $\overline{\text{SMI}}$ interrupt due to UART A's idleness.

Bit 0: URBIDLEN.

= 0 disable the generation of an $\overline{\text{SMI}}$ interrupt due to UART B's idleness.

= 1 enable the generation of an $\overline{\text{SMI}}$ interrupt due to UART B's idleness.

CRF5 (Default 0x00)

Bit 7 - 4: Reserved. Return zero when read.

Bit 3 - 0: Enable bits of the $\overline{\text{SMI}}$ generation due to device's trap.

These bits enable the generation of an $\overline{\text{SMI}}$ interrupt due to any I/O access, IRQ, and external input to the device. These 4 bits control the printer port, FDC, UART A, and UART B SMI logics respectively.

Bit 3: PRTTRAPEN.

= 0 disable the generation of an $\overline{\text{SMI}}$ interrupt due to printer port's trap.

= 1 enable the generation of an $\overline{\text{SMI}}$ interrupt due to printer port's trap.

Bit 2: FDCTRAPEN.

= 0 disable the generation of an $\overline{\text{SMI}}$ interrupt due to FDC's trap.

= 1 enable the generation of an $\overline{\text{SMI}}$ interrupt due to FDC's trap.

Bit 1: URATRAPEN.

= 0 disable the generation of an $\overline{\text{SMI}}$ interrupt due to UART A's trap.

= 1 enable the generation of an $\overline{\text{SMI}}$ interrupt due to UART A's trap.

Bit 0: URBTRAPEN.

= 0 disable the generation of an $\overline{\text{SMI}}$ interrupt due to UART B's trap.

= 1 enable the generation of an $\overline{\text{SMI}}$ interrupt due to UART B's trap.

CRF6 (Default 0x00)

Bit 7 - 6: Reserved. Return zero when read.

Bit 5 - 0: Enable bits of the $\overline{\text{SMI}}$ generation due to the device's IRQ.

These bits enable the generation of an $\overline{\text{SMI}}$ interrupt due to any IRQ of the devices. These 4 bits control the printer port, FDC, UART A, and UART B $\overline{\text{SMI}}$ logics respectively. The $\overline{\text{SMI}}$ logic output for the IRQs is as follows:

$\overline{\text{SMI}}$ logic output = (URBIRQEN and URBIRQSTS) or (URAIRQEN and URAIRQSTS) or
(FDCIRQEN and FDCIRQSTS) or (PRTIRQEN and PRTIRQSTS)
(KBCIRQEN and KBCIRQSTS) or (MOUIRQEN and MOUIRQSTS)

Bit 5: MOUIRQEN.

= 0 disable the generation of an $\overline{\text{SMI}}$ interrupt due to MOUSE's IRQ.

= 1 enable the generation of an $\overline{\text{SMI}}$ interrupt due to MOUSE's IRQ.

Bit 4: KBCIRQEN.

= 0 disable the generation of an $\overline{\text{SMI}}$ interrupt due to KBC's IRQ.

= 1 enable the generation of an $\overline{\text{SMI}}$ interrupt due to KBC's IRQ.

Bit 3: PRTIRQEN.

= 0 disable the generation of an $\overline{\text{SMI}}$ interrupt due to printer port's IRQ.

= 1 enable the generation of an $\overline{\text{SMI}}$ interrupt due to printer port's IRQ.

Bit 2: FDCIRQEN.

= 0 disable the generation of an $\overline{\text{SMI}}$ interrupt due to FDC's IRQ.

= 1 enable the generation of an $\overline{\text{SMI}}$ interrupt due to FDC's IRQ.

Bit 1: URAIRQEN.

= 0 disable the generation of an $\overline{\text{SMI}}$ interrupt due to UART A's IRQ.

= 1 enable the generation of an $\overline{\text{SMI}}$ interrupt due to UART A's IRQ.

Bit 0: URBIRQEN.

= 0 disable the generation of an $\overline{\text{SMI}}$ interrupt due to UART B's IRQ.

= 1 enable the generation of an $\overline{\text{SMI}}$ interrupt due to UART B's IRQ.

CRF7 (Default 0x00)

Bit 7 - 1: Reserved. Return zero when read.

Bit 0: SMI_EN.

This bit is the $\overline{\text{SMI}}$ output pin enable bit. When an $\overline{\text{SMI}}$ event is raised on the output of the $\overline{\text{SMI}}$ logic, setting this bit enables the $\overline{\text{SMI}}$ interrupt to be generated on the pin $\overline{\text{SMI}}$. If this bit is cleared, only the IRQ status bit in CRF3 is set, and no SMI interrupt is generated on the pin $\overline{\text{SMI}}$.

= 0 Disable $\overline{\text{SMI}}$

= 1 Enable $\overline{\text{SMI}}$

CRFE, FF (Default 0x00)

Reserved for Winbond test.

12.0 SPECIFICATIONS

12.1 Absolute Maximum Ratings

PARAMETER	RATING	UNIT
Power Supply Voltage	-0.5 to 7.0	V
Input Voltage	-0.5 to V_{DD}+0.5	V
Battery Voltage V_{BAT}	4.0 to 1.8	V
Operating Temperature	0 to +70	° C
Storage Temperature	-55 to +150	° C

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

12.2 DC CHARACTERISTICS

(Ta = 0° C to 70° C, V_{DD} = 5V ± 10%, V_{SS} = 0V)

PARAMETER	SYM.	MIN.	TYP.	MAX.	UNIT	CONDITIONS
Battery Quiescent Current	I_{BAT}			2.4	uA	V_{BAT} = 2.5 V
Stand-by Power Supply Quiescent Current	I_{BAT}			2.0	mA	V_{SB} = 5.0 V, All ACPI pins are not connected.
I/O$_{8t}$ - TTL level bi-directional pin with source-sink capability of 8 mA						
Input Low Voltage	V_{IL}			0.8	V	
Input High Voltage	V_{IH}	2.0			V	
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 8 mA
Output High Voltage	V_{OH}	2.4			V	I_{OH} = - 8 mA
Input High Leakage	I_{LIH}			+10	μA	V_{IN} = V_{DD}
Input Low Leakage	I_{LIL}			-10	μA	V_{IN} = 0V
I/O$_{6t}$ - TTL level bi-directional pin with source-sink capability of 6 mA						
Input Low Voltage	V_{IL}			0.8	V	
Input High Voltage	V_{IH}	2.0			V	
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 6 mA
Output High Voltage	V_{OH}	2.4			V	I_{OH} = - 6 mA
Input High Leakage	I_{LIH}			+10	μA	V_{IN} = V_{DD}
Input Low Leakage	I_{LIL}			-10	μA	V_{IN} = 0V

12.2 DC CHARACTERISTICS, continued

PARAMETER	SYM.	MIN.	TYP.	MAX.	UNIT	CONDITIONS
I/O$_8$ - CMOS level bi-directional pin with source-sink capability of 8 mA						
Input Low Voltage	VIL			0.3xVDD	V	
Input High Voltage	VIH	0.7xVDD			V	
Output Low Voltage	VOL			0.4	V	IOL = 8 mA
Output High Voltage	VOH	3.5			V	IOH = - 8 mA
Input High Leakage	ILIH			+ 10	μA	VIN = VDD
Input Low Leakage	ILIL			- 10	μA	VIN = 0V
I/O$_{12}$ - CMOS level bi-directional pin with source-sink capability of 12 mA						
Input Low Voltage	VIL			0.3xVDD	V	
Input High Voltage	VIH	0.7xVDD			V	
Output Low Voltage	VOL			0.4	V	IOL = 12 mA
Output High Voltage	VOH	3.5			V	IOH = - 12 mA
Input High Leakage	ILIH			+ 10	μA	VIN = VDD
Input Low Leakage	ILIL			- 10	μA	VIN = 0V
I/O$_{16u}$ - CMOS level bi-directional pin with source-sink capability of 16 mA, with internal pull-up resistor						
Input Low Voltage	VIL			0.3xVDD	V	
Input High Voltage	VIH	0.7xVDD			V	
Output Low Voltage	VOL			0.4	V	IOL = 16 mA
Output High Voltage	VOH	3.5			V	IOH = - 16 mA
Input High Leakage	ILIH			+ 10	μA	VIN = VDD
Input Low Leakage	ILIL			- 10	μA	VIN = 0V
I/OD$_{16u}$ - CMOS level Open-Drain pin with source-sink capability of 16 mA, with internal pull-up resistor						
Input Low Voltage	VIL			0.3xVDD	V	
Input High Voltage	VIH	0.7xVDD			V	
Output Low Voltage	VOL			0.4	V	IOL = 16 mA
Output High Voltage	VOH	3.5			V	IOH = - 16 mA
Input High Leakage	ILIH			+ 10	μA	VIN = VDD
Input Low Leakage	ILIL			- 10	μA	VIN = 0V

12.2 DC CHARACTERISTICS, continued

PARAMETER	SYM.	MIN.	TYP.	MAX.	UNIT	CONDITIONS
I/O$_{12t}$ - TTL level bi-directional pin with source-sink capability of 12 mA						
Input Low Voltage	VIL			0.8	V	
Input High Voltage	VIH	2.0			V	
Output Low Voltage	VOL			0.4	V	IOL = 12 mA
Output High Voltage	VOH	2.4			V	IOH = - 12 mA
Input High Leakage	ILIH			+ 10	µA	VIN = VDD
Input Low Leakage	ILIL			- 10	µA	VIN = 0V
I/O$_{24t}$ - TTL level bi-directional pin with source-sink capability of 24 mA						
Input Low Voltage	VIL			0.8	V	
Input High Voltage	VIH	2.0			V	
Output Low Voltage	VOL			0.4	V	IOL = 24 mA
Output High Voltage	VOH	2.4			V	IOH = - 24 mA
Input High Leakage	ILIH			+ 10	µA	VIN = VDD
Input Low Leakage	ILIL			- 10	µA	VIN = 0V
OUT$_{8t}$ - TTL level output pin with source-sink capability of 8 mA						
Output Low Voltage	VOL			0.4	V	IOL = 8 mA
Output High Voltage	VOH	2.4			V	IOH = - 8 mA
OUT$_{12t}$ - TTL level output pin with source-sink capability of 12 mA						
Output Low Voltage	VOL			0.4	V	IOL = 12 mA
Output High Voltage	VOH	2.4			V	IOH = -12 mA
OD$_{12}$ - Open-drain output pin with sink capability of 12 mA						
Output Low Voltage	VOL			0.4	V	IOL = 12 mA
OD$_{24}$ - Open-drain output pin with sink capability of 24 mA						
Output Low Voltage	VOL			0.4	V	IOL = 24 mA
IN$_{t}$ - TTL level input pin						
Input Low Voltage	VIL			0.8	V	
Input High Voltage	VIH	2.0			V	
Input High Leakage	ILIH			+10	µA	VIN = VDD
Input Low Leakage	ILIL			-10	µA	VIN = 0 V

12.2 DC CHARACTERISTICS, continued

PARAMETER	SYM.	MIN.	TYP.	MAX.	UNIT	CONDITIONS
IN$_c$ - CMOS level input pin						
Input Low Voltage	VIL			0.3×VDD	V	
Input High Voltage	VIH	0.7×VDD			V	
Input High Leakage	ILIH			+10	μA	VIN = VDD
Input Low Leakage	ILIL			-10	μA	VIN = 0 V
IN$_{cs}$ - CMOS level Schmitt-triggered input pin						
Input Low Threshold Voltage	Vt-	1.3	1.5	1.7	V	VDD = 5 V
Input High Threshold Voltage	Vt+	3.2	3.5	3.8	V	VDD = 5 V
Hystersis	VTH	1.5	2		V	VDD = 5 V
Input High Leakage	ILIH			+10	μA	VIN = VDD
Input Low Leakage	ILIL			-10	μA	VIN = 0 V
IN$_{cu}$ - CMOS level input pin with internal pull-up resistor						
Input Low Voltage	VIL			0.7xVDD	V	
Input High Voltage	VIH	0.7xVDD			V	
Input High Leakage	ILIH			+10	μA	VIN = VDD
Input Low Leakage	ILIL			-10	μA	VIN = 0 V
IN$_{ts}$ - TTL level Schmitt-triggered input pin						
Input Low Threshold Voltage	Vt-	0.5	0.8	1.1	V	VDD = 5 V
Input High Threshold Voltage	Vt+	1.6	2.0	2.4	V	VDD = 5 V
Hystersis	VTH	0.5	1.2		V	VDD = 5 V
Input High Leakage	ILIH			+10	μA	VIN = VDD
Input Low Leakage	ILIL			-10	μA	VIN = 0 V
IN$_{tsu}$ - TTL level Schmitt-triggered input pin with internal pull-up resistor						
Input Low Threshold Voltage	Vt-	0.5	0.8	1.1	V	VDD = 5 V
Input High Threshold Voltage	Vt+	1.6	2.0	2.4	V	VDD = 5 V
Hystersis	VTH	0.5	1.2		V	VDD = 5 V
Input High Leakage	ILIH			+10	μA	VIN = VDD
Input Low Leakage	ILIL			-10	μA	VIN = 0 V

12.3 AC Characteristics

12.3.1 FDC: Data rate = 1 MB, 500 KB, 300 KB, 250 KB/sec.

PARAMETER	**SYM.**	**TEST CONDITIONS**	**MIN.**	**TYP.** (NOTE 1)	**MAX.**	**UNIT**
SA9-SA0, AEN, $\overline{\text{DACK}}$, $\overline{\text{CS}}$, setup time to $\overline{\text{IOR}}$ ¡ õ	TAR		25			nS
SA9-SA0, AEN, $\overline{\text{DACK}}$, hold time for $\overline{\text{IOR}}$ ¡ ô	TAR		0			nS
$\overline{\text{IOR}}$ width	TRR		80			nS
Data access time from $\overline{\text{IOR}}$ ¡ õ	TFD	CL = 100 pf			80	nS
Data hold from $\overline{\text{IOR}}$ ¡ õ	TDH	CL = 100 pf	10			nS
SD to from $\overline{\text{IOR}}$ ¡ ô	TDF	CL = 100 pf	10		50	nS
IRQ delay from $\overline{\text{IOR}}$ ¡ ô	TRI				360/570 /675	nS
SA9-SA0, AEN, $\overline{\text{DACK}}$, setup time to $\overline{\text{IOW}}$ ¡ õ	TAW		25			nS
SA9-SA0, AEN, $\overline{\text{DACK}}$, hold time for $\overline{\text{IOW}}$ ¡ ô	TWA		0			nS
$\overline{\text{IOW}}$ width	TWW		60			nS
Data setup time to $\overline{\text{IOW}}$ ¡ ô	TDW		60			nS
Data hold time from $\overline{\text{IOW}}$ ¡ ô	TWD		0			nS
IRQ delay from $\overline{\text{IOW}}$ ¡ ô	TWI				360/570 /675	nS
DRQ cycle time	TMCY		27			µS
DRQ delay time $\overline{\text{DACK}}$ ¡ õ	TAM				50	nS
DRQ to $\overline{\text{DACK}}$ delay	TMA		0			nS
$\overline{\text{DACK}}$ width	TAA		260/430 /510			nS
$\overline{\text{IOR}}$ delay from $\overline{\text{DRQ}}$	TMR		0			nS
$\overline{\text{IOW}}$ delay from $\overline{\text{DRQ}}$	TMW		0			nS

12.3.1 AC Characteristics, FDC continued

PARAMETER	SYM.	TEST CONDITIONS	MIN.	TYP. (NOTE 1)	MAX.	UNIT
$\overline{\text{IOW}}$ or $\overline{\text{IOR}}$ response time from DRQ	TMRW			6/12 /20/24		μS
TC width	TTC		135/220 /260			nS
RESET width	TRST		1.8/3/3.5			μS
$\overline{\text{INDEX}}$ width	TIDX		0.5/0.9 /1.0			μS
$\overline{\text{DIR}}$ setup time to $\overline{\text{STEP}}$	TDST		1.0/1.6 /2.0			μS
$\overline{\text{DIR}}$ hold time from $\overline{\text{STEP}}$	TSTD		24/40/48			μS
$\overline{\text{STEP}}$ pulse width	TSTP		6.8/11.5 /13.8	7/11.7 /14	7.2/11.9 /14.2	μS
$\overline{\text{STEP}}$ cycle width	TSC		Note 2	Note 2	Note 2	μS
$\overline{\text{WD}}$ pulse width	TWDD		100/185 /225	125/210 /250	150/235 /275	μS
Write precompensation	TWPC		100/138 /225	125/210 /250	150/235 /275	μS

Notes:

1. Typical values for T = 25° C and normal supply voltage.

2. Programmable from 2 mS through 32 mS in 2 mS increments.

12.3.2 UART/Parallel Port

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	MAX.	UNIT
Delay from Stop to Set Interrupt	TSINT		9/16		Baud Rate
Delay from $\overline{\mathrm{IOR}}$ Reset Interrupt	TRINT	100 pf Loading		1	µS
Delay from Initial IRQ Reset to Transmit Start	TIRS		1/16	8/16	Baud Rate
Delay from $\overline{\mathrm{IOW}}$ to Reset interrupt	THR	100 pf Loading		175	nS
Delay from Initial $\overline{\mathrm{IOW}}$ to interrupt	TSI		9/16	16/16	Baud Rate
Delay from Stop to Set Interrupt	TSTI			1/2	Baud Rate
Delay from $\overline{\mathrm{IOR}}$ to Reset Interrupt	TIR	100 pF Loading		250	nS
Delay from $\overline{\mathrm{IOR}}$ to Output	TMWO	100 pF Loading		200	nS
Set Interrupt Delay from Modem Input	TSIM			250	nS
Reset Interrupt Delay from $\overline{\mathrm{IOR}}$	TRIM			250	nS
Interrupt Active Delay	TIAD	100 pF Loading		25	nS
Interrupt Inactive Delay	TIID	100 pF Loading		30	nS
Baud Divisor	N	100 pF Loading		$2^{16}-1$	

12.3.3 Parallel Port Mode Parameters

PARAMETER	SYM.	MIN.	TYP.	MAX.	UNIT
PD0-7, $\overline{\mathrm{INDEX}}$, $\overline{\mathrm{STROBE}}$, $\overline{\mathrm{AUTOFD}}$ Delay from $\overline{\mathrm{IOW}}$	t1			100	nS
IRQ Delay from $\overline{\mathrm{ACK}}$, nFAULT	t2			60	nS
IRQ Delay from $\overline{\mathrm{IOW}}$	t3			105	nS
IRQ Active Low in ECP and EPP Modes	t4	200		300	nS
$\overline{\mathrm{ERROR}}$ Active to IRQ Active	t5			105	nS

12.3.4 EPP Data or Address Read Cycle Timing Parameters

PARAMETER	SYM.	MIN.	MAX.	UNIT
Ax Valid to $\overline{\text{IOR}}$ Asserted	t1	40		nS
IOCHRDY Deasserted to $\overline{\text{IOR}}$ Deasserted	t2	0		nS
$\overline{\text{IOR}}$ Deasserted to Ax Valid	t3	10	10	nS
$\overline{\text{IOR}}$ Deasserted to $\overline{\text{IOW}}$ or $\overline{\text{IOR}}$ Asserted	t4	40		
$\overline{\text{IOR}}$ Asserted to IOCHRDY Asserted	t5	0	24	nS
PD Valid to SD Valid	t6	0	75	nS
$\overline{\text{IOR}}$ Deasserted to SD Hi-Z (Hold Time)	t7	0	40	µS
SD Valid to IOCHRDY Deasserted	t8	0	85	nS
$\overline{\text{WAIT}}$ Deasserted to IOCHRDY Deasserted	t9	60	160	nS
PD Hi-Z to PDBIR Set	t10	0		nS
$\overline{\text{WRITE}}$ Deasserted to $\overline{\text{IOR}}$ Asserted	t13	0		nS
$\overline{\text{WAIT}}$ Asserted to $\overline{\text{WRITE}}$ Deasserted	t14	0	185	nS
Deasserted to $\overline{\text{WRITE}}$ Modified	t15	60	190	nS
$\overline{\text{IOR}}$ Asserted to PD Hi-Z	t16	0	50	nS
$\overline{\text{WAIT}}$ Asserted to PD Hi-Z	t17	60	180	nS
Command Asserted to PD Valid	t18	0		nS
Command Deasserted to PD Hi-Z	t19	0		nS
$\overline{\text{WAIT}}$ Deasserted to PD Drive	t20	60	190	nS
$\overline{\text{WRITE}}$ Deasserted to Command	t21	1		nS
PBDIR Set to Command	t22	0	20	nS
PD Hi-Z to Command Asserted	t23	0	30	nS
Asserted to Command Asserted	t24	0	195	nS
$\overline{\text{WAIT}}$ Deasserted to Command Deasserted	t25	60	180	nS
Time out	t26	10	12	nS
PD Valid to $\overline{\text{WAIT}}$ Deasserted	t27	0		nS
PD Hi-Z to $\overline{\text{WAIT}}$ Deasserted	t28	0		µS

12.3.5 EPP Data or Address Write Cycle Timing Parameters

PARAMETER	SYM.	MIN.	MAX.	UNIT
Ax Valid to $\overline{\text{IOW}}$ Asserted	t1	40		nS
SD Valid to Asserted	t2	10		nS
$\overline{\text{IOW}}$ Deasserted to Ax Invalid	t3	10		nS
$\overline{\text{WAIT}}$ Deasserted to IOCHRDY Deasserted	t4	0		nS
Command Asserted to $\overline{\text{WAIT}}$ Deasserted	t5	10		nS
$\overline{\text{IOW}}$ Deasserted to $\overline{\text{IOW}}$ or $\overline{\text{IOR}}$ Asserted	t6	40		nS
IOCHRDY Deasserted to $\overline{\text{IOW}}$ Deasserted	t7	0	24	nS
$\overline{\text{WAIT}}$ Asserted to Command Asserted	t8	60	160	nS
$\overline{\text{IOW}}$ Asserted to $\overline{\text{WAIT}}$ Asserted	t9	0	70	nS
PBDIR Low to $\overline{\text{WRITE}}$ Asserted	t10	0		nS
$\overline{\text{WAIT}}$ Asserted to $\overline{\text{WRITE}}$ Asserted	t11	60	185	nS
$\overline{\text{WAIT}}$ Asserted to $\overline{\text{WRITE}}$ Change	t12	60	185	nS
$\overline{\text{IOW}}$ Asserted to PD Valid	t13	0	50	nS
$\overline{\text{WAIT}}$ Asserted to PD Invalid	t14	0		nS
PD Invalid to Command Asserted	t15	10		nS
$\overline{\text{IOW}}$ to Command Asserted	t16	5	35	nS
$\overline{\text{WAIT}}$ Asserted to Command Asserted	t17	60	210	nS
$\overline{\text{WAIT}}$ Deasserted to Command Deasserted	t18	60	190	nS
Command Asserted to $\overline{\text{WAIT}}$ Deasserted	t19	0	10	µS
Time out	t20	10	12	µS
Command Deasserted to $\overline{\text{WAIT}}$ Asserted	t21	0		nS
$\overline{\text{IOW}}$ Deasserted to $\overline{\text{WRITE}}$ Deasserted and PD invalid	t22	0		nS

12.3.6 Parallel Port FIFO Timing Parameters

PARAMETER	SYMBOL	MIN.	MAX.	UNIT
DATA Valid to nSTROBE Active	t1	600		nS
nSTROBE Active Pulse Width	t2	600		nS
DATA Hold from nSTROBE Inactive	t3	450		nS
BUSY Inactive to PD Inactive	t4	80		nS
BUSY Inactive to nSTROBE Active	t5	680		nS
nSTROBE Active to BUSY Active	t6		500	nS

12.3.7 ECP Parallel Port Forward Timing Parameters

PARAMETER	SYMBOL	MIN.	MAX.	UNIT
nAUTOFD Valid to nSTROBE Asserted	t1	0	60	nS
PD Valid to nSTROBE Asserted	t2	0	60	nS
BUSY Deasserted to nAUTOFD Changed	t3	80	180	nS
BUSY Deasserted to PD Changed	t4	80	180	nS
nSTROBE Deasserted to BUSY Deasserted	t5	0		nS
BUSY Deasserted to nSTROBE Asserted	t6	80	200	nS
nSTROBE Asserted to BUSY Asserted	t7	0		nS
BUSY Asserted to nSTROBE Deasserted	t8	80	180	nS

12.3.8 ECP Parallel Port Reverse Timing Parameters

PARAMETER	SYMBOL	MIN.	MAX.	UNIT
PD Valid to nACK Asserted	t1	0		nS
nAUTOFD Deasserted to PD Changed	t2	0		nS
nAUTOFD Asserted to nACK Asserted	t3	0		nS
nAUTOFD Deasserted to nACK Deasserted	t4	0		nS
nACK Deasserted to nAUTOFD Asserted	t5	80	200	nS
PD Changed to nAUTOFD Deasserted	t6	80	200	nS

12.3.9 KBC Timing Parameters

NO.	DESCRIPTION	MIN.	MAX.	UNIT
T1	Address Setup Time from WRB	0		nS
T2	Address Setup Time from RDB	0		nS
T3	WRB Strobe Width	20		nS
T4	RDB Strobe Width	20		nS
T5	Address Hold Time from WRB	0		nS
T6	Address Hold Time from RDB	0		nS
T7	Data Setup Time	50		nS
T8	Data Hold Time	0		nS
T9	Gate Delay Time from WRB	10	30	nS
T10	RDB to Drive Data Delay		40	nS
T11	RDB to Floating Data Delay	0	20	nS
T12	Data Valid After Clock Falling (SEND)		4	µS
T13	K/B Clock Period	20		µS
T14	K/B Clock Pulse Width	10		µS
T15	Data Valid Before Clock Falling (RECEIVE)	4		µS
T16	K/B ACK After Finish Receiving	20		µS
T17	RC Fast Reset Pulse Delay (8 Mhz)	2	3	µS
T18	RC Pulse Width (8 Mhz)	6		µS
T19	Transmit Timeout		2	mS
T20	Data Valid Hold Time	0		µS
T21	Input Clock Period (6–12 Mhz)	83	167	nS
T22	Duration of CLK inactive	30	50	µS
T23	Duration of CLK active	30	50	µS
T24	Time from inactive CLK transition, used to time when the auxiliary device sample DATA	5	25	µS
T25	Time of inhibit mode	100	300	µS
T26	Time from rising edge of CLK to DATA transition	5	T28-5	µS
T27	Duration of CLK inactive	30	50	µS
T28	Duration of CLK active	30	50	µS
T29	Time from DATA transition to falling edge of CLK	5	25	µS

12.3.10 GPIO Timing Parameters

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
t_{WGO}	Write data to GPIO update		300(Note 1)	ns

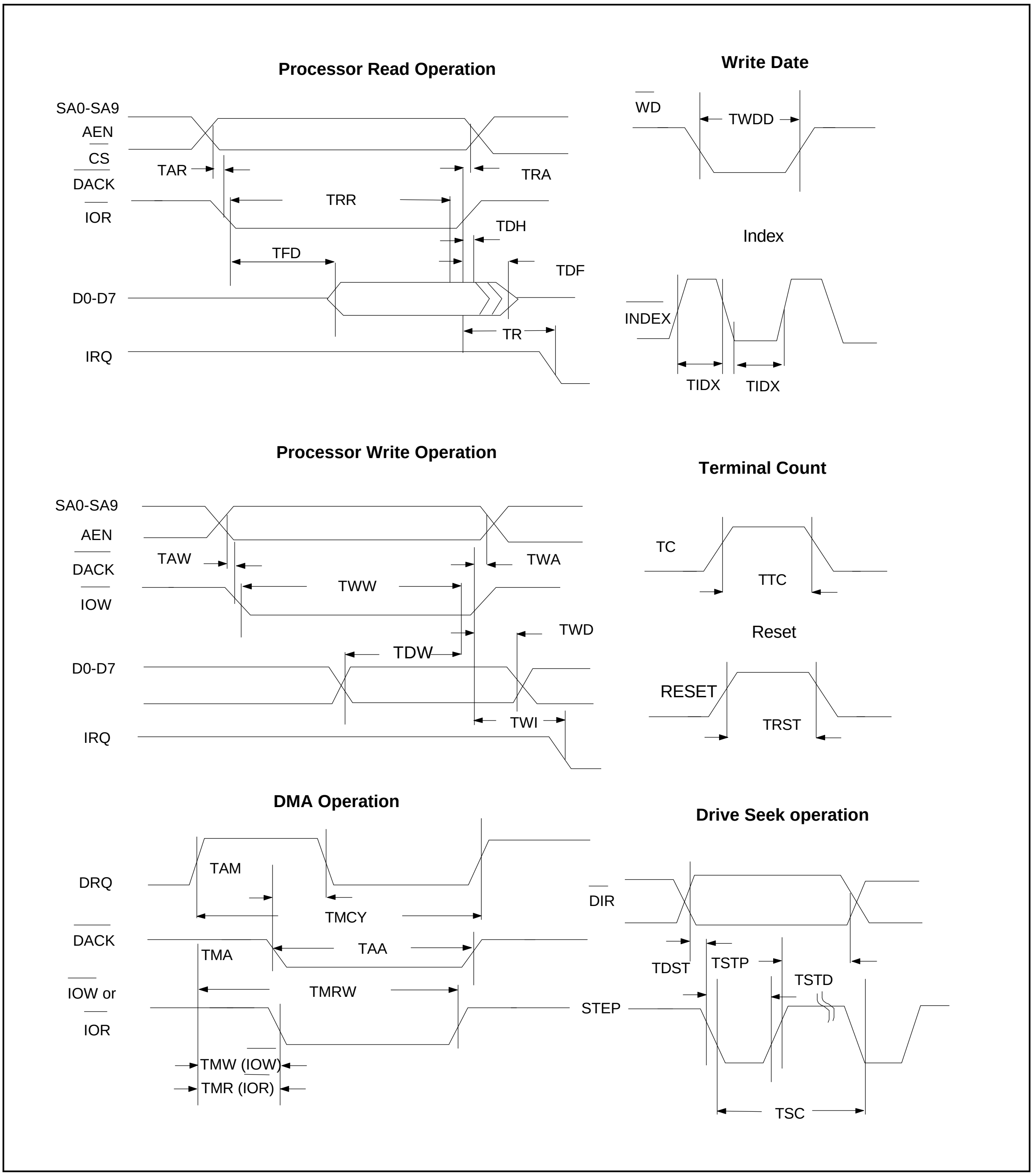
Note : Refer to Microprocessor Interface Timing for Read Timing.

12.3.11 Keyboard/Mouse Timing Parameters

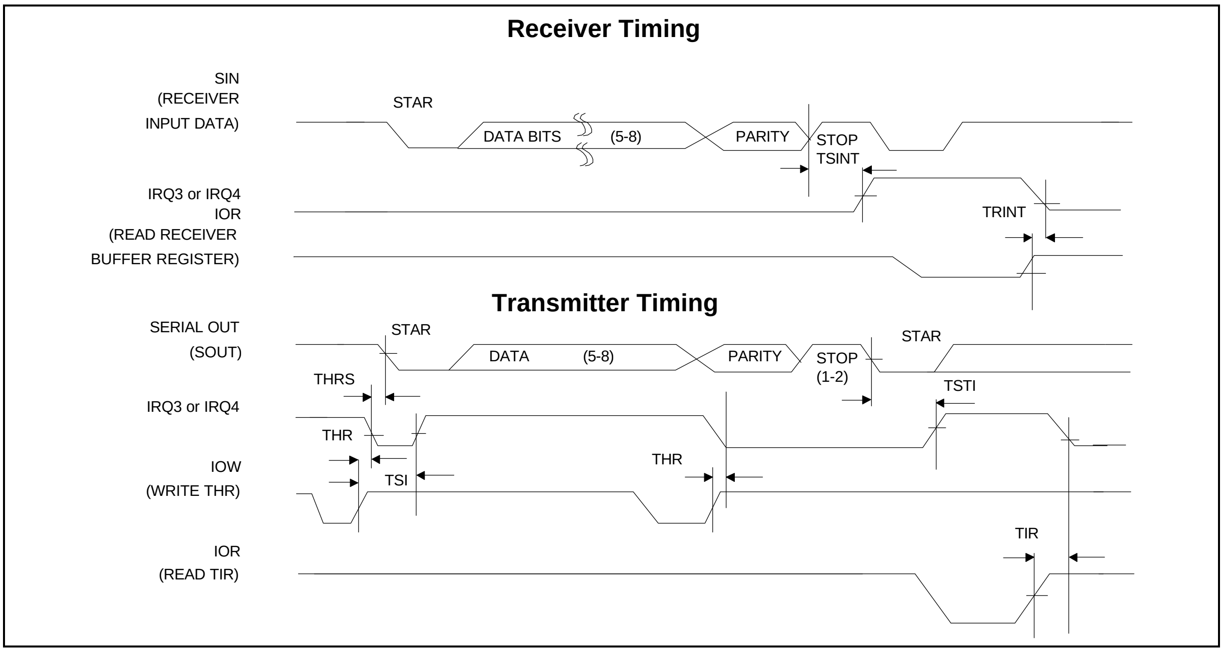
SYMBOL	PARAMETER	MIN.	MAX.	UNIT
t_{SWL}	$\overline{\text{PANSWIN}}$ falling edge to $\overline{\text{PANSWOUT}}$ falling edge		20	ns
t_{SWH}	$\overline{\text{PANSWIN}}$ falling edge to $\overline{\text{PANSWOUT}}$ Hi-Z		50	ns
t_{WKUPD}	KCLK/MCLK falling edge to $\overline{\text{PANSWOUT}}$ falling edge delay		200	ns
t_{WKUPW}	$\overline{\text{PANSWOUT}}$ active pulse width	0.5	1	sec

13.0 TIMING WAVEFORMS

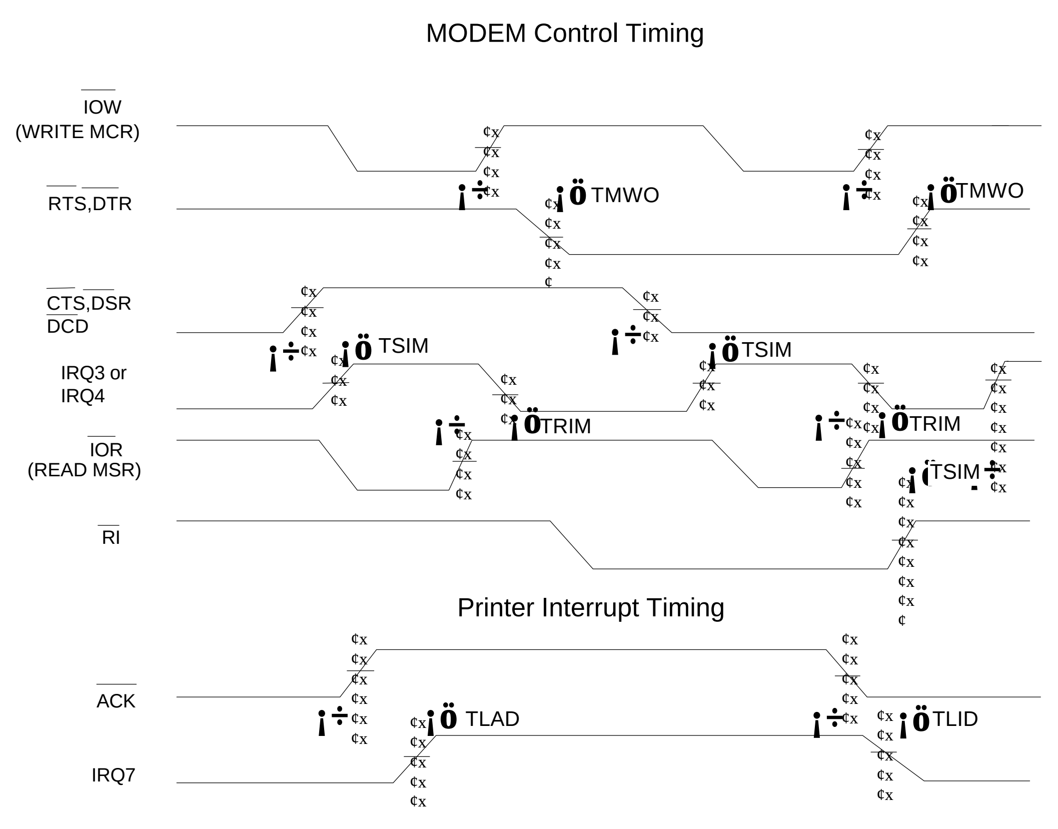
13.1 FDC


Processor Read Operation
SA0-SA9
AEN
CS
DACK
IOR
D0-D7
IRQ
TAR
TRA
TRR
TDH
TFD
TDF
TR
Write Date
WD
TWDD
Index
INDEX
TIDX
TIDX
Processor Write Operation
SA0-SA9
AEN
DACK
IOW
D0-D7
IRQ
TAW
TWA
TWW
TWD
TDW
TWI
Terminal Count
TC
TTC
Reset
RESET
TRST
DMA Operation
DRQ
DACK
IOW or
IOR
TAM
TMCY
TMA
TAA
TMRW
TMW (IOW)
TMR (IOR)
Drive Seek operation
DIR
STEP
TDST
TSTP
TSTD
TSC

13.2 UART/Parallel

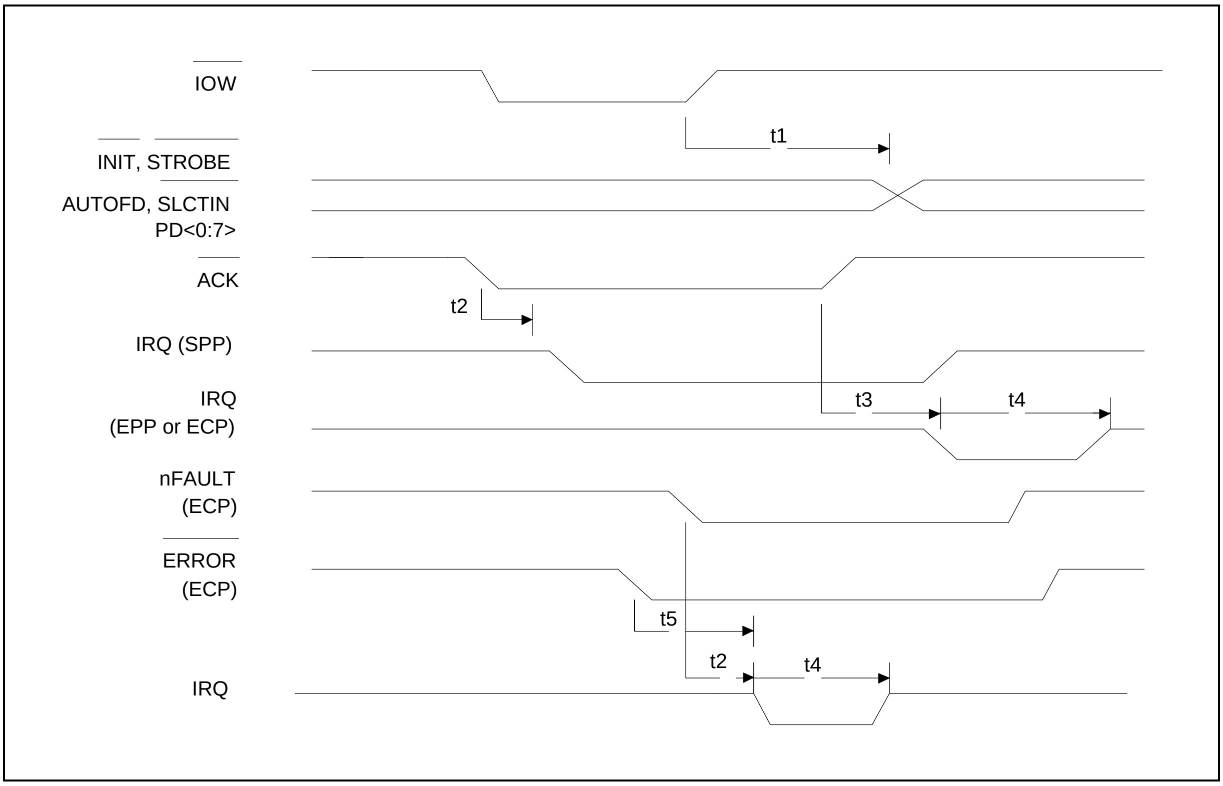

Receiver Timing
SIN
(RECEIVER
INPUT DATA)
STAR
DATA BITS
(5-8)
PARITY
STOP
TSINT
IRQ3 or IRQ4
IOR
(READ RECEIVER
BUFFER REGISTER)
TRINT
Transmitter Timing
SERIAL OUT
(SOUT)
STAR
DATA
(5-8)
PARITY
STOP
(1-2)
STAR
THRS
TSTI
IRQ3 or IRQ4
THR
IOW
(WRITE THR)
TSI
THR
IOR
(READ TIR)
TIR

13.2.1 Modem Control Timing

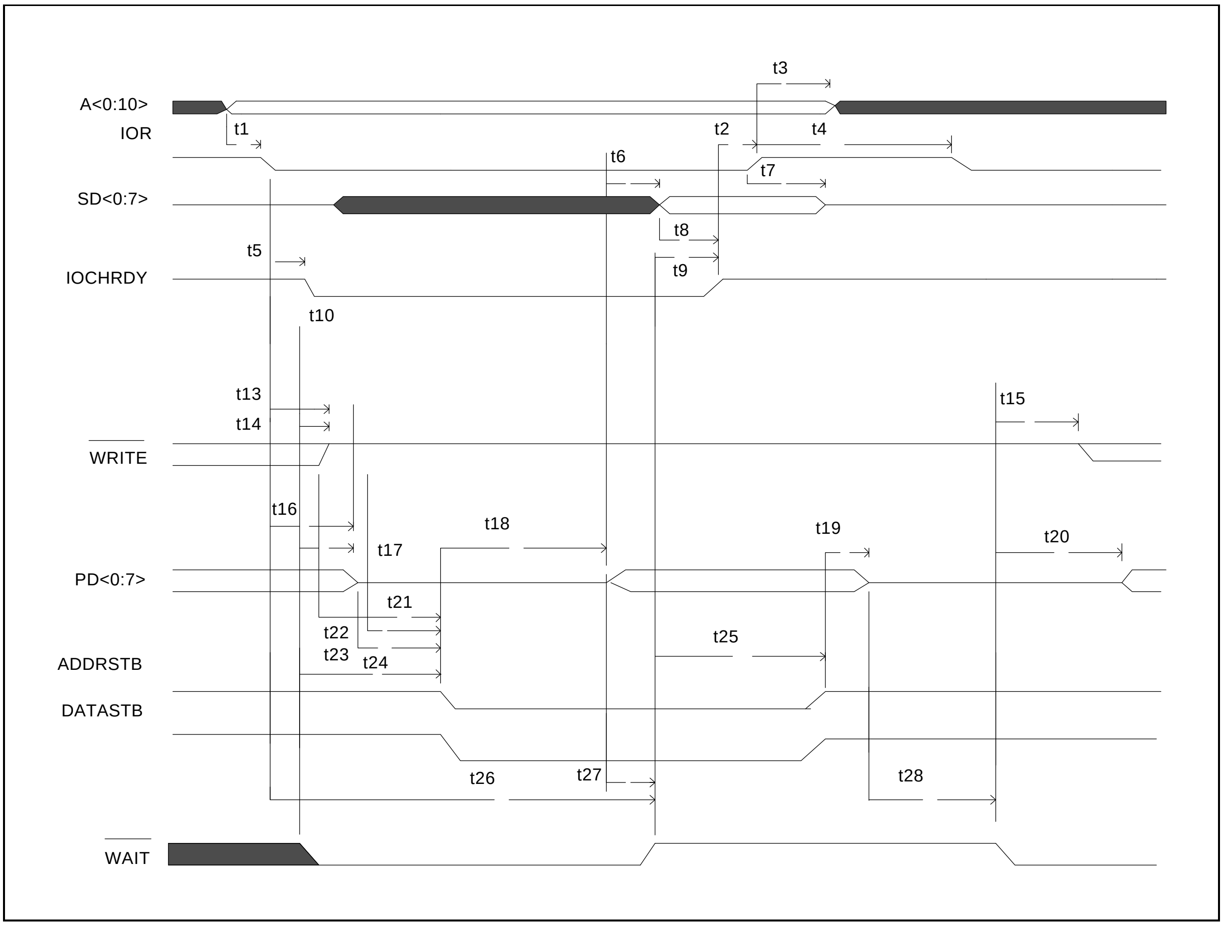

MODEM Control Timing
IOW
(WRITE MCR)
RTS,DTR
CTS,DSR
DCD
IRQ3 or
IRQ4
IOR
(READ MSR)
RI
TMWO
TSIM
TRIM
Printer Interrupt Timing
ACK
IRQ7
TLAD
TLID

13.3 Parallel Port

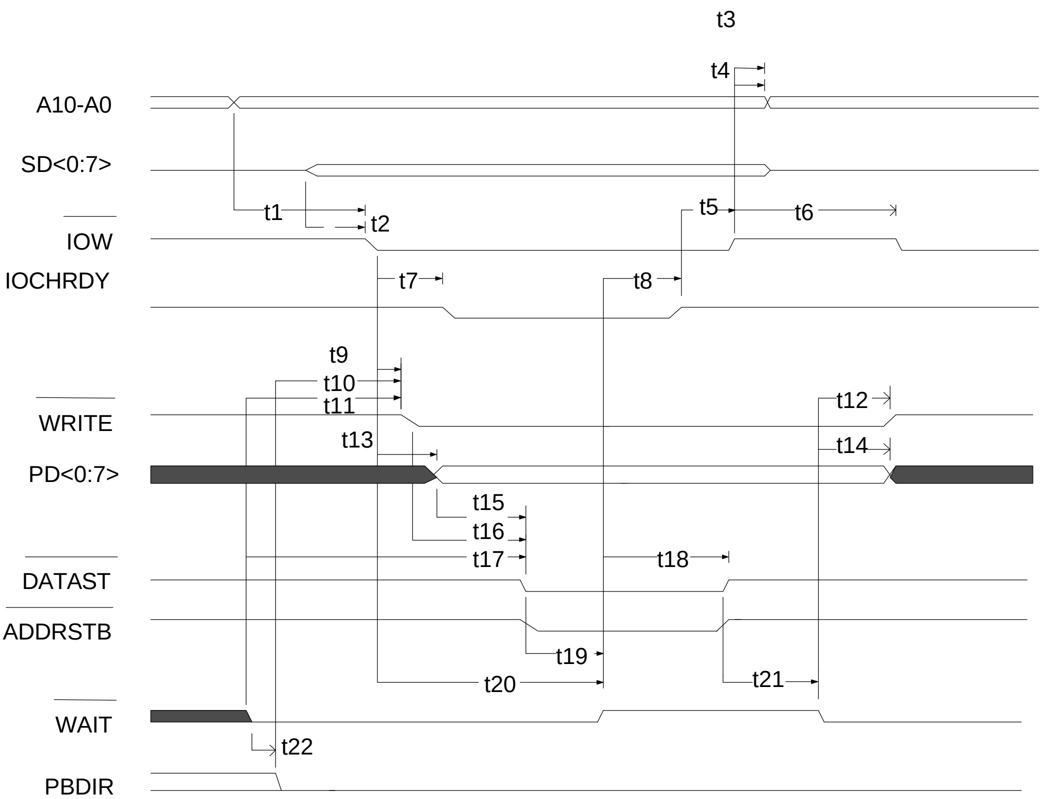
13.3.1 Parallel Port Timing


IOW
t1
INIT, STROBE
AUTOFD, SLCTIN
PD<0:7>
ACK
t2
IRQ (SPP)
IRQ
(EPP or ECP)
t3
t4
nFAULT
(ECP)
ERROR
(ECP)
t5
t2
t4
IRQ

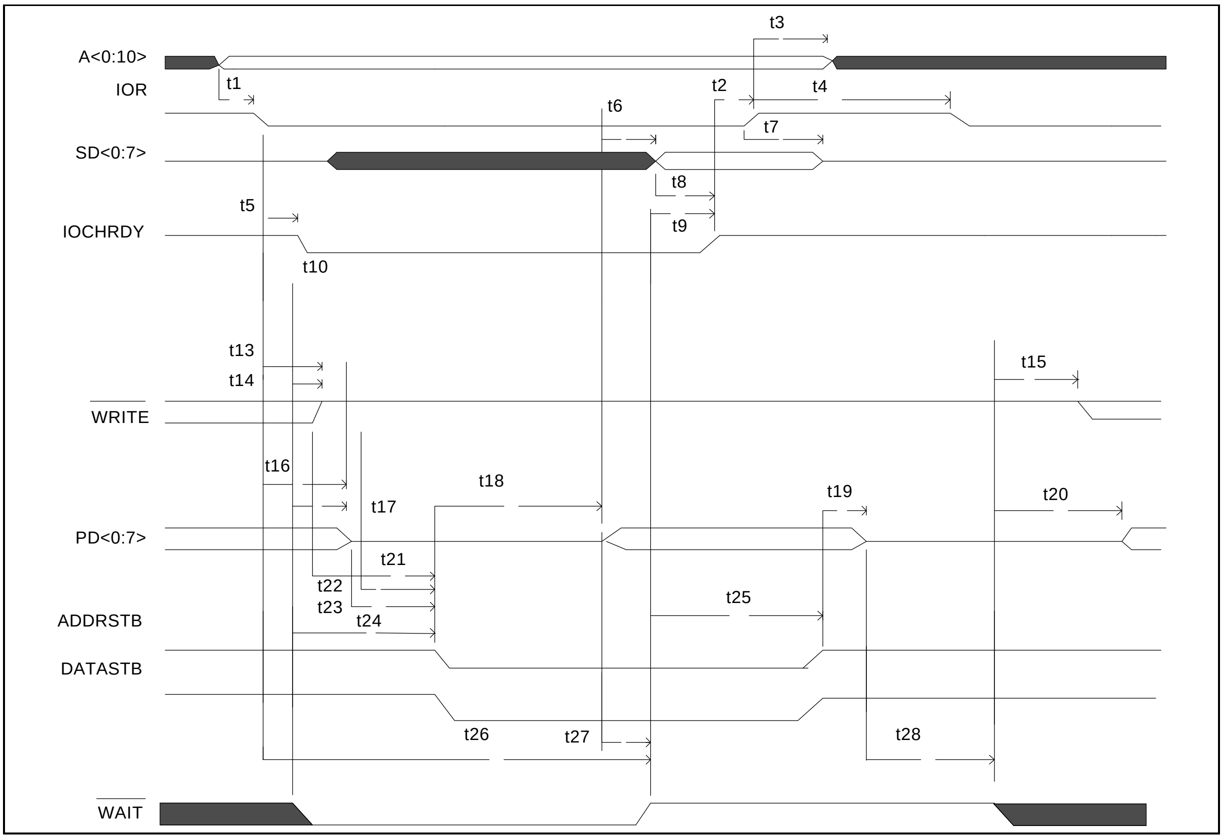
13.3.2 EPP Data or Address Read Cycle (EPP Version 1.9)


A<0:10>
IOR
SD<0:7>
IOCHRDY
WRITE
PD<0:7>
ADDRSTB
DATASTB
WAIT
t1
t2
t3
t4
t5
t6
t7
t8
t9
t10
t13
t14
t15
t16
t17
t18
t19
t20
t21
t22
t23
t24
t25
t26
t27
t28

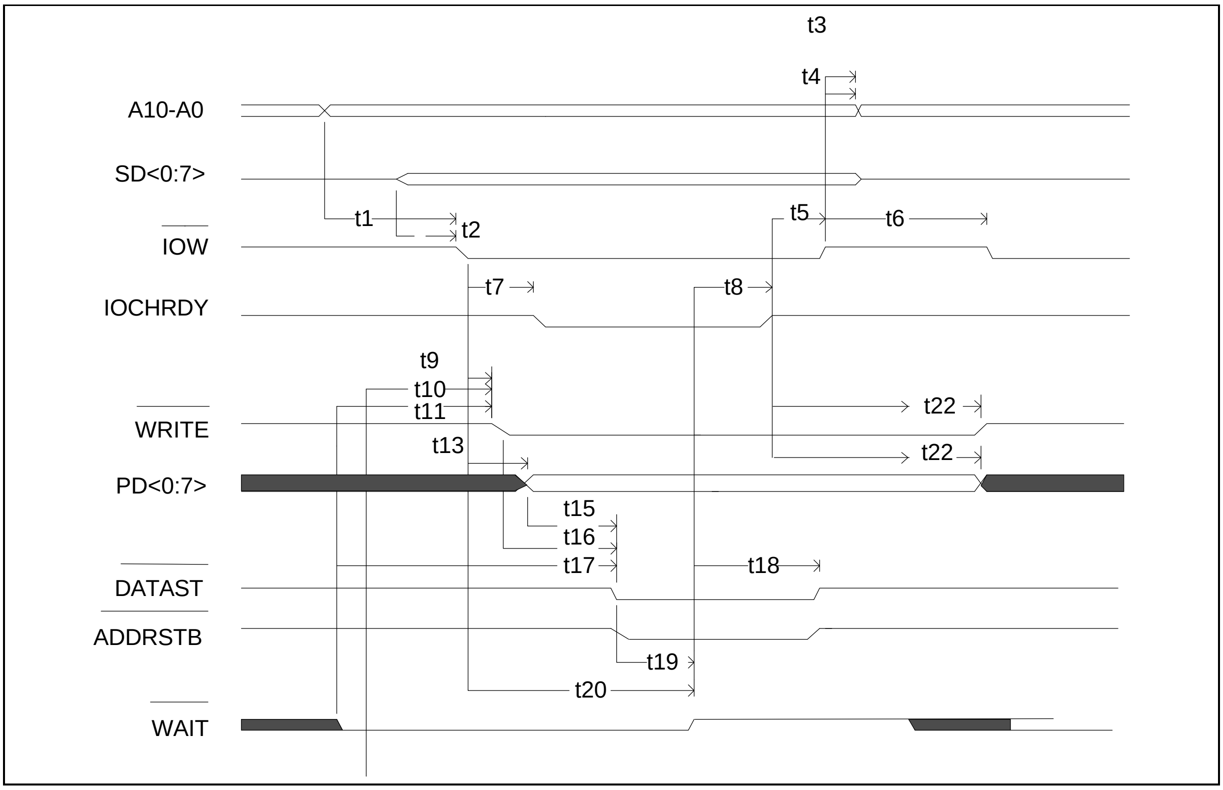
13.3.3 EPP Data or Address Write Cycle (EPP Version 1.9)


t3
t4
A10-A0
SD<0:7>
t1
t2
t5
t6
IOW
IOCHRDY
t7
t8
t9
t10
t11
t12
WRITE
t13
t14
PD<0:7>
t15
t16
t17
t18
DATAST
ADDRSTB
t19
t20
t21
WAIT
t22
PBDIR

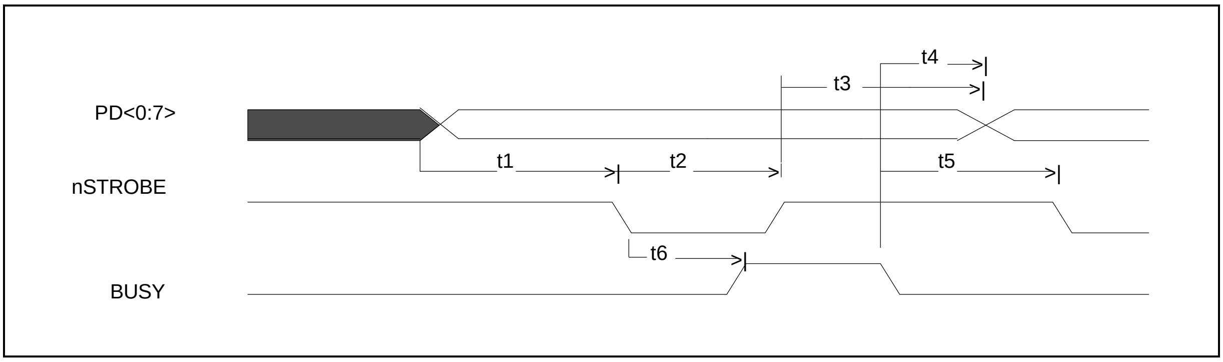
13.3.4 EPP Data or Address Read Cycle (EPP Version 1.7)


A<0:10>
IOR
SD<0:7>
IOCHRDY
WRITE
PD<0:7>
ADDRSTB
DATASTB
WAIT
t1
t2
t3
t4
t5
t6
t7
t8
t9
t10
t13
t14
t15
t16
t17
t18
t19
t20
t21
t22
t23
t24
t25
t26
t27
t28

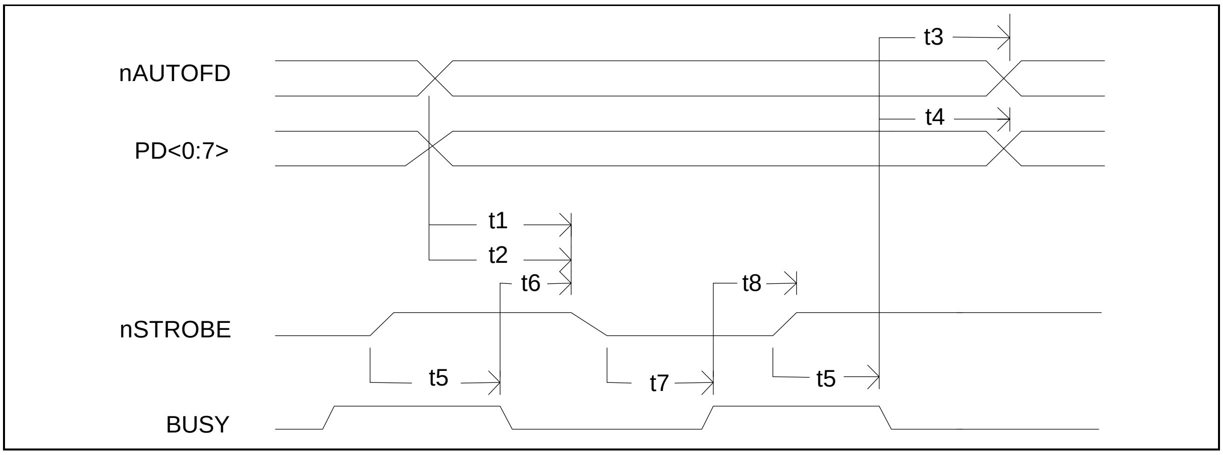
13.3.5 EPP Data or Address Write Cycle (EPP Version 1.7)


t3
t4
A10-A0
SD<0:7>
t1
t2
t5
t6
IOW
t7
t8
IOCHRDY
t9
t10
t11
t22
WRITE
t13
t22
PD<0:7>
t15
t16
t17
t18
DATAST
ADDRSTB
t19
t20
WAIT

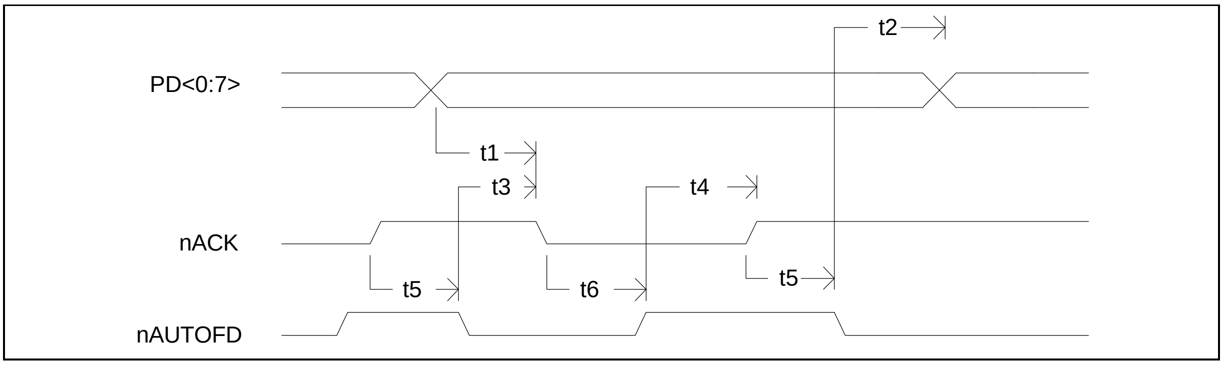
13.3.6 Parallel Port FIFO Timing


t4
t3
PD<0:7>
t1
t2
t5
nSTROBE
t6
BUSY

13.3.7 ECP Parallel Port Forward Timing

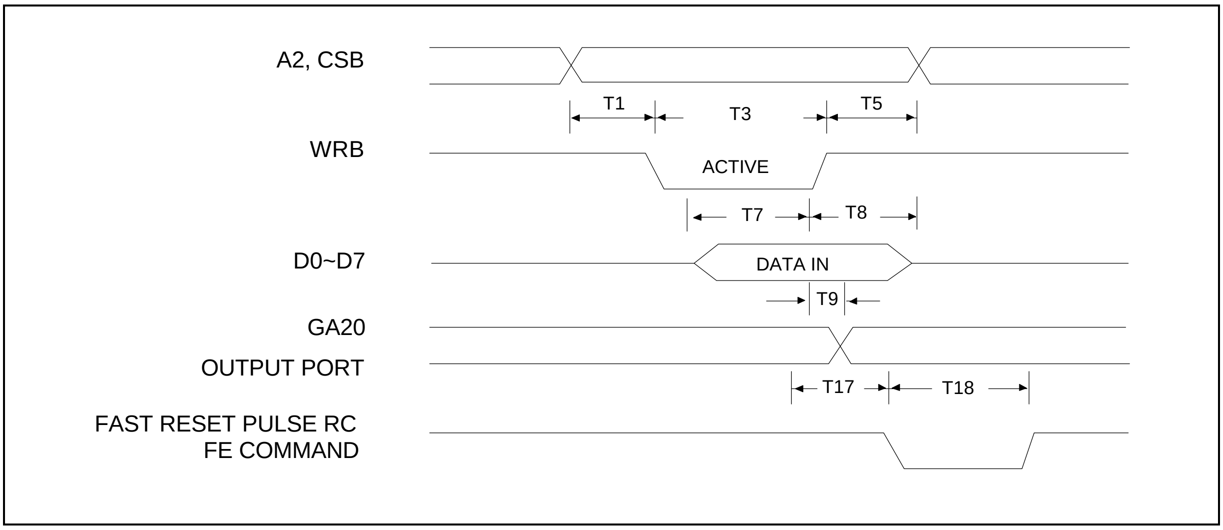

nAUTOFD
PD<0:7>
nSTROBE
BUSY
t1
t2
t3
t4
t5
t6
t7
t8
t5

13.3.8 ECP Parallel Port Reverse Timing

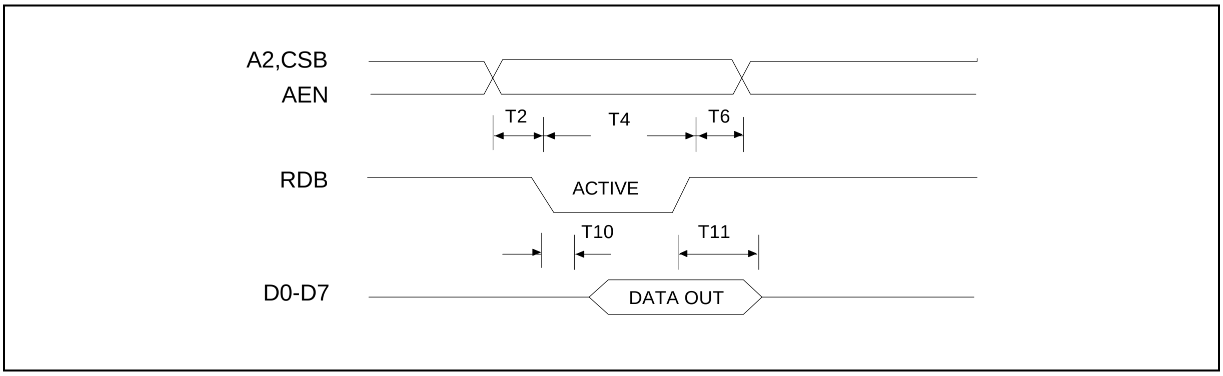

PD<0:7>
nACK
nAUTOFD
t1
t2
t3
t4
t5
t6
t5

13.4 KBC

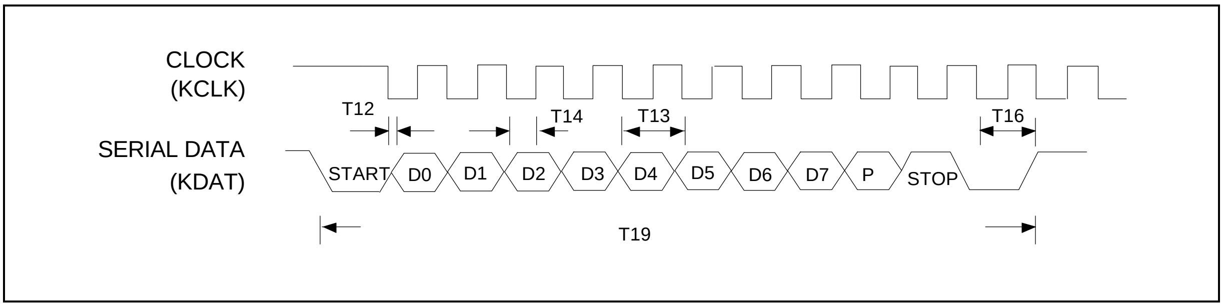
13.4.1 Write Cycle Timing


A2, CSB
T1
T3
T5
WRB
ACTIVE
T7
T8
D0~D7
DATA IN
T9
GA20
OUTPUT PORT
T17
T18
FAST RESET PULSE RC
FE COMMAND

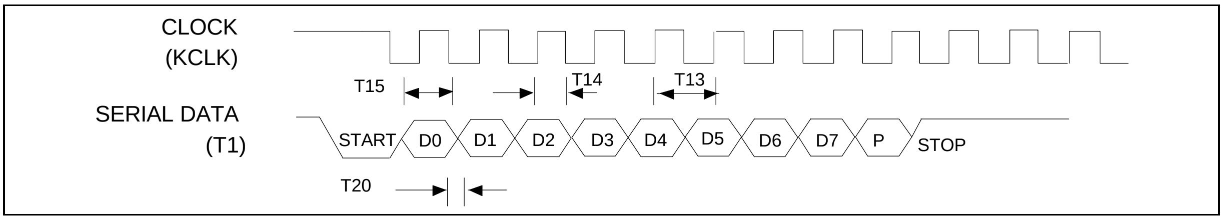
13.4.2 Read Cycle Timing


A2,CSB
AEN
T2
T4
T6
RDB
ACTIVE
T10
T11
D0-D7
DATA OUT

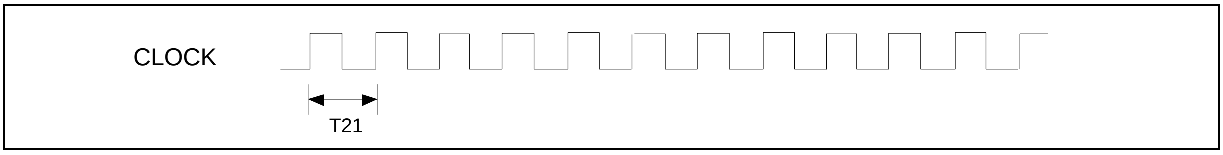
13.4.3 Send Data to K/B


CLOCK
(KCLK)
T12
T14
T13
T16
SERIAL DATA
(KDAT)
START
D0
D1
D2
D3
D4
D5
D6
D7
P
STOP
T19

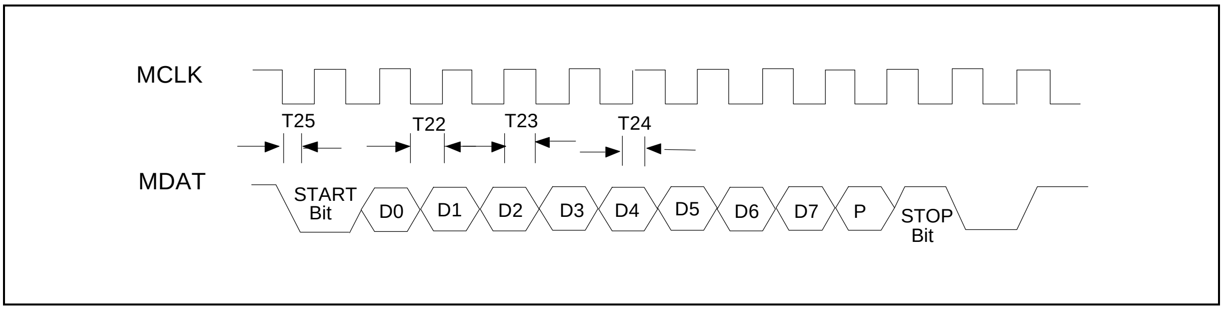
13.4.4 Receive Data from K/B


CLOCK
(KCLK)
T15
T14
T13
SERIAL DATA
(T1)
START
D0
D1
D2
D3
D4
D5
D6
D7
P
STOP
T20

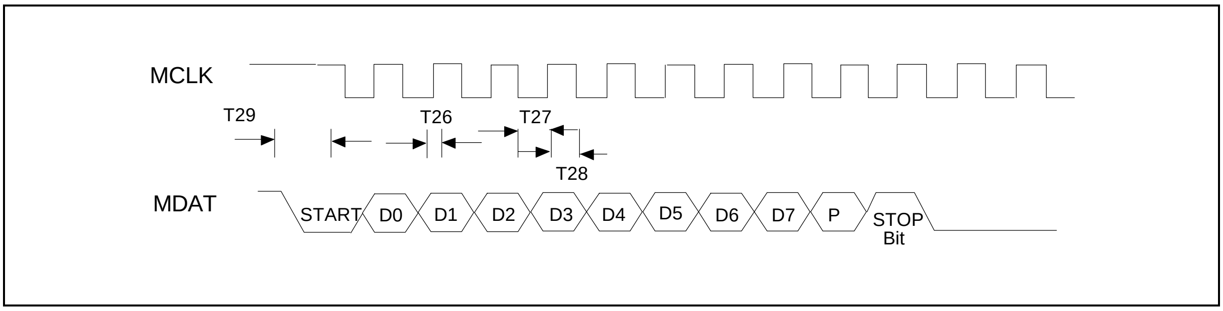
13.4.5 Input Clock



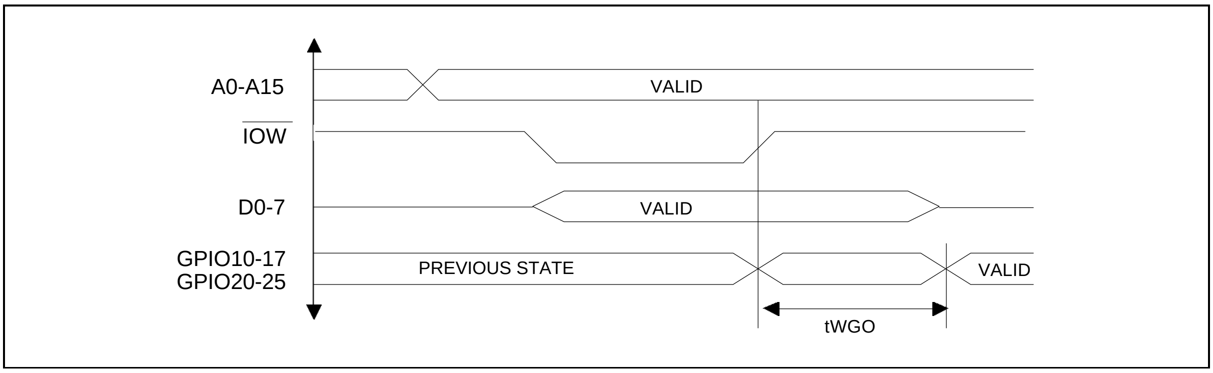
13.4.6 Send Data to Mouse


MCLK
T25
T22
T23
T24
MDAT
START
Bit
D0
D1
D2
D3
D4
D5
D6
D7
P
STOP
Bit

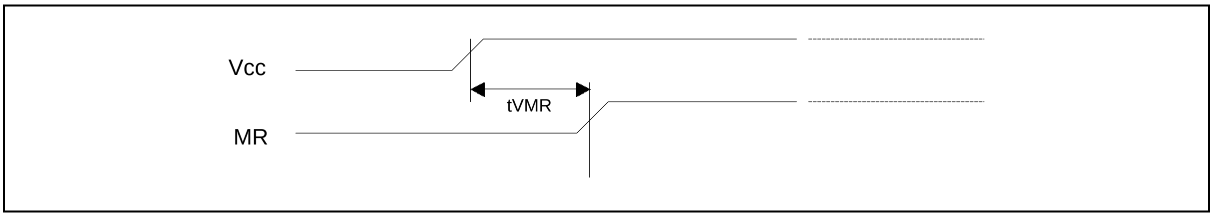
13.4.7 Receive Data from Mouse


MCLK
T29
T26
T27
T28
MDAT
START
D0
D1
D2
D3
D4
D5
D6
D7
P
STOP
Bit

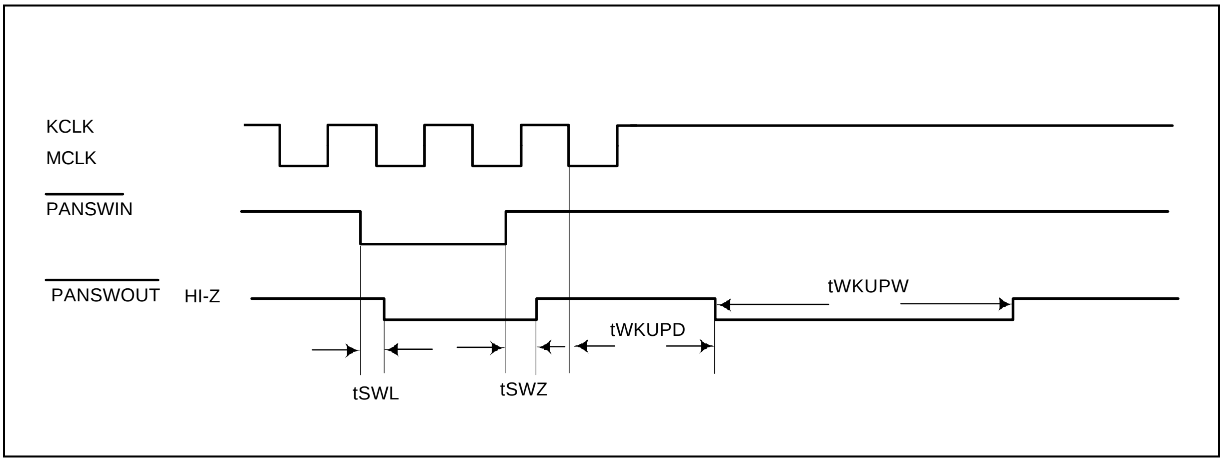
13.5 GPIO Write Timing Diagram


A0-A15
VALID
IOW
D0-7
VALID
GPIO10-17
GPIO20-25
PREVIOUS STATE
VALID
tWGO

13.6 Master Reset (MR) Timing

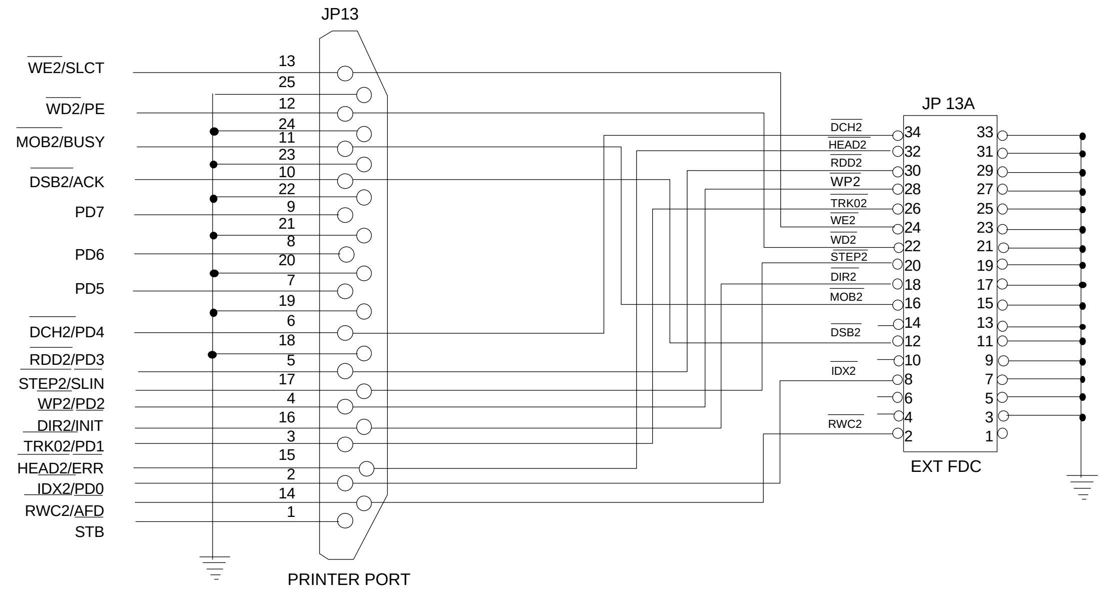


13.7 Keyboard/Mouse Wake-up Timing


KCLK
MCLK
PANSWIN
PANSWOUT
HI-Z
tWKUPW
tWKUPD
tSWL
tSWZ

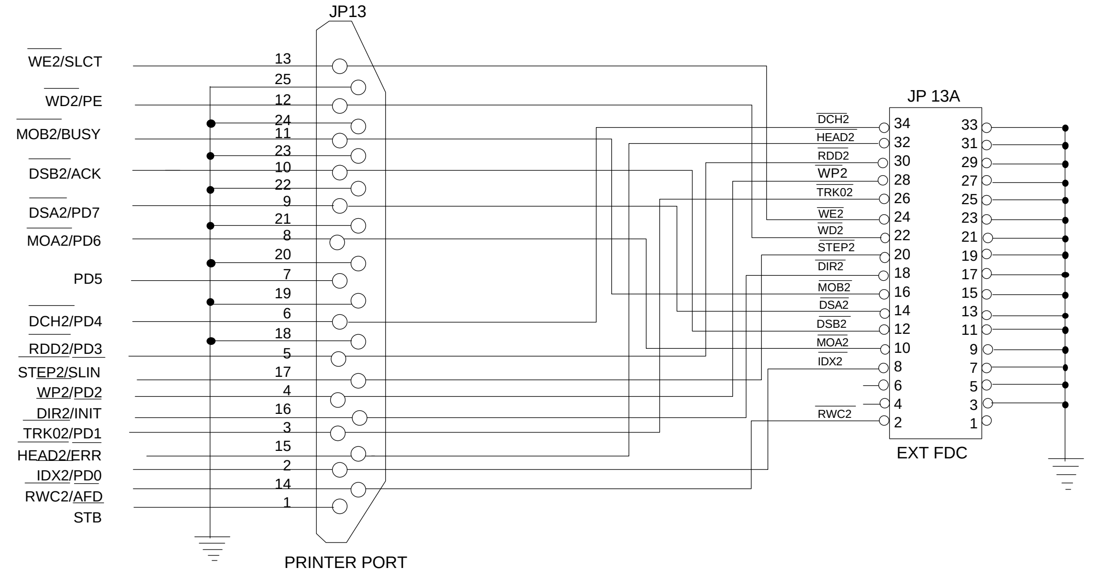
14.0 APPLICATION CIRCUITS

14.1 Parallel Port Extension FDD


JP13
WE2/SLCT
WD2/PE
MOB2/BUSY
DSB2/ACK
PD7
PD6
PD5
DCH2/PD4
RDD2/PD3
STEP2/SLIN
WP2/PD2
DIR2/INIT
TRK02/PD1
HEAD2/ERR
IDX2/PD0
RWC2/AFD
STB
13 25 12 24 11 23 10 22 9 21 8 20 7 19 6 18 5 17 4 16 3 15 2 14 1
PRINTER PORT
JP 13A
DCH2
HEAD2
RDD2
WP2
TRK02
WE2
WD2
STEP2
DIR2
MOB2
DSB2
IDX2
RWC2
34 32 30 28 26 24 22 20 18 16 14 12 10 8 6 4 2
33 31 29 27 25 23 21 19 17 15 13 11 9 7 5 3 1
EXT FDC

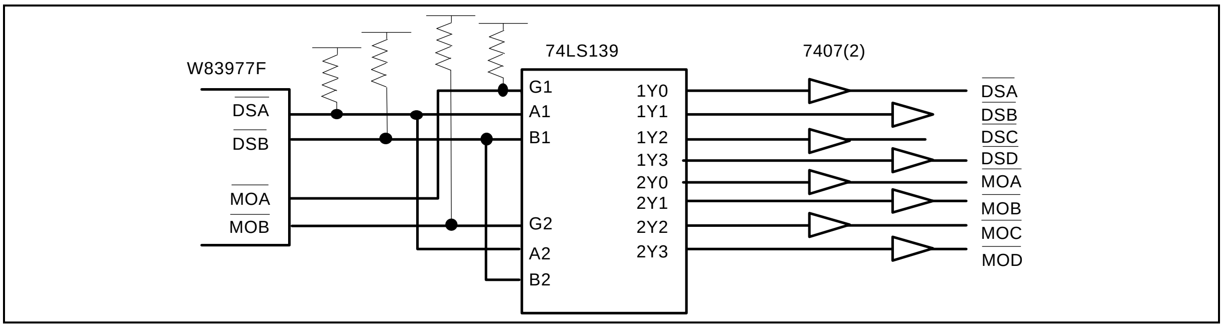
Parallel Port Extension FDD Mode Connection Diagram

14.2 Parallel Port Extension 2FDD


JP13
WE2/SLCT
WD2/PE
MOB2/BUSY
DSB2/ACK
DSA2/PD7
MOA2/PD6
PD5
DCH2/PD4
RDD2/PD3
STEP2/SLIN
WP2/PD2
DIR2/INIT
TRK02/PD1
HEAD2/ERR
IDX2/PD0
RWC2/AFD
STB
13 25 12 24 11 23 10 22 9 21 8 20 7 19 6 18 5 17 4 16 3 15 2 14 1
PRINTER PORT
JP 13A
DCH2
HEAD2
RDD2
WP2
TRK02
WE2
WD2
STEP2
DIR2
MOB2
DSA2
DSB2
MOA2
IDX2
RWC2
34 32 30 28 26 24 22 20 18 16 14 12 10 8 6 4 2
33 31 29 27 25 23 21 19 17 15 13 11 9 7 5 3 1
EXT FDC

Parallel Port Extension 2FDD Connection Diagram

14.3 Four FDD Mode

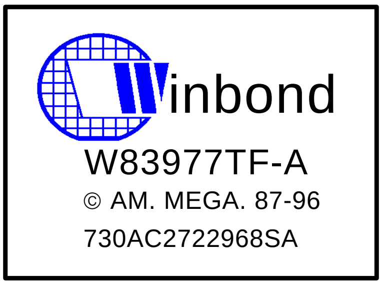

W83977F
DSA
DSB
MOA
MOB
74LS139
G1
A1
B1
G2
A2
B2
1Y0
1Y1
1Y2
1Y3
2Y0
2Y1
2Y2
2Y3
7407(2)
DSA
DSB
DSC
DSD
MOA
MOB
MOC
MOD

15.0 ORDERING INFORMATION

PART NO.	KBC FIRMWARE	REMARKS
W83977TF-P	Phoenix MultiKey/42^{TM}	
W83977TF-A	AMIKEY^{TM}-2	
W83977TF-PW	Phoenix MultiKey/42^{TM}	with OnNow / security keyboard wake-up
W83977TF-AW	AMIKEY^{TM}-2	with OnNow / security keyboard wake-up

16.0 HOW TO READ THE TOP MARKING

Example: The top marking of W83977TF-A


Winbond
W83977TF-A
© AM. MEGA. 87-96
730AC2722968SA

1st line: Winbond logo

2nd line: the type number: W83977TF-A

3rd line: the source of KBC F/W -- American Megatrends Incorporated^{TM}

4th line: the tracking code 730 A C 2 722968 SA

730: packages made in '97, week 30

A: assembly house ID; A means ASE, S means SPIL.... etc.

C: IC revision; B means version B, C means version C

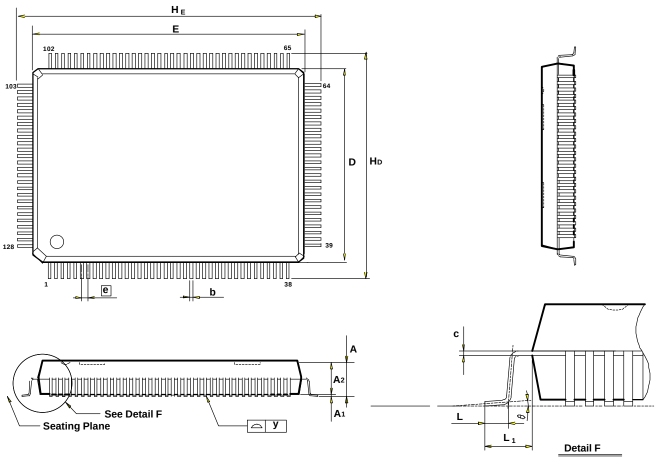
2: wafers manufactured in Winbond FAB 2

722968: wafer production series lot number

SA: if made by 0.5-um process: SA; otherwise by 0.6-um process: blank

17.0 PACKAGE DIMENSIONS

(128-pin PQFP)



Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A_1	0.25	0.35	0.45	0.010	0.014	0.018
A_2	2.57	2.72	2.87	0.101	0.107	0.113
b	0.10	0.20	0.30	0.004	0.008	0.012
c	0.10	0.15	0.20	0.004	0.006	0.008
D	13.90	14.00	14.10	0.547	0.551	0.555
E	19.90	20.00	20.10	0.783	0.787	0.791
e	—	0.50	—	—	0.020	—
H_D	17.00	17.20	17.40	0.669	0.677	0.685
H_E	23.00	23.20	23.40	0.905	0.913	0.921
L	0.65	0.80	0.95	0.025	0.031	0.037
L_1	—	1.60	—	—	0.063	—
y	—	—	0.08	—	—	0.003
θ	0	—	7	0	—	7

Note:

1. Dimension D & E do not include interlead flash.
2. Dimension b does not include dambar protrusion/intrusion .
3. Controlling dimension : Millimeter
4. General appearance spec. should be based on final visual inspection spec.
5. PCB layout please use the "mm".

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2730 Orchard Parkway
San Jose, CA 95134 U.S.A.
TEL: 1-408-9436666
FAX: 1-408-9436668

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