WD83B692

Ethernet Transceiver

WESTERN DIGITAL

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1.0 DESCRIPTION AND APPLICATION

The WD83B692 Ethernet Transceiver is a high-speed, bipolar line transmitter/receiver. The device includes analog transmit and receive buffers, a 10-MHz on-board oscillator, timing logic for jabber and heartbeat functions, output drivers, and a bandgap reference, in addition to a current reference and collision detector. The WD83B692 is pin-for-pin compatible with the National DP8392/NS32492 Coaxial Transceiver Interface (CTI).

The Ethernet Transceiver (ET) is used as a coaxial cable line transmitter/receiver for Ethernet/Cheapernet-type local area networks (LANs). In Ethernet applications, the ET is part of a transceiver media attachment unit (MAU) that connects directly to the coaxial transmission media and communicates with the data terminal equipment (DTE) through a transceiver cable, the attachment unit interface (AUI).

1.1 FEATURES

- Conforms to Ethernet II (10BASE5) and Cheapernet (10BASE2) IEEE 802.3 standards, including IEEE 802.3 reliability specifications and receive mode collision circuitry requirements
- Provides complete integration of transceiver function (except signal and power isolation)
- Requires minimal external components
- Contains on-board jabber function
- Provides combined noise rejection and squelch circuits for transmit and receive inputs
- Provides heartbeat disable to allow use in repeaters
- Incorporates high speed bipolar technology

2.0 THEORY OF OPERATION

This document describes the operation of the WD83B692 Ethernet Transceiver, and provides information on the following:

1. Receiver
2. Transmitter
3. Collision Signaling
4. Collision Detection
5. Jabber Function
6. Heartbeat Function

The WD83B692 is part of a three-device set that implements the complete 802.3 IEEE-compatible Ethernet network node electronics (see Figure 1-1). The WD83C690 Ethernet LAN controller (ELC) and the WD83C691 Ethernet Manchester encoder/decoder (MED) comprise the other two devices in the set. The ELC provides media access protocol functions and performs buffer management tasks, while the MED provides the Manchester encoding and decoding for transmission and data clock separation from received data.

Figure 1-1 shows the connection for Ethernet applications of the WD83B692 ET between the coaxial cable and the DTE.

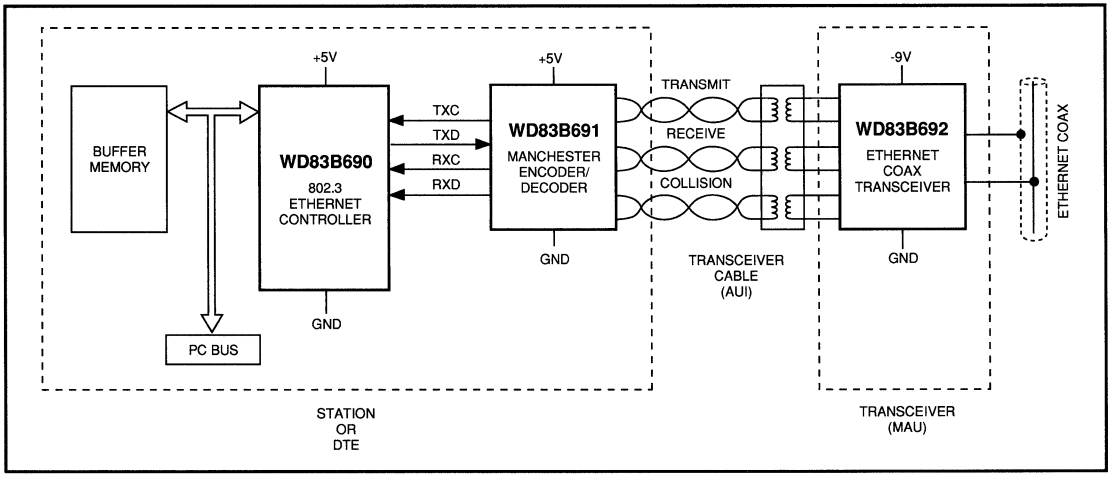

FIGURE 1-1. WD83B692 SYSTEM INTERFACE

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The coaxial transmitter is a current source driver with a controlled pulse waveform that minimizes jitter and spurious harmonics during transmissions. The receiver senses data on the coaxial transmission media and outputs the data to the Manchester encoder/decoder via the RX+ and RX- AUI pins. These pins drive the AUI cable through a pulse isolation transformer.

3.0 OPERATIONAL DESCRIPTION

This section describes the six basic functions of the Ethernet Transceiver, including receiving, transmitting, collision signaling, collision detection, jabber timing, and the heartbeat function. Refer to Figure 3-1 for a general system block diagram.

3.1 Receiver Functions

The receiver senses signals at pin 14 through the RXI input, which minimizes reflections on the transmission media using a low capacitance, high resistance input buffer amplifier. The CDS ground input at pin 16 attaches directly to the input buffer from the coaxial shield to eliminate ground loop noise.

In addition to the input buffer, the receiver data path consists of an equalizer, data slicer, receiver squelch circuitry, and an output line driver.

The equalizer improves the jitter margin; the data slicer restores equalized received signals to fast transition signals with binary levels to drive the receiver line driver; and the receiver line driver drives the AUI cable through an isolation transformer that connects to the AUI interface. See Figure 3-2.

Noise on the transmission media is rejected by the receiver squelch circuitry, which determines valid data via two criteria: DC level and pulse width. The DC voltage level is detected and compared to a set level in the receiver comparator circuit. The pulse width must be greater than 20 nsec and repeat at valid data rates. It is detected using a pulse detector, operating like a retriggerable one-shot that resets at approximately two signal bit times. The pulse width detector disables the receiver line driver at the end of a transmission (Figure C-1).

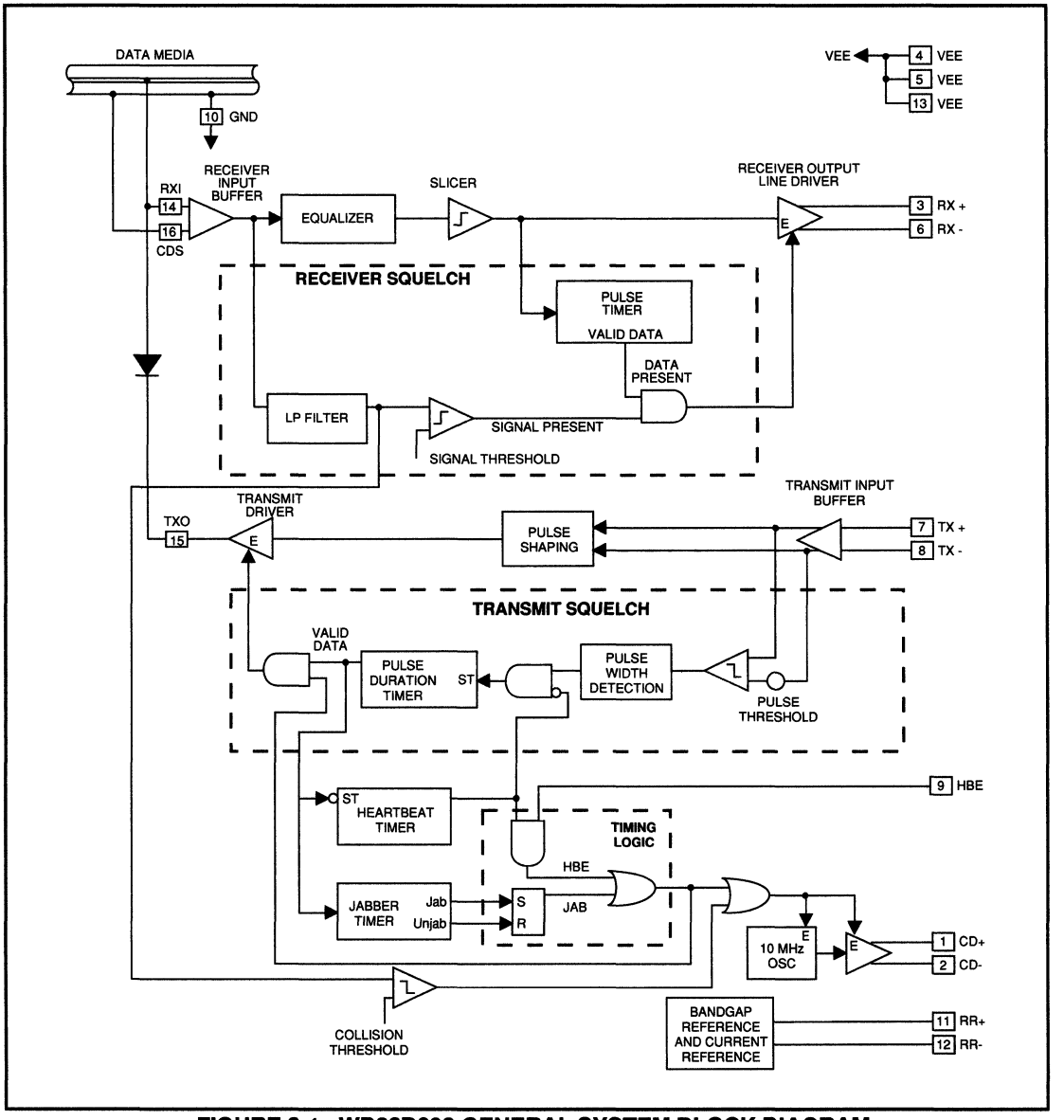

FIGURE 3-1. WD83B692 GENERAL SYSTEM BLOCK DIAGRAM

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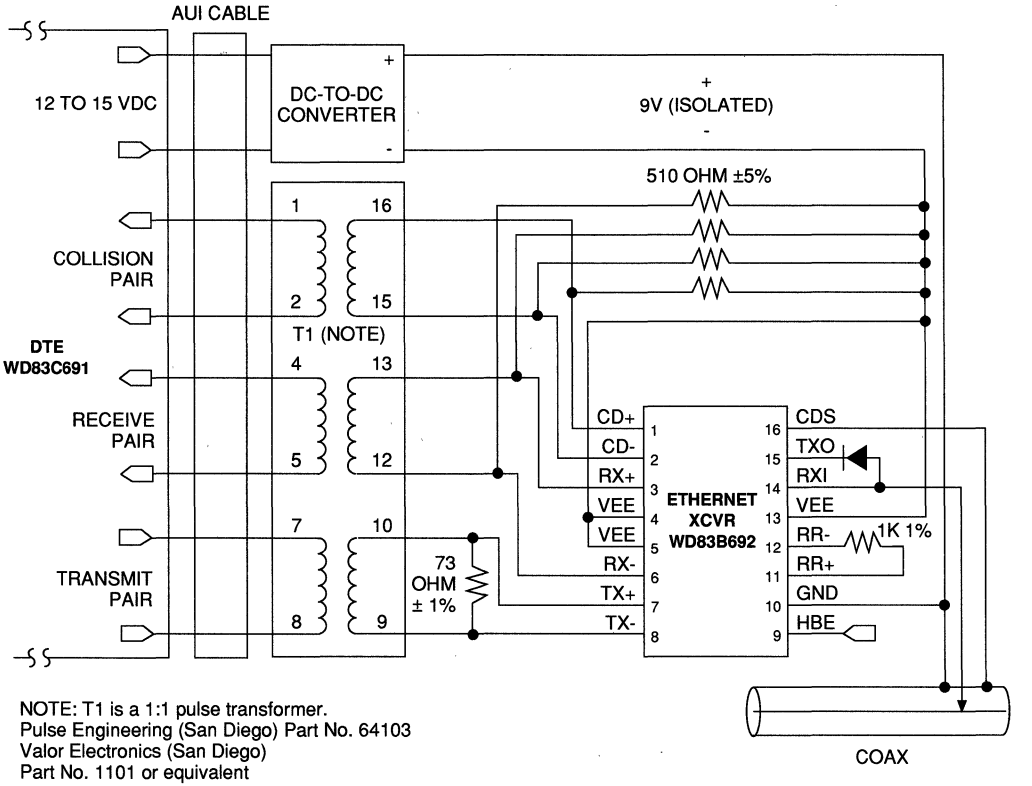

FIGURE 3-2. CONNECTION DIAGRAM

3.2 Transmitter Functions

The transmitter data path consists of a transmit input buffer, a pulse-shaping network (ramp generator), transmit squelch circuitry, a transmit driver, and a transmit output line driver.

The self-biasing, transmit input buffer receives data through an isolation transformer and translates the AUI differential analog signal to digital signals suitable for driving the pulse shaping network. The pulse shaping network gives equal rise and fall times to the transmit driver, which uses a high impedance current source output to drive the transmission media. The capacitance of the transmit driver is isolated from the transmission media by an external diode with a low capacitance anode. The shield of the transmission media serves as the ground return for the transmitter function.

A transmit squelch circuit, which consists of a pulse threshold detector, a pulse width detector, and a pulse duration timer, is used to suppress noise, as well as crosstalk, on the AUI cable. The squelch circuitry disables the transmit driver if the signal at TX+ or TX- is smaller than the pulse threshold. Pulse noise is rejected by a pulse width detector that passes only pulses with durations greater than 20 nsec. The pulse duration timer disables the transmit driver if no pulses are received for two-bit periods following valid pulses. At the end of a transmission, the pulse duration timer disables the transmitter and triggers the blanking timer, used to block "dribble" bits.

3.3 Collision Signaling

When collision signaling is enabled, a 10-MHz signal is sent to the CD% pins (1,2) through an isolation transformer to the Manchester encoder/decoder. When the function is disabled, this output goes to a zero differential state. The 10-MHz output from the CD pins indicates a collision on the transmission media, a heartbeat function, or that the transmitter is in jabber mode.

3.4 Collision Detection

A collision occurs when two or more transmitters simultaneously access the transmission media. A collision is detected by comparing the DC level of the transmission media to a collision threshold. The received signal at RXI (pin 14) is buffered and sent through a low pass filter, then compared in the collision threshold circuit. If the DC level exceeds the collision threshold, the 10-MHz oscillator and CD outputs are enabled.

3.5 Jabber Function

When valid data is transmitted, the jabber timer is started. If there is valid data for more than 20 msec, a latch is set which disables the transmitter and enables the 10-MHz output on the CD pins. The latch is reset within 0.5 seconds after the valid data is removed from the transmitter input (TX%). This action resets the jabber timer and disables the 10-MHz oscillator and CD output. The TX% inputs must remain inactive during the 0.5-second reset period.

3.6 Heartbeat Function

The 10-MHz oscillator and CD outputs are enabled for about 1 µsec at approximately 1.1 µsec after the end of each transmission. The heartbeat signal tells the DTE that the circuit is functioning. This is implemented by starting the heartbeat timer when the valid data signal indicates the end of a transmission.

A.0 APPENDIX A

A.1 PIN DESIGNATIONS

Figure A-1 illustrates the 16-pin DIP device. Table A-1 lists all pin designations.

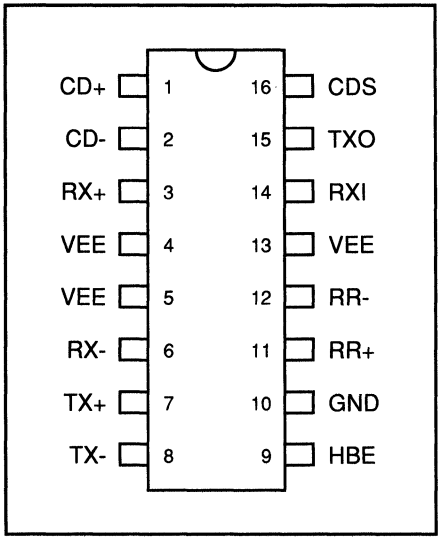

FIGURE A-1. WD83B692 16-PIN DIP ETHERNET TRANSCEIVER

PIN NUMBERS	MNEMONIC	SIGNAL NAME	FUNCTION
1,2	CD+,CD-*	Collision Output	Balanced differential line driver outputs from the collision detect circuitry. The 10-MHz signal from the internal oscillator is transferred to these outputs in the event of collision, jabber, or a heartbeat condition. These outputs are open emitters; pull-down resistors to VEE are required. When operating into a 78-ohm transmission line, these resistors should be 500 ohms. In Cheapernet applications, where the 78-ohm drop cable is not used, higher resistor values (up to 1.5K) may be used to save power.
3,6	RX+,RX-*	Receiver Output	Balanced differential line driver outputs from the receiver. These outputs require 500-ohm pull-down resistors.
7,8	TX+,TX-*	Transmit Input	Balanced differential line receiver inputs to the transmitter. The common mode voltage for these inputs is determined internally. Signals meeting transmitter squelch requirements are wave-shaped and output at TXO (pin 15).
9	HBE	Heartbeat Enable	This input enables CD heartbeat when grounded and disables it when connected to VEE.
10	GND	Ground	Ground positive supply. A 0.1 μ F ceramic decoupling capacitor must be connected across GND and VEE as close to the component as possible.
11,12	RR+, RR-	External Resistor	A fixed, 1.0K, 1.0% resistor connected between these pins establishes internal operating currents.
14	RXI	Receiver Input	Connects directly to the coaxial cable. Signals meeting receiver squelch requirements are equalized for intersymbol distortion, amplified, then output at the RX+ or RX- pin.
15	TXO	Transmitter Output	In both Ethernet and Cheapernet applications, this connects through an isolation diode to the coaxial cable.

TABLE A-1. PIN DESIGNATIONS

PIN NUMBERS	MNEMONIC	SIGNAL NAME	FUNCTION
16	CDS	Collision Detect Sense	This is the ground sense connection for the collision detect circuit. This pin should be connected separately to the shield to avoid ground drops from altering the receive mode collision.
4,5,13	VEE	Negative Supply	These pins should be connected to a large area of the lower metal layer on the PC board to handle heat dissipation.

TABLE A-1. PIN DESIGNATIONS (Continued)

*IEEE names for CD± = CI±; RX± = DI±; TX± = DO±

B.0 APPENDIX B

B.1 DC OPERATING CHARACTERISTICS

Absolute maximum ratings indicate limits beyond which permanent damage may occur. Continuous operation at these limits is not recommended; operation should be limited to those conditions specified under Recommended Operating Characteristics.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	-12V
Input Voltage	0 to -12V
Package Power Rating at 25° C (77° F)	2.5 Watts

(PC Board Mounted)

Derate linearly at the rate of 20 mWatts/°C

Lead Temperature (soldering, 10 seconds)	300°C (572 °F)

Electrostatic Discharge (ESD) 1200V*

* All pins tested per MIL-STD-883 Method 3015, Human Body Model. For the RXI pin only, the specified value is 500V.

Storage Temperature -65°C (-85°F) to 150°C (302°F)

(For actual dissipation of the device refer to Table B-1.)

RECOMMENDED OPERATING CONDITIONS

Supply Voltage (VEE)	-9V ±5%
Ambient Temperature	0°C (32°F) to 70°C (158°F)

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SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	NOTES*
VOC	Common Mode Output Voltage (RX%, CD%)	-2.5	-2.0	-1.5	V	3,7,8
VOB	Differential Output Voltage Imbalance (RX%, CD%)	-	-	%40	mV	3,8,9
IOB	Differential Output Current Imbalance	-	-	%4.0	mA	3,8,9
VOD	Differential Output Voltage	%600	-	%1200	mV	3,8
ZR	Input Impedance Real (TX%)	1.24	-	-	KΩ	-
ZI	Input Capacitance (TX%)	0	-	6.0	pF	-
VTC	Common Mode Input Voltage (TX%)	-1.8	-	-1.2	V	12
VLT	Differential Logic Threshold (TX%)	0	-	338	mV	-
CMR	Common Mode Rejection (TX%)	40	-	-	dB	11
HE	Heartbeat Enable	VEE+1.5	GND	-	V	-
HD	Heartbeat Disable	-	VEE	VEE+.01	V	-
RR	Reference Resistor	0.99	-	1.01	KΩ	-
IEE1	Supply Current - Non-Transmitting	-	85	130	mA	-
IEE2	Supply Current - Transmitting	-	125	180	mA	-
IRX1	Receive Input Bus Current	-2.0	-	+20	µA	3
CX	Input Capacitance (RXI)	-	1.2	-	pF	3
RRXI	Shunt Resistance - Non-Transmitting (RXI)	1.0	-	-	MΩ	3

TABLE B-1. DC OPERATING CHARACTERISTICS

Ta = 0°C (32°F) to 70°(158°), VEE = -9V% 5% (See Note 2 on page 1-11.)

*Refer to Notes on p. 1-11.

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	NOTES
VCD	Collision Threshold (Receive Mode)	-1.58	-1.492	-1.404	V	10
VSQ	Input Squelch Threshold	-0.6	-	-0.35	V	-
ITDC	Transmit Output DC Current Level	37	41	45	mA	4
ITAC	Transmit Output AC Current Level	%28	-	ITDC	mA	4,5
RTXON	Shunt Resistance - Transmitting (TXO)	7.5	10	-	KΩ	4,6
RTXOF	Shunt Resistance - Non-Transmitting (TXO)	200	-	-	KΩ	4
ILOF	Leakage Current - Non-Transmitting	-	-	%1.0	µA	3,4
CTXO	Capacitance - Non-Transmitting	-	8	-	pF	3,4

TABLE B-1. DC OPERATING CHARACTERISTICS (continued)

NOTES:

1. Currents into device pins are positive; currents out of device pins are negative. If not specified, voltages are referenced to ground.
2. All typicals are for VEE = -9V, Ta = 25°.
3. 0 > VEE > -9.5V.
4. The voltage on TXO is -4V < V(TXO) < 0.0V.
5. The AC current measurement is referenced to the DC current level.
6. The shunt resistance does not degrade the ITAC current if five transmitters are simultaneously driving a 50Ω-terminated coax cable.
7. Operating or idle state.
8. Test load as shown in Figure B-1.
9. Device measurement taken in idle state.
10. This threshold can be determined by monitoring the CD% output with a DC level into RXI.
11. The TXO does not switch with a 100 mVpp common mode sine wave input for frequencies from 0 to 10 MHz input to TX+, TX- with a common mode DC level from 0 to -3V.
12. This is a self-bias, level-generated on device, and is measured with a DC voltmeter with no external load on the TX+ or TX- pin.

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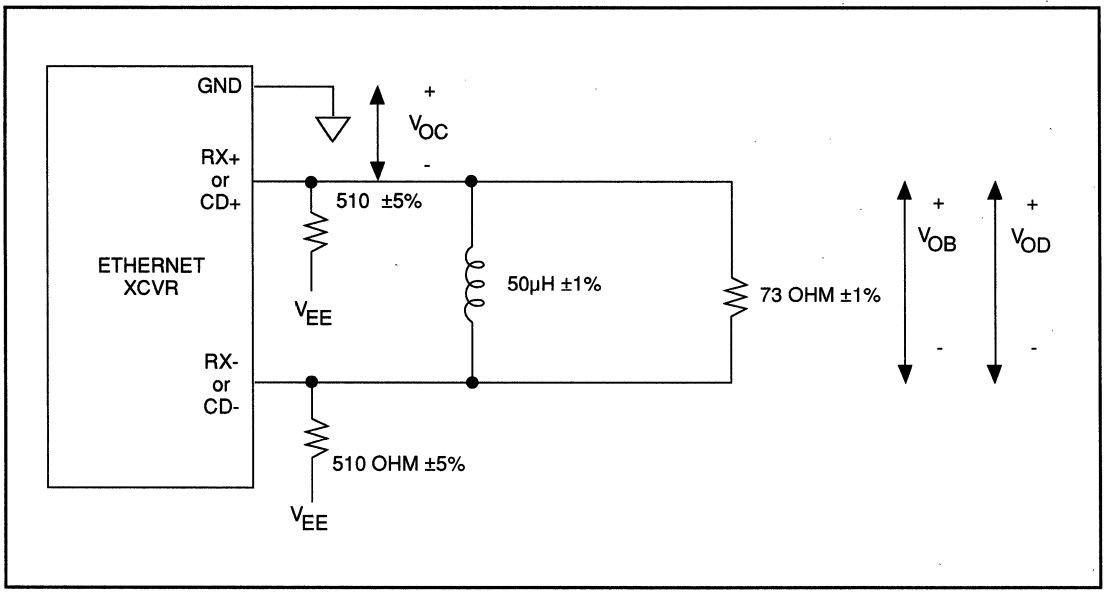

FIGURE B-1. TEST LOAD FOR CD% OR RX%

C.0 APPENDIX C
C.1 AC OPERATING CHARACTERISTICS AND TIMING DIAGRAMS

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	NOTES*
	Transmit Specification					
t_{TST}	Transmitter Start-up Delay (See Figure C-2)	-	1	2	bits	8
t_{TD}	Transmitter Propagation Delay (See Figure C-2)	-	25	50	nsec	8
t_{TS}	Transmitter Jitter	-	%0.5	2.0	nsec	7,8
t_{TR}	Transmitter Rise Time; 10 - 90% (See Figure C-2)	20	25	30	nsec	-
t_{TF}	Transmitter Fall Time; 90 - 10% (See Figure C-2)	20	25	30	nsec	-
t_{TM}	t_{TR} and t_{TF} Mismatch (See Figure C-2)	-	1	-	nsec	-
	TX% Transmit Squelch Timing					
t_{TON}	Transmit Turn-on Pulse Width at VTS (See Figure C-2)	8	25	30	nsec	-
t_{TOFF}	Minimum Transmit Turn-off Pulse Width at VTS (See Figure C-2)	-	180	-	nsec	-
	Receive Specification					
t_{RJ}	Receive Jitter (See Figure C-6)	-	2	4	nsec	5
t_{RON}	Receiver Start-up Delay (See Figure C-1)	-	4	5	bits	4
t_{RD}	Propagation Delay (See Figure C-1)	-	15	50	nsec	-

TABLE C-1. AC OPERATING CHARACTERISTICS

Ta = 0°C (32°F) to 70°C (158°F); see note 3 on page 1-16. VEE = -9V%5%, Bit Time = 100 nsec

*Refer to Notes on p. 16.

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Transmit Specifications

The first bit transmitted from TXO may have data and phase violations. The second through last bit reproduce the TX% signal with less than or equal to specified jitter.

There is no logical signal inversion between TX% and TXO output. A low level from TX+ to TX- results in more current flowing from the coaxial cable into the TXO pin.

At the end of transmission, when the transmitter changes from the enabled state to the idle state, no spurious pulses are generated, i.e., the transition on TXO proceeds monotonically to zero current.

Receive Specifications

The first bit sent from RX% may have data and phase violations. The second through last bit reproduce the received signal with less than or equal to specified jitter.

There is no logical signal inversion between the RXI input and the RX% output. A high level at RXI produces a positive differential voltage from RX+ to RX-.

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	NOTES*
	RX%, CD% Specification					
t_{RR}	Differential Outputs Rise Time	-	4	5	nsec	-
t_{RF}	Differential Outputs Fall Time	-	4	5	nsec	-
t_{EV}	Dynamic Pulse Envelope	(See Figure C-9)				6
v_{CM}	AC Common Mode Signal	-	-	50	mV	-

TABLE C-1. AC OPERATING CHARACTERISTICS (continued)

*Refer to Notes on p. 16.

Active to Idle Transition

The output waveform conforms to the limits as specified in Figure C-10.

Short Protection

The electrical and physical characteristics of the RX%, CD% outputs are not altered if the pins are shorted together or to ground.

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	NOTES*
	CD% Collision Detection Timing					
t_{CON}	Collision Turn-on Delay (See Figure C-3)	-	7	9	bits	-
t_{COFF}	Collision Turn-off Delay (see Figure C-3)	-	-	20	bits	-
f_{CD}	Collision Frequency (See Figure C-3)	8.5	-	11.5	MHz	-
t_{CP}	Collision Pulse Width (See Figure C-3)	40	-	60	nsec	-
t_{HON}	CD Heartbeat Delay (see Figure C-4)	0.6	-	1.6	µsec	-
t_{HW}	CD Heartbeat Duration (See Figure C-4)	0.6	1.0	1.5	µsec	-

TABLE C-1. AC OPERATING CHARACTERISTICS (continued)

*Refer to Notes on p. 16.

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	NOTES
Jabber Timing						
t_{JA}	Jabber Activation Delay (See Figure C-5)	20	50	150	msec	-
t_{JR}	Jabber Reset Unjab Time (See Figure C-5)	250	300	750	msec	-

TABLE C-1. AC OPERATING CHARACTERISTICS (continued)

NOTES

1. Absolute maximum ratings are values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits.
2. All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to ground unless otherwise specified.
3. All typicals are given for VEE = -9V and Ta = 25°.
4. RXI low to RX± out of idle state.
5. Using the test configuration load shown in Figure C-6, jitter is measured at RX± in relation to transmitter edges. The waveform is a 10-MB Manchester-coded signal with an amplitude of 0.749 to 2.6 Vpp. The waveform has a rise and fall time of 25 ± 1 nsec and zero jitter. The DC level is from 0 to 2.6V and does not clip input waveform.
6. The dynamic voltage waveform stays within the shaded area of Figure C-9 when loaded as shown in Figure B-1.
7. Transmitter jitter is the difference in propagation delay from TX± to TXO for rising and falling output transition. This is measured using a random Manchester-coded signal.
8. The TX± input operates with signals meeting the RX± timing and amplitude specifications.

TIMING DIAGRAMS

Table C-2 lists all timing diagrams. Figures C-1 through C-12 illustrate all timings.

FIGURE NUMBER	TITLE
C-1	Receiver Timing
C-2	Transmitter Timing
C-3	Collision Timing
C-4	Heartbeat Timing
C-5	Jabber Timing
C-6	Receive Jitter Timing
C-7	Coaxial Transceiver Receive Timing
C-8	Coaxial Transceiver Transmit Timing
C-9	Dynamic Pulse Envelope
C-10	Enable to Idle Transition; CD±,RX±
C-11	Test Loads
C-12	Test Circuit for TX± Input

TABLE C-2. WD83B692 TIMING DIAGRAMS

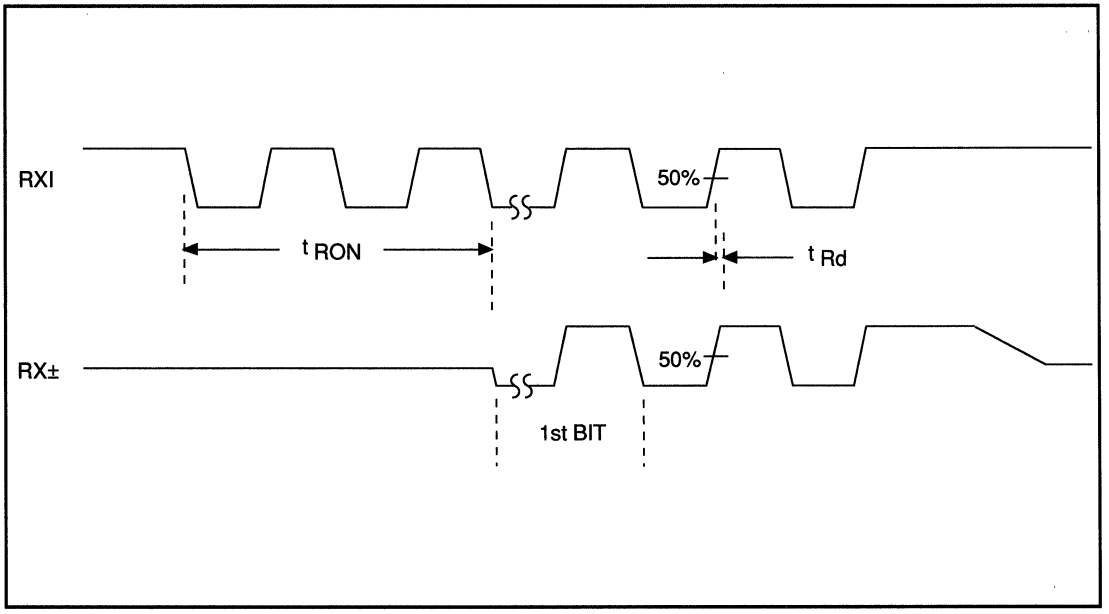

FIGURE C-1. RECEIVER TIMING

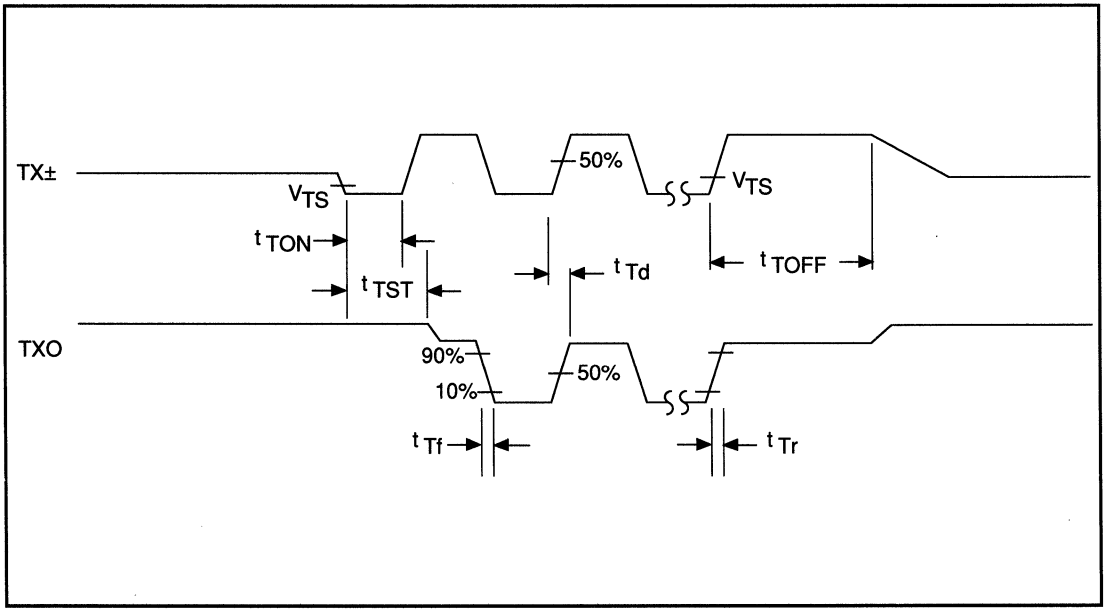

FIGURE C-2. TRANSMITTER TIMING

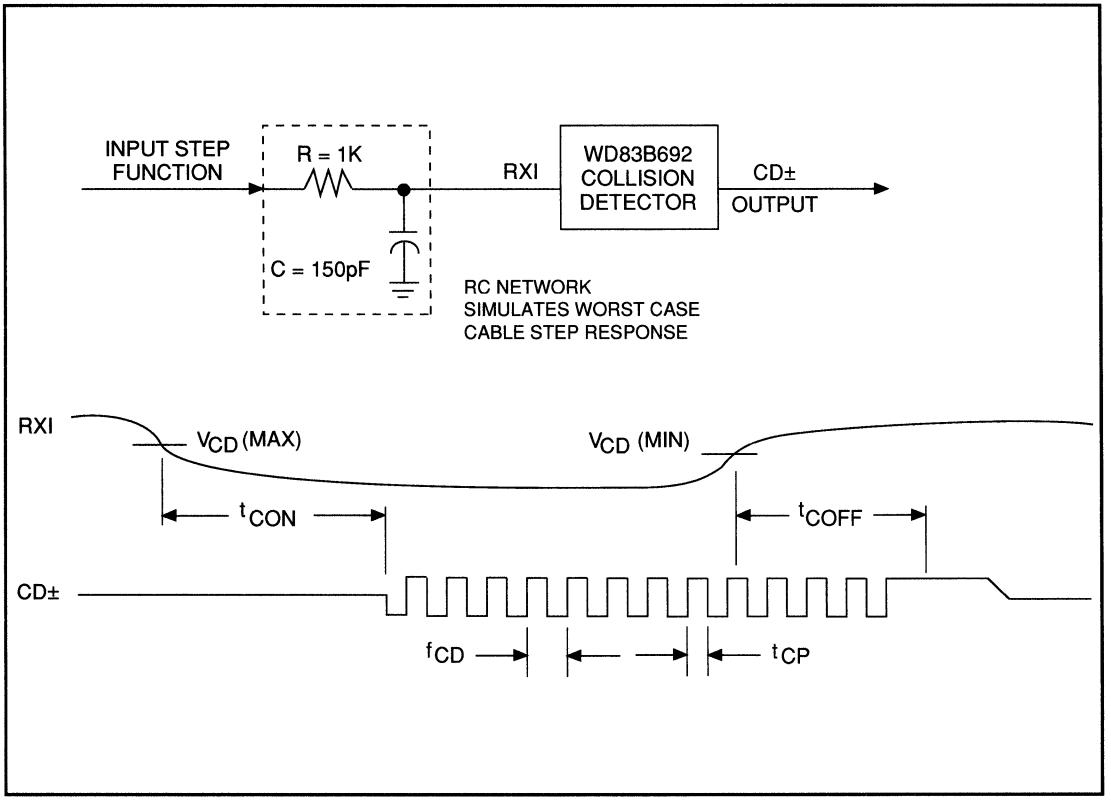

FIGURE C-3. COLLISION TIMING

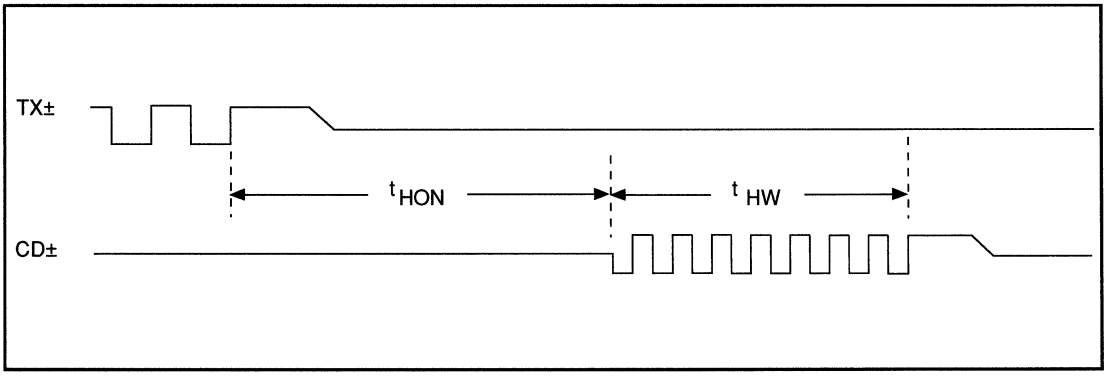

FIGURE C-4. HEARTBEAT TIMING

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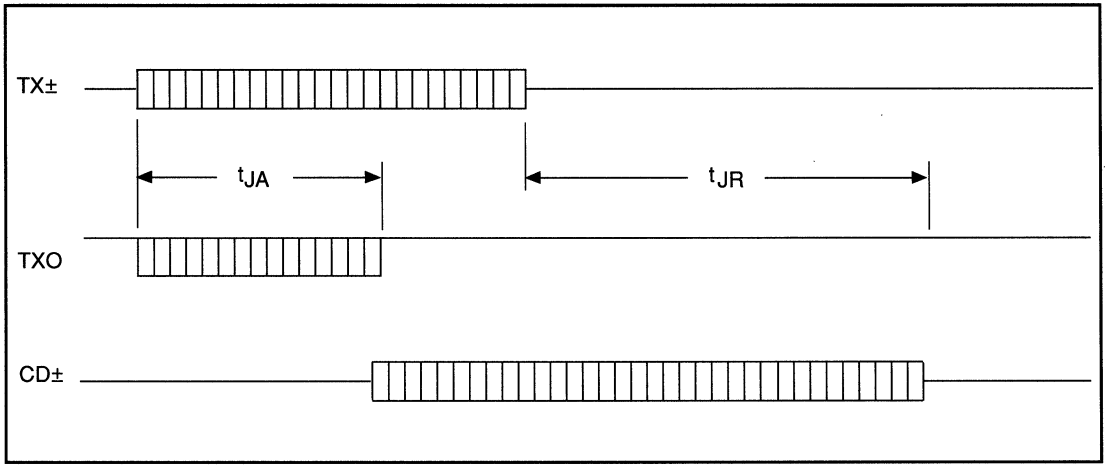

FIGURE C-5. JABBER TIMING

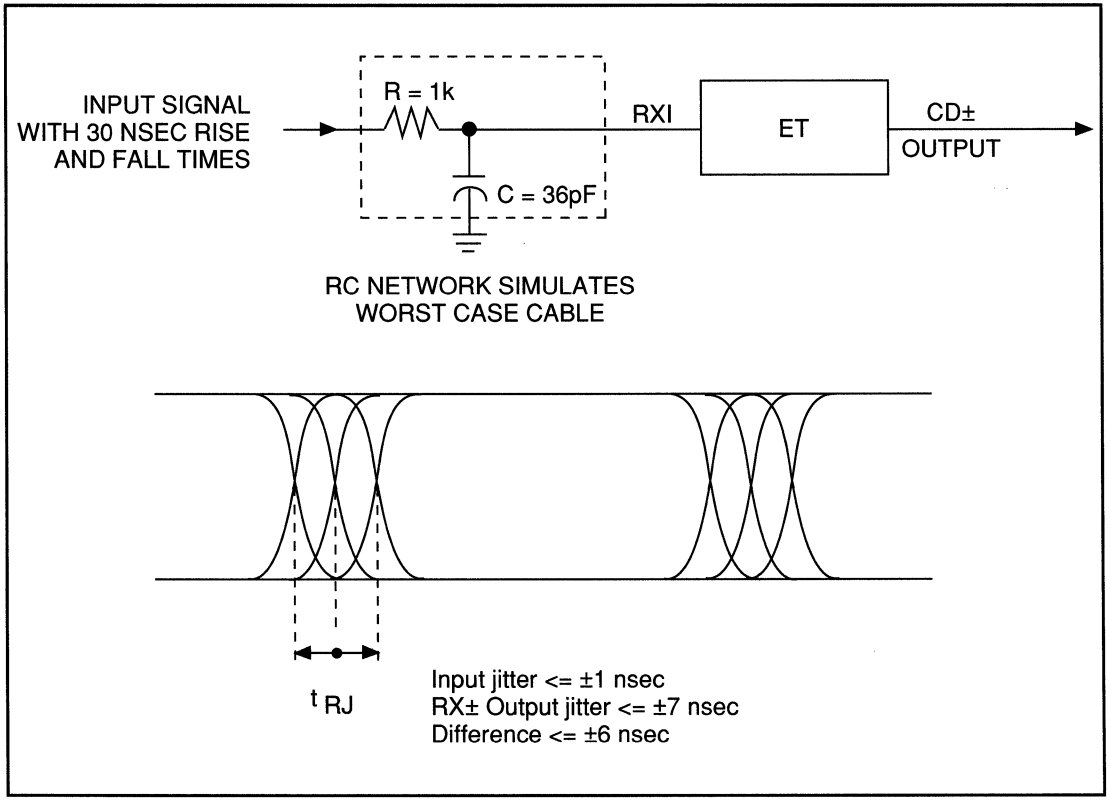

FIGURE C-6. RECEIVE JITTER TIMING

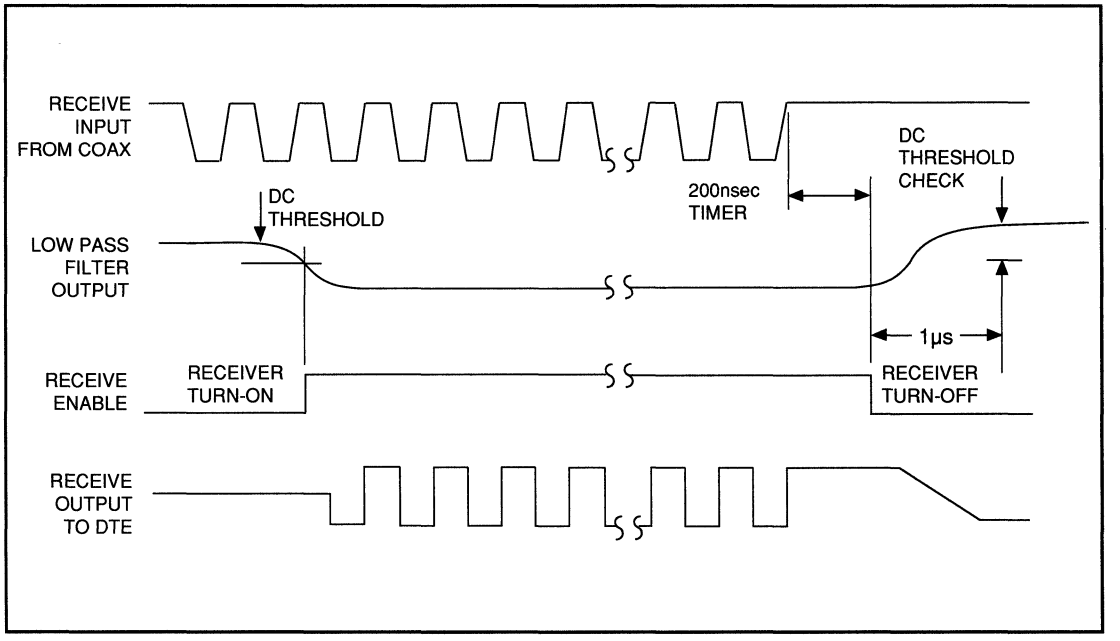

FIGURE C-7. COAXIAL TRANSCEIVER RECEIVE TIMING

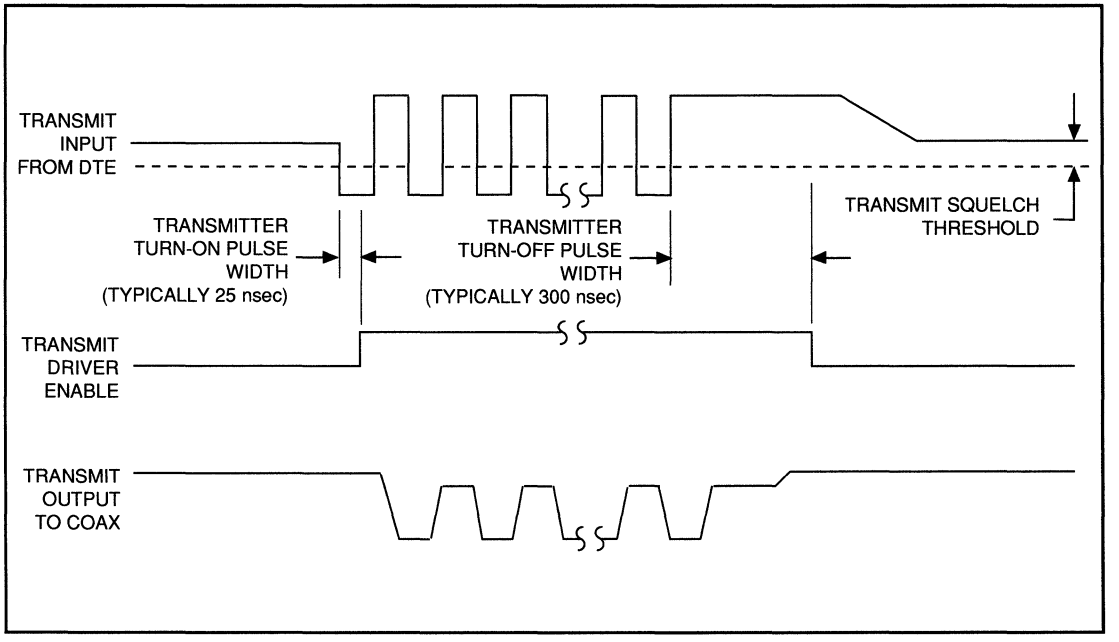

FIGURE C-8. COAXIAL TRANSCEIVER TRANSMIT TIMING

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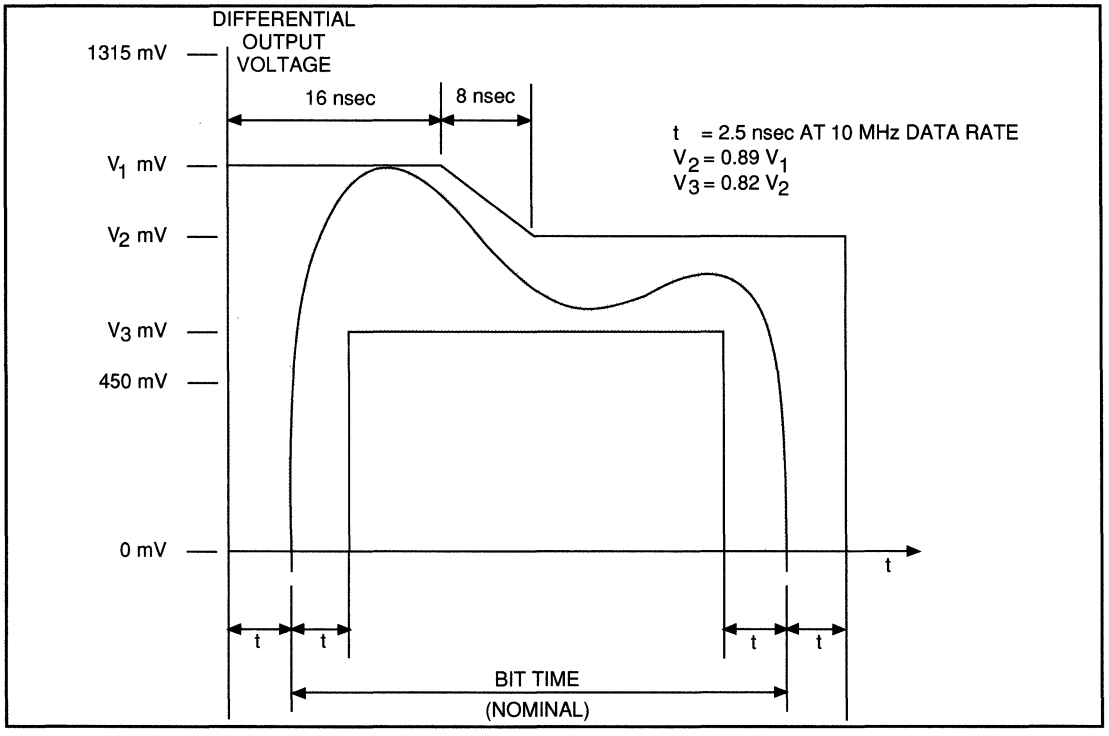

FIGURE C-9. DYNAMIC PULSE ENVELOPE

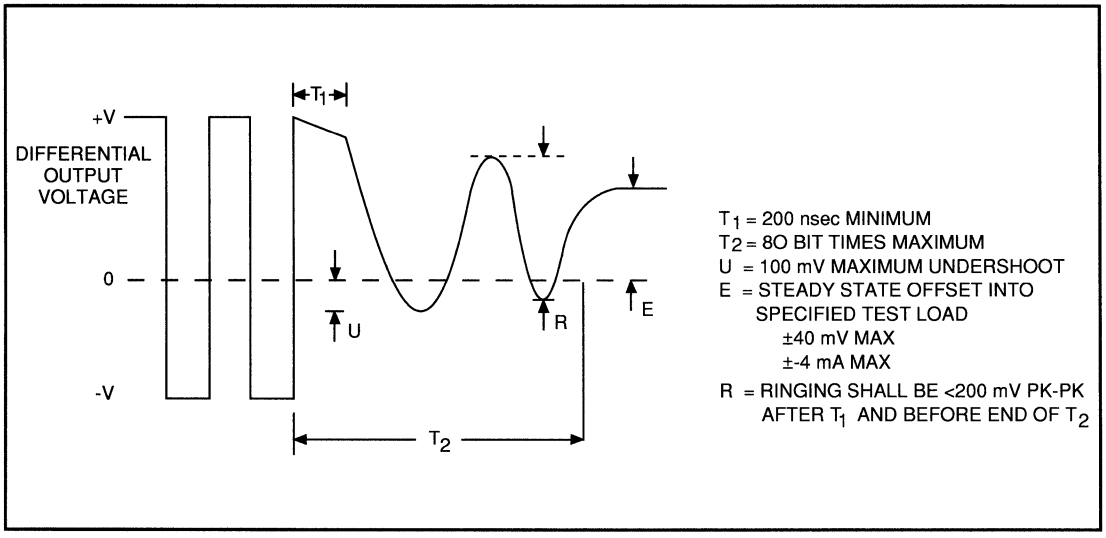

FIGURE C-10. ENABLE TO IDLE TRANSITION CD±,RX±

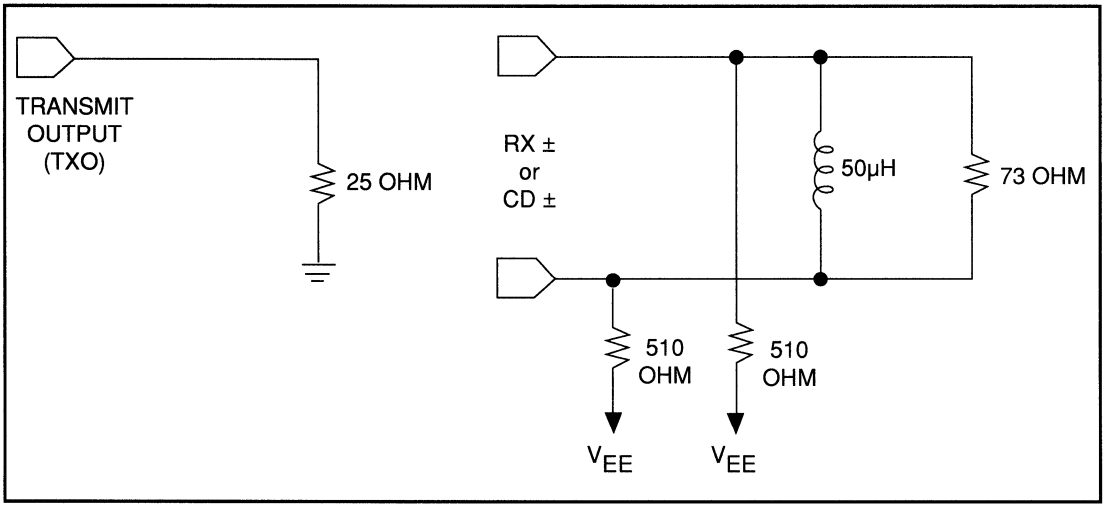

FIGURE C-11. TEST LOADS

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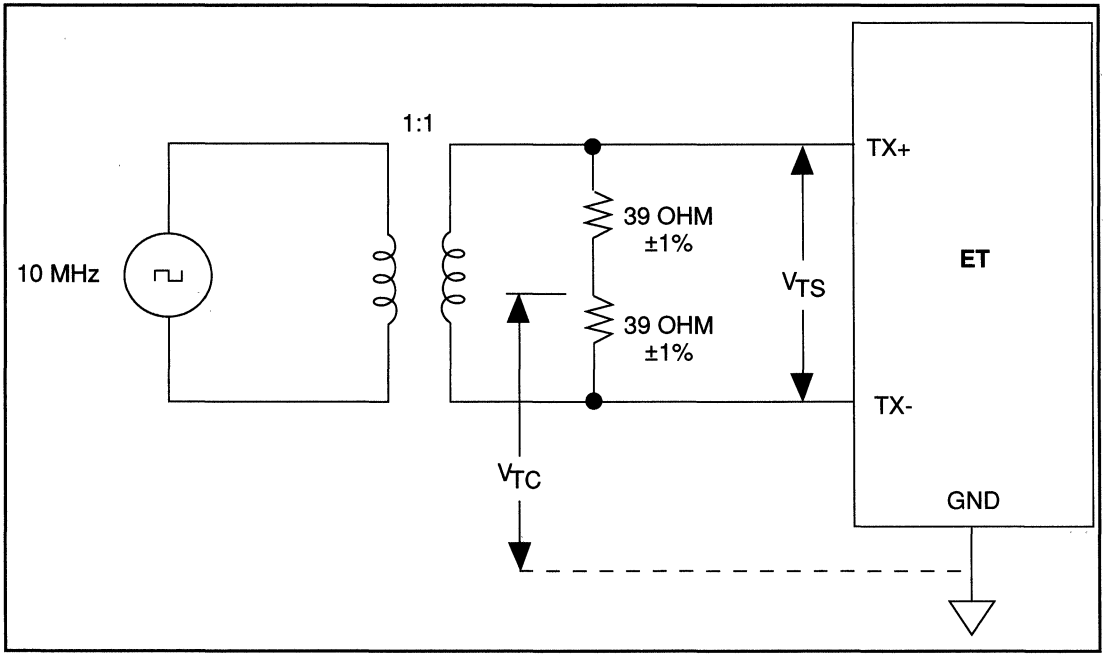

FIGURE C-12. TEST CIRCUIT FOR TX± INPUT

D.0 APPENDIX D

D.1 PACKAGE SPECIFICATIONS

Figure D-1 illustrates the 16-Pin DIP package showing dimensions in inches (and millimeters).

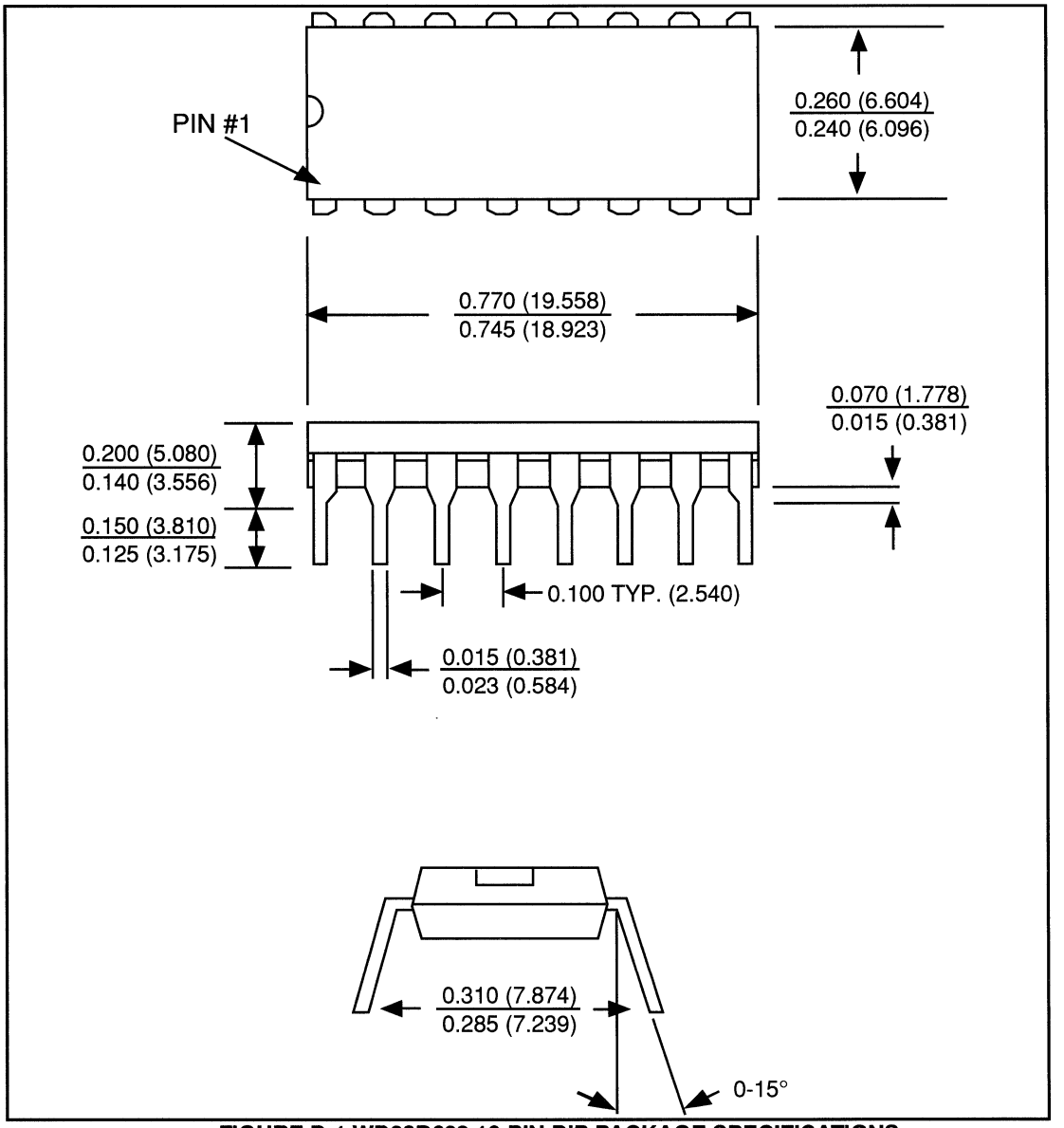

FIGURE D-1 WD83B692 16-PIN DIP PACKAGE SPECIFICATIONS

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