MOS
INTEGRATED
CIRCUITS

X CARD
M 274

PRELIMINARY DATA

PROGRAMMABLE ELECTRONIC CREDIT CARD

- LOW COST PLASTIC CREDIT CARD STYLE PACKAGING
- BUILT-IN CHIP WITH 105 CREDIT CELLS, ALL SEPARATELY ADDRESSABLE
- ONE SECURITY KEY WORD OF 8 BITS PROTECTED BY A SECURITY FUSE
- ONE MASK-PROGRAMMABLE 8-BIT CODE FOR USER IDENTIFICATION
- TYPICAL 10V POWER SUPPLY, 25V PROGRAMMING VOLTAGE
- LOW POWER CONSUMPTION: 115 mW (READING MODE), 320mW (PROGRAMMING MODE)
- WELL PROVEN NON-VOLATILE MEMORY DESIGN WITH 100 YEAR DATA RETENTION

This device is a remarkable new programmable memory product designed for electronic credit and identification cards. The product has only 7 connections (6 for user interfacing) and is essentially an EPROM of 17x8 bits.
If the XCARD is used as a credit card, the bit cells of the EPROM are all erased (content logic high) when the device is first delivered, and represent credit for services. Each time the card is used some bit cells are written, becoming useless. At any time the card can be checked for the amount of credit remaining and the reader can display this value.
When the XCARD is used as an identity card, it can be programmed with any one of several different codes (up to 2^{105}). This code can be read at any time by using an appropriate reader.
Row 16 of the matrix holds a mask programmable 8 bit code which can identify up to 256 different users. Since it is programmed during fabrication this code word is unerasable.
A second 8 bit word is used as a security key to detect fraudulent erasure and prevent re-use of the card.
This device is available in a plastic credit card style format (XCARD) or in a 14-lead plastic DIP for sampling and prototyping purposes (M274).

ABSOLUTE MAXIMUM RATINGS*

	Voltage on any pin (except PR)	-0.5 to 20	V
V_{PR}	Voltage on PR	-0.5 to 27	V
I_O	Output current	4	mA
P	Power dissipation	500	mW
T_{op}	Operating temperature range (XCARD only)	-30 to 60	°C
T_{stg}	Storage temperature range (XCARD only)	-30 to 60	°C

* Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

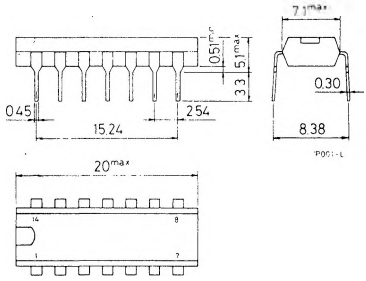
ORDERING NUMBERS

XCARD for credit card style package
M274B1 for dual in-line plastic package (samples only for evaluation)

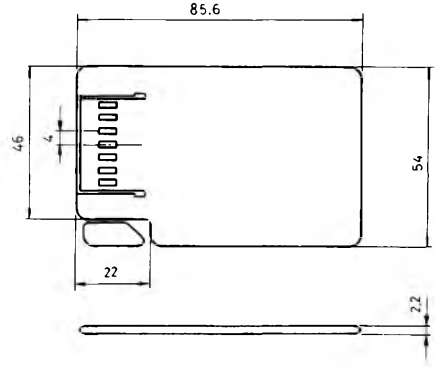
X CARD M 274

MECHANICAL DATA (dimensions in mm)

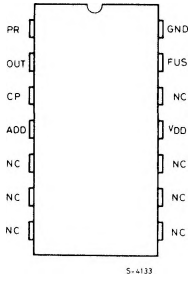
Dual in-line plastic package

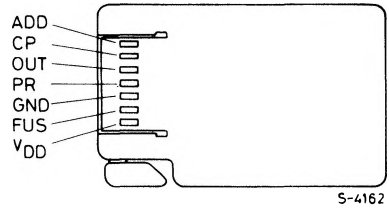


Plastic credit card style package



PIN CONNECTIONS



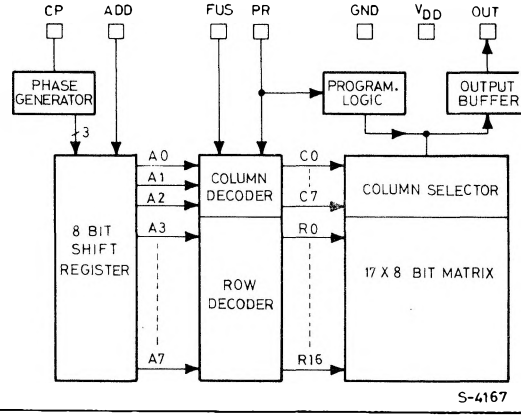


PIN DESCRIPTION

ADD	Address code input
CP	Clock input
PR	Programming signal input
OUT	Output
V_{DD}	Supply
GND	Ground
FUS*	Protection fuse
NC	Not connected

* Not connected
(see security key description)

BLOCK DIAGRAM



OPERATION

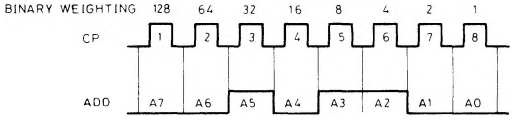
The matrix of 17 words by 8 bits must be addressed by serially loading an internal 8 bit shift register. The parallel outputs A0-A7 are decoded by the column and row decoders to address a single bit cell of the memory matrix. The content of this cell is output via an internal buffer. The logic of the M274 output is:

output = logic low (< 0.8V) = cell bit debited (written)
output = logic high (output transistor off) = cell bit in credit (unwritten)

The output is an open drain MOS transistor. During read operation the PR input is externally connected via a diode to the supply as shown in the application circuit, the current consumption is 10 mA (max) for V_{DD}= 10V.
The address data is loaded using an external clock of up to 100 kHz to read in the address bits A7 to A0 with clock pulses 1-8. When a frequency of less than 100 KHz is used, it is important to ensure that the mark time (i.e. CP pulse width) lies within the range 3 to 6 μs.
After the 8th clock pulse the output data is valid in 2 μs. Writing a bit cell is achieved by the application of a single +25V/10 mA pulse, of length 50 ms, to the PR input (> 10 μs after clock bit 8).

ADDRESSING

The serial address is obtained by generating a 1 or 0 in correspondence with one of 8 consecutive clock pulses. If for example cell number 44 is to be addressed (i.e. R5, C4 - see 17x8 BIT MATRIX ORGANIZATION), the correspondence between the two signals CP and ADD must be as shown below:



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The 8-bit word corresponding to address 44 is therefore:

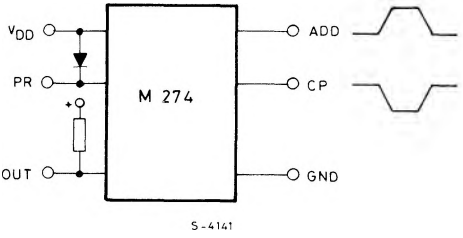
A7	A6	A5	A4	A3	A2	A1	A0
0	0	1	0	1	1	0	0

Note: The first cell (i.e. R0, C0) is considered number 0.

SECURITY KEY

One row of the matrix is written with an 8 bit word at manufacture, after writing this word - or security key - the write circuits to this row are destroyed by blowing an on-chip fuse and it is not possible to mend this fuse.
If any attempt is made to erase the card, to regain the credit value, the security key will also be erased: since the service point is normally designed to check for a valid security key before providing services, and before debiting the card, this is a complete method of protection against fraudulent re-use of the card.

APPLICATION CIRCUIT



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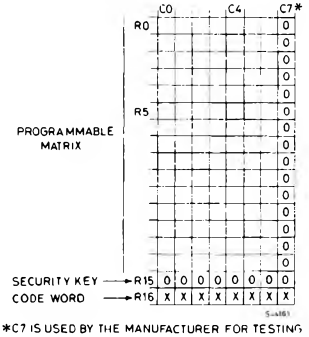
17x8 BIT MATRIX ORGANIZATION

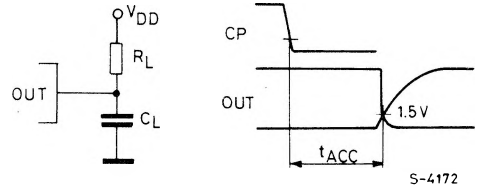


*C7 IS USED BY THE MANUFACTURER FOR TESTING

READING CHARACTERISTICS (see also timing waveforms)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
V_{DD}	Supply voltage		9		11	V
$V_{IL(ADD)}$	Address input low voltage		-0.3		0.5	V
$V_{IH(ADD)}$	Address input high voltage		8		V_{DD}	V
$V_{IL(CP)}$	Clock input low voltage		-0.3		0.5	V
$V_{IH(CP)}$	Clock input high voltage		8		V_{DD}	V
$V_{IL(PR)}$	Voltage on PR during verification		V_{DD}-0.8		V_{DD}-0.4	V
V_{OL}	Output low voltage	I_{OL}= 2 mA			0.8	V
I_{CP}	Clock input current (logic 0 and 1)				100	μA
I_{ADD}	Address input current (logic 0 and 1)				100	μA
I_{OL}	Output leakage current in OFF state	$V_O = V_{DD}$			100	μA
$I_{IL(PR)}$	Input current on PR during verification	$V_{PR} = V_{IL}$			5	mA
I_{DD}	Supply current				5	mA
f_{CP}	Clock frequency				100	kHz
$t_{s(ADD)}$	Address set-up time		0.5			μs
$t_{h(ADD)}$	Address hold time		0.5			μs
$t_{r(ADD)}$	Address rise time				2	μs
$t_{f(ADD)}$	Address fall time				2	μs
t_{ACC}	Access time	Note 1			2	μs
$t_{rCP)}$	Clock rise time				2	μs
$t_{f(CP)}$	Clock fall time				2	μs
$t_{w(CP)}$	CP pulse width		3		6	μs

Note 1 - t_{ACC} test conditions:
R_L= 5 kΩ, C_L= 100 pF, V_{DD}= 9V

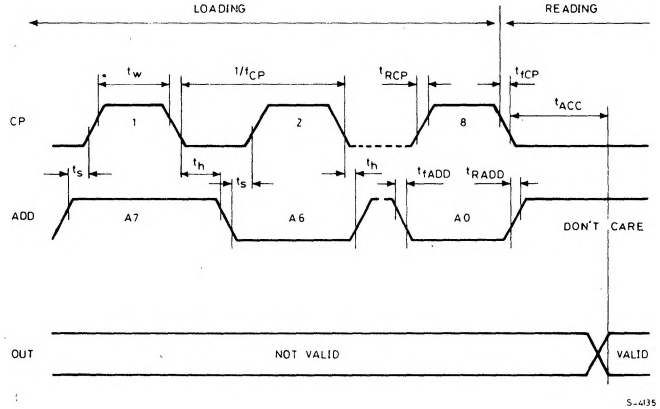


PROGRAMMING CHARACTERISTICS (see also timing waveforms)

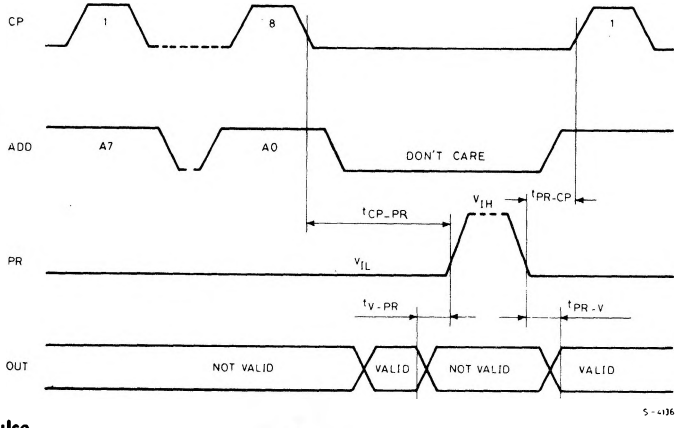
Parameter		Test conditions	Min.	Typ.	Max.	Unit
V_{DD}	Supply voltage		9		11	V
$V_{IL(ADD)}$	Address input low voltage		-0.3		0.5	V
$V_{IH(ADD)}$	Address input high voltage		8		V_{DD}	V
$V_{IL(CP)}$	Clock input low voltage		-0.3		0.5	V
$V_{IH(CP)}$	Clock input high voltage		8		V_{DD}	V
$V_{IH(PR)}$	Voltage on PR during programming pulse		24		26	V
I_{CP}	Clock input current (logic 0 and 1)				100	μA
I_{ADD}	Address input current (logic 0 and 1)				100	μA
$I_{IH(PR)}$	Input current on PR	$V_{PR}= V_{IH}$			10	mA
I_{DD}	Supply current				5	mA
f_{CP}	Clock frequency				100	kHz
$t_{s(ADD)}$	Address set-up time		0.5			μs
$t_{h(ADD)}$	Address hold time		0.5			μs
$t_{r(ADD)}$	Address rise time				2	μs
$t_{f(ADD)}$	Address fall time				2	μs
$t_{r(CP)}$	Clock rise time				2	μs
$t_{f(CP)}$	Clock fall time				2	μs
$t_{w(CP)}$	CP pulse width		3		6	μs
$t_{r(PR)}$	Programming rise time		10		100	μs
$t_{f(PR)}$	Programming fall time		10		100	μs
$t_{w(PR)}$	PR pulse width		50			ms
t_{CP-PR}	Time between last CP pulse and PR		10			μs
t_{PR-CP}	Time between last PR pulse and CP		10			μs
t_{V-PR}	Time between valid output data and PR pulse		0			μs
t_{PR-V}	Time between end of PR pulse and valid output data		3			μs

TIMING WAVEFORMS

Reading



Programming



Programming pulse