Z80230

ESCC™ ENHANCED SERIAL COMMUNICATION CONTROLLER

GENERAL DESCRIPTION

The Zilog Enhanced Serial Communications Controller, Z80230 ESCC, is a pin and software compatible CMOS member of the SCC family introduced by Zilog in 1981. The ESCC is a dual-channel, full-duplex data communications controller capable of supporting a wide range of popular protocols. The ESCC is built from Zilog's industry standard SCC core and is compatible with designs using Zilog's SCC to receive and transmit data. It has many improvements that significantly reduce CPU overhead. The addition of a 4-byte transmit FIFO and an 8-byte receive FIFO significantly reduces the overhead required to provide data to, and get data from, the transmitters and receivers.

The ESCC also has many features that improve packet handling in SDLC mode. The ESCC will automatically: transmit a flag before the data, reset the Tx Underrun/EOM latch, force the TxD pin high at the appropriate time when using NRZI encoding, deassert the /RTS pin after the closing flag, and better handle ABORTed frames when using the 10x19 status FIFO. The combination of these features along with the deeper data FIFOs significantly simplifies SDLC driver software.

The CPU hardware interface has been simplified by relieving the databus setup time requirement and supporting the software generation of the interrupt acknowledge signal (INTACK). These changes allow an interface with less external logic to many microprocessor families while maintaining compatibility with existing designs. I/O handling of the ESCC is improved over the SCC with faster response of the /INT and /DTR//REQ pins.

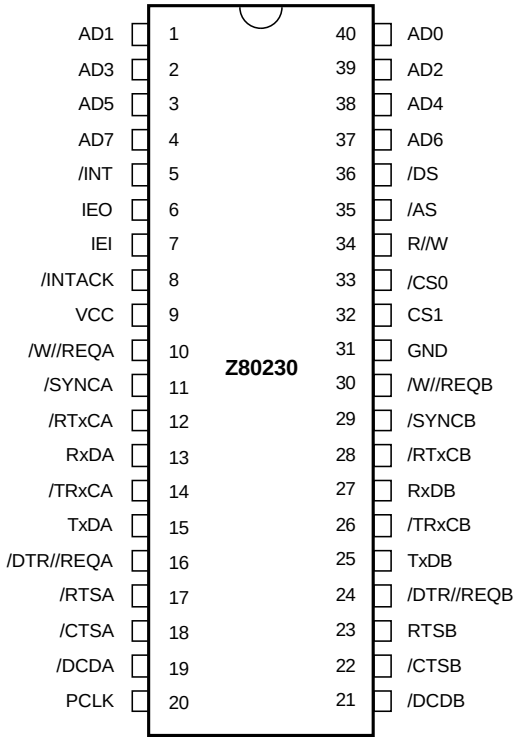
The many enhancements added to the ESCC permits a system design that increases overall system performance with better data handling and less interface logic.

Notes:
All Signals with a preceding front slash, "/", are active Low, e.g.: B//W (WORD is active Low); /B/W (BYTE is active Low, only).

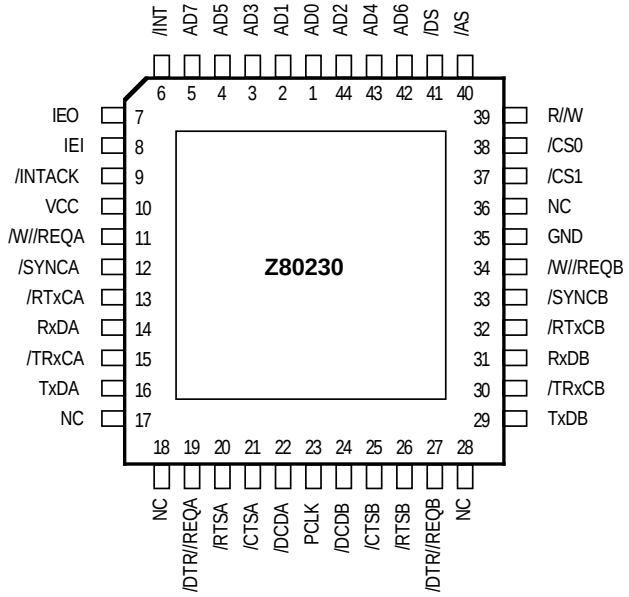
Power connections follow conventional descriptions below:

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

GENERAL DESCRIPTION (Continued)



Z80230 DIP Pin Assignments



Z80230 PLCC Pin Assignments

ABSOLUTE MAXIMUM RATINGS

V_{CC} Supply Voltage range ..... -0.3V to +7.0V
Voltages on all pins
with respect to GND..... -0.3V to V_{CC} +0.3V
Operating Ambient
Temperature..... See Ordering Information
Storage Temperature ..... -65°C to +150°C

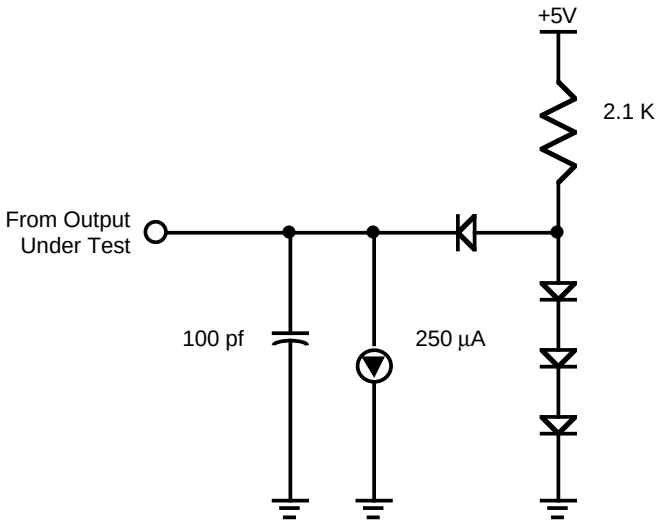
Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

STANDARD TEST CONDITIONS

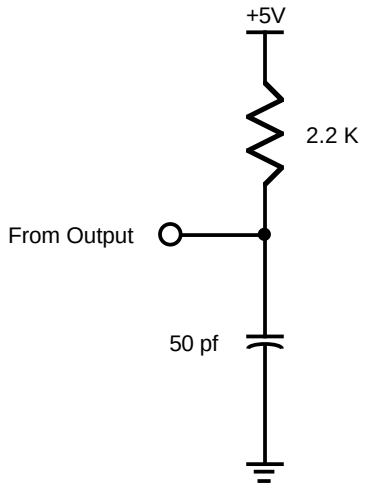
The DC Characteristics and capacitance sections below apply for the following standard test conditions, unless otherwise noted. All voltages are referenced to GND. Positive current flows into the referenced pin.

Standard conditions are as follows:

- +4.50 V ≤ V_{CC} ≤ + 5.50 V
- GND = 0 V
- T_A as specified in Ordering Information



Standard Test Load



Open-Drain Test Load

CAPACITANCE

Symbol	Parameter	Min	Max	Unit	Test Condition
C_{IN}	Input Capacitance		10	pF	Unmeasured pins
C_{OUT}	Output Capacitance		15	pF	returned to ground.
$C_{I/O}$	Bidirectional Capacitance		20	pF	

Note:
f = 1 MHz, over specified temperature range.

MISCELLANEOUS

Gate Count - 11,000

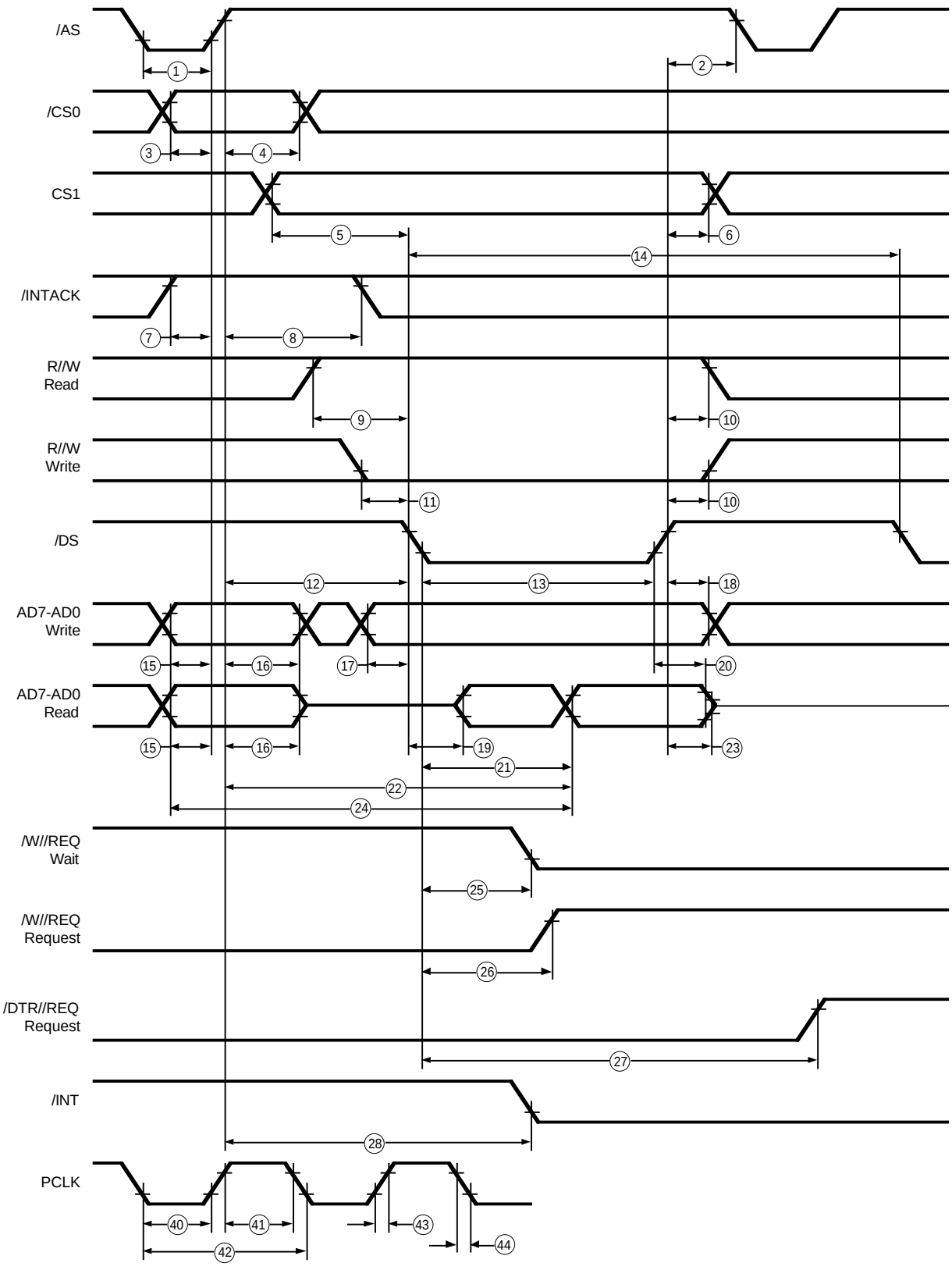
DC CHARACTERISTICS
Z80230

Symbol	Parameter	Min	Typ	Max	Unit	Condition
V_{IH}	Input High Voltage	2.2		V_{CC}+0.3	V	
V_{IL}	Input Low Voltage	-0.3		0.8	V	
V_{OH1}	Output High Voltage	2.4			V	I_{OH} = -1.6mA
V_{OH2}	Output High Voltage	V_{CC}-0.8			V	I_{OH} = -250µA
V_{OL}	Output Low Voltage			0.4	V	I_{OL} = +2.0mA
I_{IL}	Input Leakage			±10.0	µA	0.4 <V_{IN}<+2.4V
I_{OL}	Output Leakage			±10.0	µA	0.4 <V_{OUT}<+2.4V
I_{CC1}	V_{CC} Supply Current		4	10 (8.5 MHz)	mA	
			5	12 (10 MHz)	mA	V_{CC}=5V V_{IH}=4.8 V_{IL}=0.2V
			7	15 (16 MHz)	mA	Crystal Oscillators off
			9	20 (20 MHz)	mA	
$I_{CC(OSC)}$	Crystal OSC Current		6		mA	Current for each osc. in addition to I_{CC1}

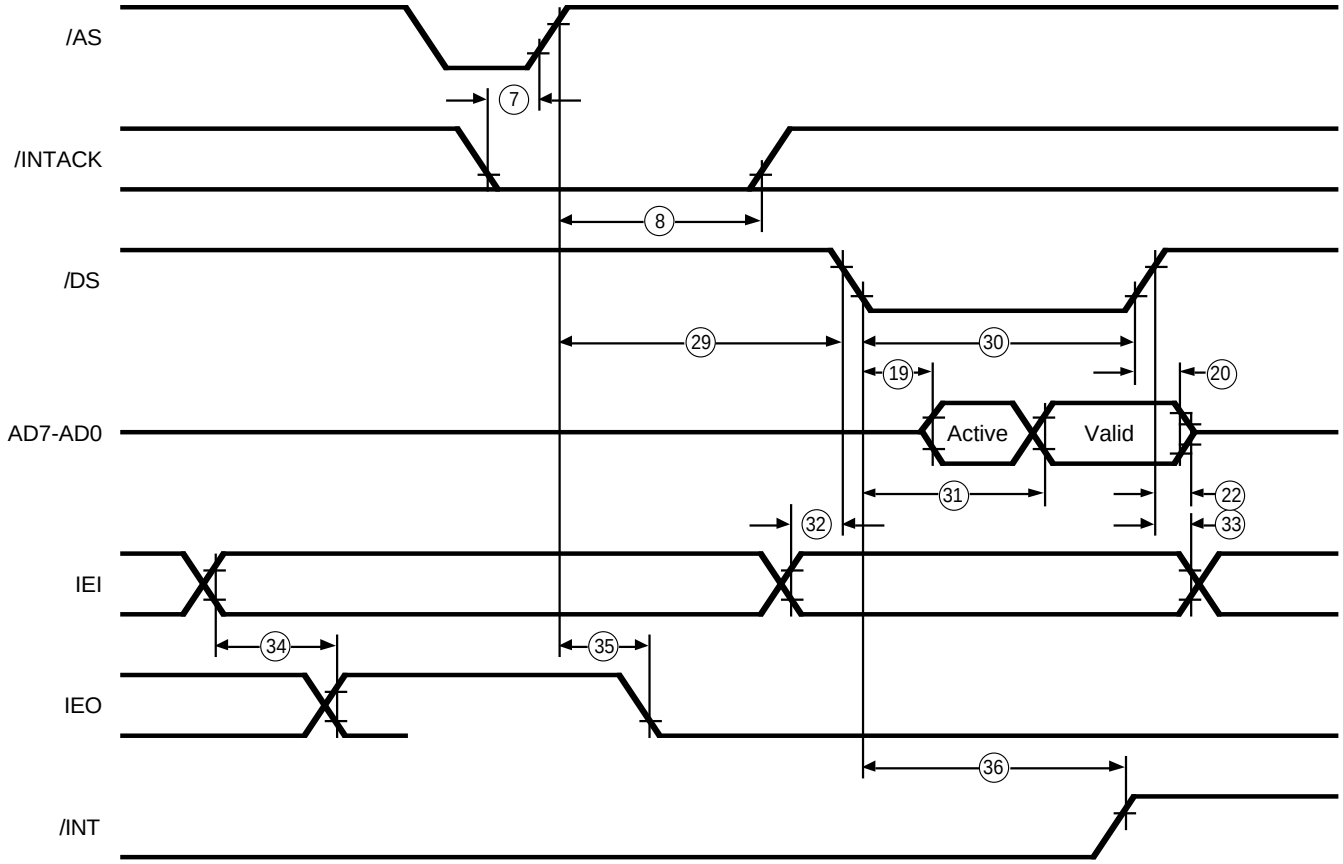
Notes:
[1] V_{CC} = 5V ± 10% unless otherwise specified, over specified temperature range.
[2] Typical I_{CC} was measured with oscillator off.
[3] No I_{CC}(osc) max is specified due to dependency on the external circuit.

AC CHARACTERISTICS

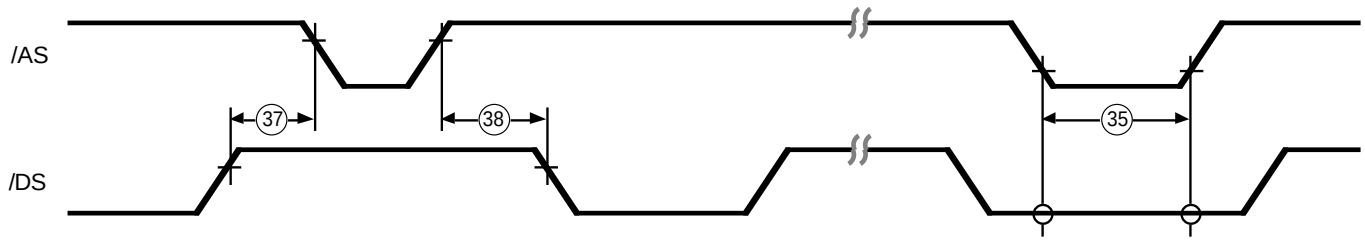
Z80230 Read and Write Timing Diagrams



Z80230 Read/Write Timing Diagram



Z80230 Interrupt Acknowledge Timing Diagram



Z80230 Reset Timing Diagram

AC CHARACTERISTICS

Z80230 Read/Write Timing Table

No	Symbol	Parameter	10 MHz Min	10 MHz Max	16 MHz Min	16 MHz Max	Notes*
1	TwAS	/AS Low Width	30		20		
2	TdDS(AS)	/DS Rise to /AS Fall Delay	10		10		[1]
3	TsCSO(AS)	/CS0 to /AS Rise Setup Time	0		0		[1]
4	ThCSO(AS)	/CS0 to /AS Rise Hold Time	20		15		[1]
5	TsCS1(DS)	CS1 to /DS Fall Setup Time	50		35		[1]
6	ThCS1(DS)	CS1 to /DS Rise Hold Time	20		10		[1]
7	TslA(AS)	/INTACK to /AS Rise Setup Time	10		10		
8	ThlA(AS)	/INTACK to /AS Rise Hold Time	125		100		
9	TsRWR(DS)	R//W (Read) to /DS Fall Setup Time	50		30		
10	ThRW(DS)	R//W to /DS Rise Hold Time	0		0		
11	TsRWW(DS)	R//W (Write) to /DS Fall Setup Time	0		0		
12	TdAS(DS)	/AS Rise to /DS Fall Delay	20		15		
13	TwDSl	/DS Low Width	125		80		
14	TrC	Valid Access Recovery Time	4TcPc		4TcPc		[2]
15	TsA(AS)	Address to /AS Rise Setup Time	10		10		[1]
16	ThA(AS)	Address to /AS Rise Hold Time	20		10		[1]
17	TsDW(DS)	Write Data to /DS Fall Setup Time	10		10		
18	ThDW(DS)	Write Data to /DS Rise Hold Time	0		0		
19	TdDS(DA)	/DS Fall to Data Active Delay	0		0		
20	TdDSr(DR)	/DS Rise to Read Data Not Valid Delay	0		0		
21	TdDSf(DR)	/DS Fall to Read Data Valid Delay		120		70	
22	TdAS(DR)	/AS Rise to Read Data Valid Delay		190		110	
23	TdDS(DRz)	/DS Rise to Read Data Float Delay		35		20	[3]
24	TdA(DR)	Address Required Valid to Read Data Valid Delay		210		100	
25	TdDS(W)	/DS Fall to Wait Valid Delay		160		60	[4]
26	TdDSf(REQ)	/DS Fall to /W//REQ Not Valid Delay		160		60	
27	TdDSr(REQ)	/DS Fall to /DTR//REQ Not Valid Delay		4TcPc		4TcPc	
28	TdAS(INT)	/AS Rise to /INT Valid Delay		500		175	[4]
29	TdAS(DSA)	/AS Rise to /DS Fall (Acknowledge) Delay	225		50		[5]
30	TwDSA	/DS (Acknowledge) Low Width	125		75		
31	TdDSA(DR)	/DS Fall (Acknowledge) to Read Data Valid Delay			70		
32	TslEl(DSA)	IEI to /DS Fall (Acknowledge) Setup Time	80		50		
33	ThlEl(DSA)	IEI to /DS Rise (Acknowledge) Hold Time	0		0		
34	TdlEl(IEO)	IEI to IEO Delay		90		45	
35	TdAS(IEO)	/AS Rise to IEO Delay		175		80	[6]
36	TdDSA(INT)	/DS Fall (Acknowledge) to /INT Inactive Delay		450		200	[4]
37	TdDS(ASQ)	/DS Rise to /AS Fall Delay for No Reset	15		10		
38	TdASQ(DS)	/AS Rise to /DS Fall Delay for No Reset	15		10		
39	TwRES	/AS and /DS Coincident Low for Reset	100		75		[7]
40	TwPCl	PCLK Low Width	40	100	26	1000	

AC CHARACTERISTICS

Z80230 Read/Write Timing Table (Continued)

No	Symbol	Parameter	10 MHz Min	10 MHz Max	16 MHz Min	16 MHz Max	Notes*
41	TwPCh	PCLK High Width	40	1000	26	1000	
42	TcPC	PCLK Cycle Time	100	2000	61	2000	
43	TrPC	PCLK Rise Time		10		5	
44	TfPC	PCLK Fall Time		10		5	

Notes:

[1] Parameter does not apply to Interrupt Acknowledge transactions.

[2] Parameter applies only between transactions involving the SCC.

[3] Float delay is defined as the time required for a ±0.5V change in the output with a maximum DC load and a minimum AC load.

[4] Open-drain output, measured with open-drain test load.

[5] Parameter is system dependent. For any Z-SCC in the daisy chain. TdAS(DSA) must be greater than the sum of TdAS(IEO) for the highest priority device in the daisy chain. TslEl(DSA) for the Z-SCC, and TdIElf(IEO) for each device separating them in the daisy chain.

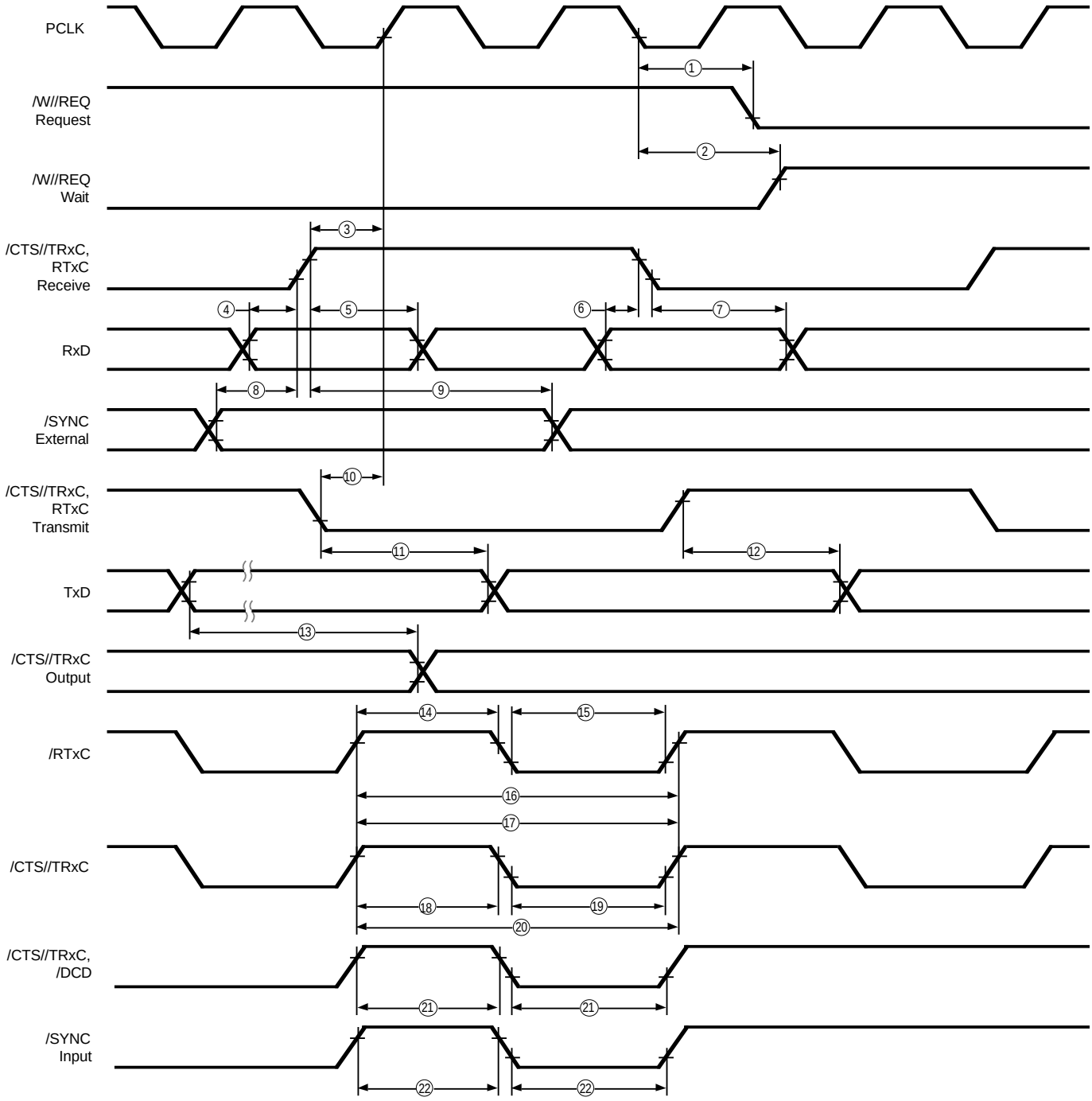
[6] Parameter applies only to a Z-SCC pulling INT Low at the beginning of the Interrupt Acknowledge transaction.

[7] Internal circuitry allows for the reset provided by the Z8 to be recognized as a reset by the Z-SCC. All timing references assume 2.0V for a logic "1" and 0.8V for a logic "0".

* Units in nanoseconds (ns).

AC CHARACTERISTICS

Z80230 General Timing Diagram



Z80230 General Timing Diagram

AC CHARACTERISTICS

Z80230 General Timing Table

No	Symbol	Parameter	10 MHz Min	10 MHz Max	16 MHz Min	16 MHz Max	Notes*
1	TdPC(REQ)	/PCLK Low to W/REQ Valid		200		110	
2	TsPC(W)	/PCLK Low to Wait Inactive		300		180	
3	TsRXC(PC)	/RxC High to /PCLK High Setup Time	NA		NA		[1,4]
4	TsRXD(RXCr)	RxD to /RxC High Setup Time	0		0		[1]
5	ThRXD(RxCr)	RxD to /RxC High Hold Time	125		60		[1]
6	TsRXD(RXCf)	RxD to /RxC Low Setup Time	0		0		[1,5]
7	ThRXD(RXCf)	RxD to /RxC Low Hold Time	125		60		[1,5]
8	TsSY(RXC)	SYNC to /RxC High Setup Time	-150		-100		[1]
9	ThSY(RXC)	SYNC to /RxC High Hold Time	5TcPc		5TcPc		[1]
10	TsTXC(PC)	/TxC Low to /PCLK High Setup Time	NA		NA		[2,4]
11	TdTXCf(TXD)	/TxC Low to TxD Delay		150		85	[2]
12	TdTxCr(TXD)	/TxC High to TxD Delay		150		85	[2,5]
13	TdTXD(TRX)	TxD to TRxC Delay		140		80	
14	TwRTXh	RTxC High Width	120		80		[6]
15	TwRTXl	TRxC Low Width	120		80		[6]
16a	TcRTX	RTxC Cycle Time	400		244		[6,7]
16b	TxRX(DPLL)	DPLL Cycle Time Min	50		31		[7,8]
17	TcRTXX	Crystal Osc. Period	100	1000	100	1000	[3]
18	TwTRXh	TRxC High Width	120		80		[6]
19	TwTRXl	TRxC Low Width	120		80		[6]
20	TcTRX	TRxC Cycle Time	400		244		[6,7]
21	TwEXT	DCD or CTS Pulse Width	120		70		
22	TwSY	SYNC Pulse Width	120		70		

Notes:

[1] RxC is /RTxC or /TRxC, whichever is supplying the receive clock.

[2] TxC is /TRxC or /RTxC, whichever is supplying the transmit clock.

[3] Both /RTxC and /SYNC have 30 pf capacitors to ground connected to them.

[4] Synchronization of RxC to PCLK is eliminated in divide by four operation.

[5] Parameter applies only to FM encoding/decoding.

[6] Parameter applies only for transmitter and receiver; DPLL and baud rate generator timing requirements are identical to case PCLK requirements.

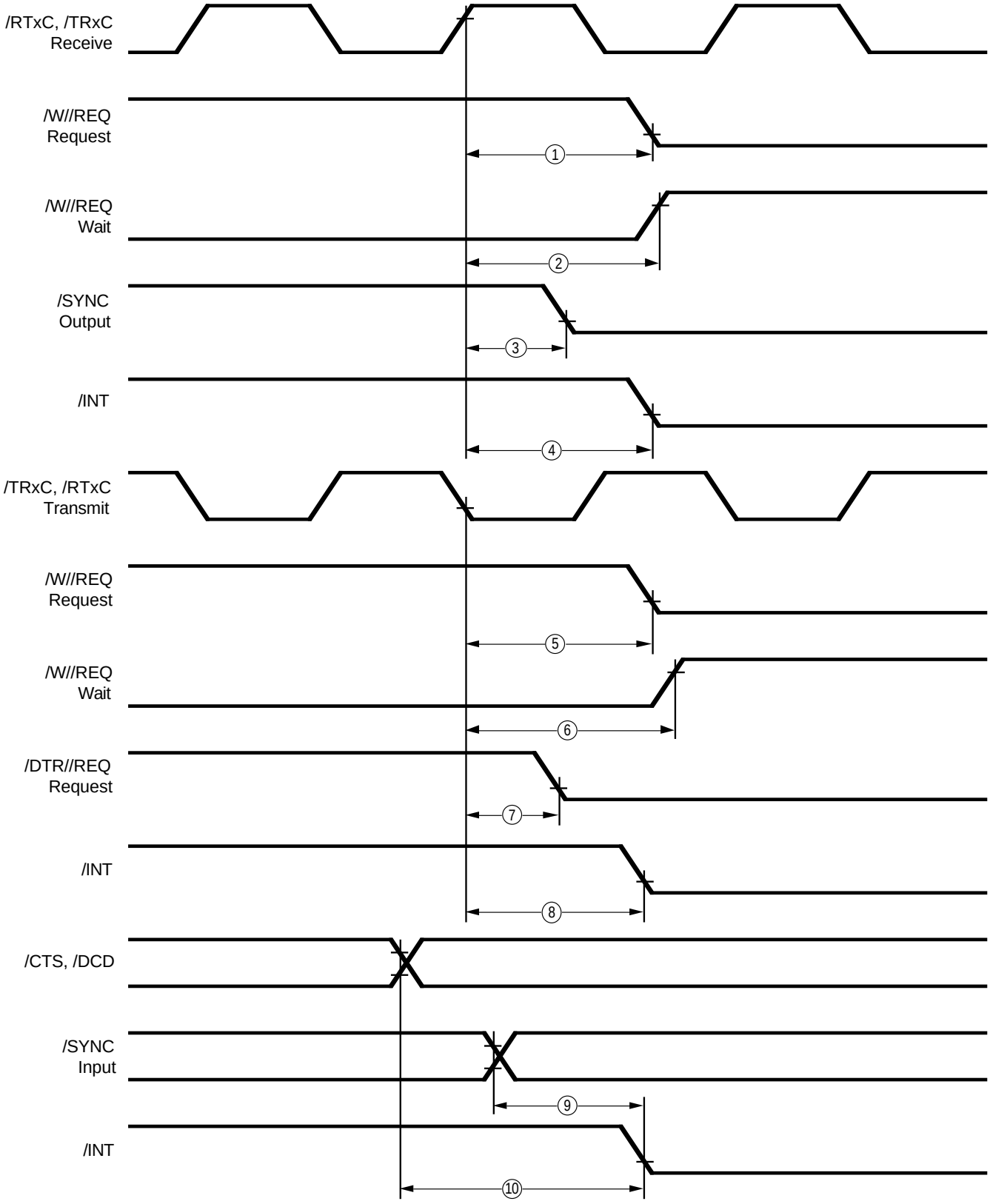
[7] The maximum receive or transmit data rate is 1/4 PCLK.

[8] Applies to DPLL clock source only. Maximum data rate of 1/4 PCLK still applies. DPLL clock should have a 50% duty cycle.

* Units in nanoseconds (ns).

AC CHARACTERISTICS

Z80230 System Timing Diagram



Z80230 System Timing Diagram

AC CHARACTERISTICS

Z80230 System Timing Table

No	Symbol	Parameter	10 MHz Min	10 MHz Max	16 MHz Min	16 MHz Max	Notes*
1	TdRXC(REQ)	/RxC High to W/REQ Valid	13	17	13	17	[2]
2	TdRXC(W)	/RxC High to Wait Inactive	13	19	13	19	[1,2]
3	TdRdXC(SY)	/RxC High to SYNC Valid	4	7	4	7	[2]
4b	TdRXC(INT), Z80230	/RxC High to INT Valid	13	17	13	17	[1,2]
			2	3	+2	+3	[4]
5	TdTXC(REQ)	/TxC Low to W/REQ Valid	11	14	11	14	[3]
6	TdTXC(W)	/TxC Low to Wait Inactive	8	14	8	14	[1,3]
7	TdTXC(DRQ)	/Txc Low to DTR/REQ Valid	9	12	9	12	[3]
8b	TdTXC(INT), Z80230	/TxC Low to /INT Valid	7	9	7	9	[1,3]
			+2	+3	+2	+3	[4]
9	TdSY(INT)	SYNC to INT Valid	2	6	2	6	[1]
			+2	+3	+2	+3	[4]
10b	TdEXT(INT), Z80230		2	3	3	8	[1,4]

Notes:

* Units equal to TcPc.

[1] Open drain-output, measured with open-drain test load.

[2] /RxC is /RTxC or /TRxC, whichever is supplying the receive clock.

[3] /TxC is /TRxC or /RTxC, whichever is supplying the transmit clock.

[4] Units equal to /AS.