



Z85233

EMSCC™ ENHANCED MONO SERIAL COMMUNICATION CONTROLLER

GENERAL DESCRIPTION

The Zilog Enhanced Mono Serial Communication Controller, Z85233 EMSCC, is a software compatible CMOS member of the SCC family introduced by Zilog in 1981. The EMSCC is a full-duplex data communications controller capable of supporting a wide range of popular protocols. The Z85233 EMSCC is a single channel version (Channel A) of Zilog's Z85230 ESCC. Based on Zilog's unique Superintegration™ Technology, the EMSCC is compatible with designs using Zilog's SCC and ESCC to receive and transmit data. It has many improvements that significantly reduce CPU overhead. The addition of a 4-byte transmit FIFO and an 8-byte receive FIFO significantly reduces the overhead required to provide data to, and get data from, the transmitter and receiver.

The EMSCC also has many features that improve packet handling in SDLC mode. The EMSCC will automatically: transmit a flag before the data, reset the Tx Underrun/EOM latch, force the TxD pin high at the appropriate time when using NRZI encoding, deassert the /RTS pin after the closing flag, and better handle ABORTed frames when using the 10x19 status FIFO. The combination of these features along with the deeper data FIFOs significantly simplifies SDLC driver software.

The CPU hardware interface has been simplified by relieving the databus setup time requirement and supporting the software generation of the interrupt acknowledge signal (/INTACK). These changes allow an interface with less external logic to many microprocessor families while maintaining compatibility with existing designs. I/O handling of the EMSCC is improved over the SCC with faster response of the /INT and /DTR//REQ pins.

The many enhancements added to the EMSCC permits a system design that increases overall system performance with better data handling and less interface logic.

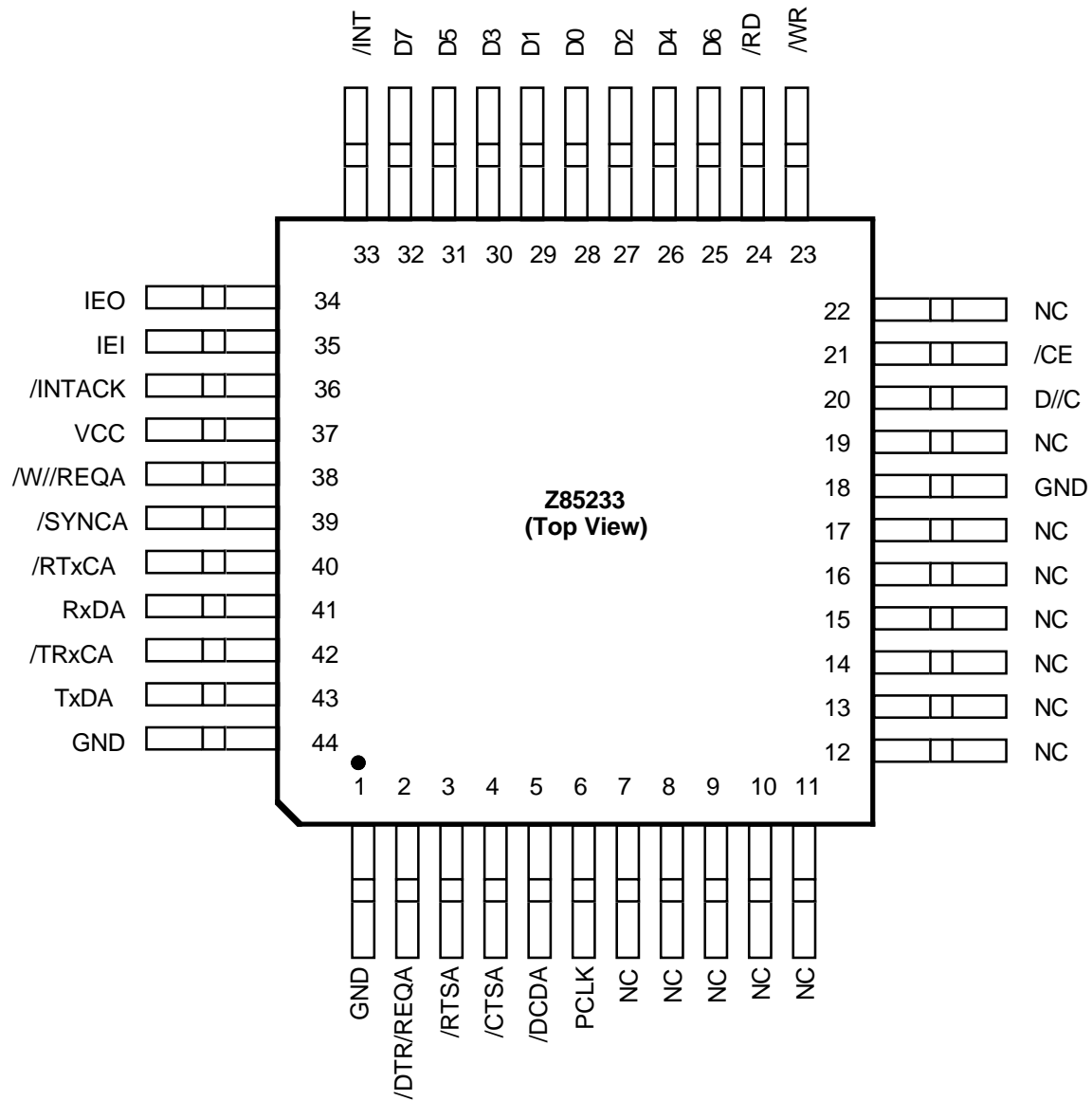
Notes:

All Signals with a preceding front slash, "/", are active Low, e.g.: B//W (WORD is active Low); /B/W (BYTE is active Low, only).

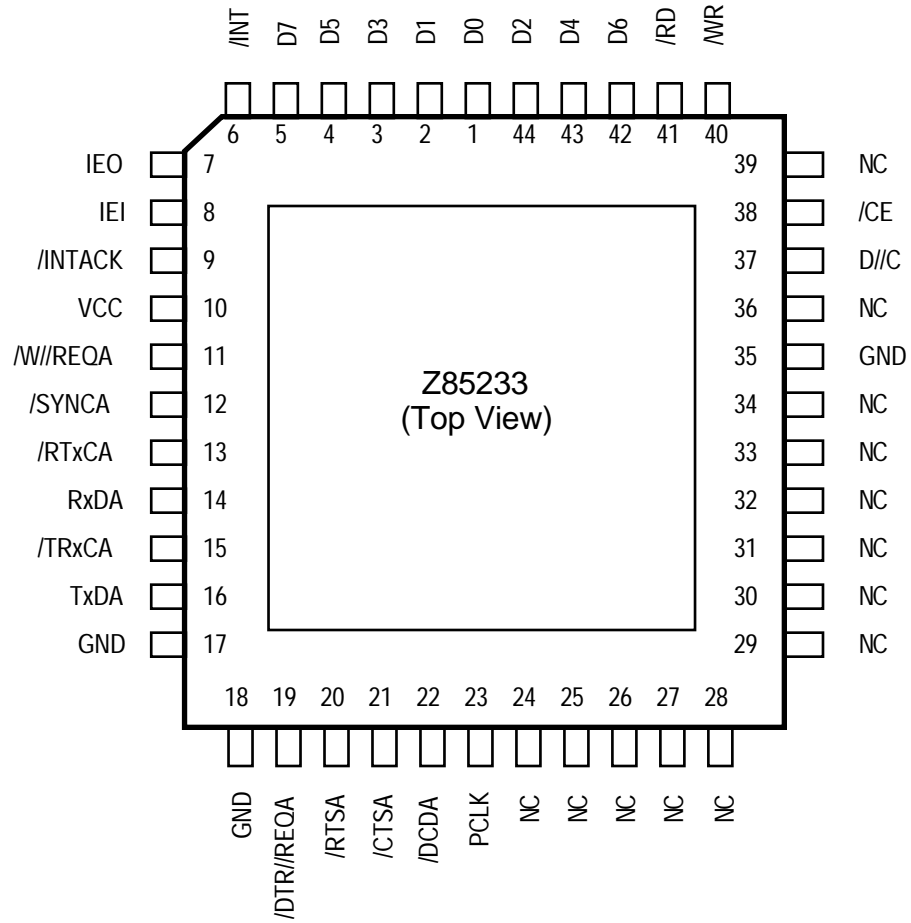
Power connections follow conventional descriptions below:

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

PIN DESCRIPTIONS



Z85233 PQFP Pin Assignments



Z85233 PLCC Pin Assignments

ABSOLUTE MAXIMUM RATINGS

V_{CC} Supply Voltage range -0.3V to +7.0V
 Voltages on all pins
 with respect to GND -0.3V to V_{CC} +0.3V
 Operating Ambient
 Temperature See Ordering Information
 Storage Temperature -65°C to +150°C

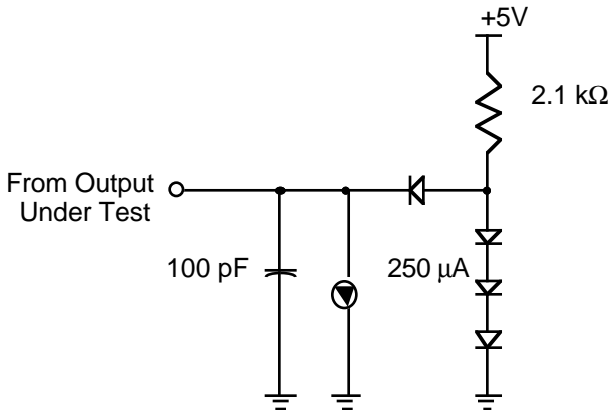
Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

STANDARD TEST CONDITIONS

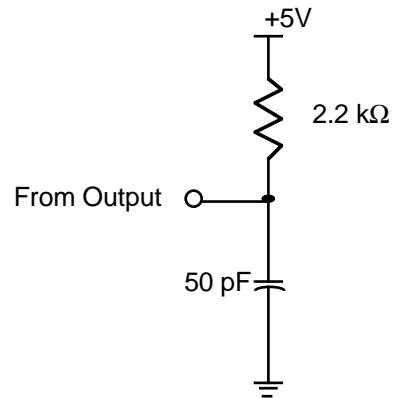
The DC Characteristics and capacitance sections below apply for the following standard test conditions, unless otherwise noted. All voltages are referenced to GND. Positive current flows into the referenced pin.

Standard conditions are as follows:

- $+4.50\text{ V} \leq V_{CC} \leq +5.50\text{ V}$
- $\text{GND} = 0\text{ V}$
- T_A as specified in Ordering Information



Standard Test Load



Open-Drain Test Load

CAPACITANCE

Symbol	Parameter	Min	Max	Unit	Test Condition
C_{IN}	Input Capacitance		10	pF	Unmeasured pins returned to ground.
C_{OUT}	Output Capacitance		15	pF	
$C_{I/O}$	Bidirectional Capacitance		20	pF	

Note:

f = 1 MHz, over specified temperature range.

MISCELLANEOUS

Gate Count - 7000

DC CHARACTERISTICS

Z85233

Symbol	Parameter	Min	Typ	Max	Unit	Condition
V_{IH}	Input High Voltage	2.2		$V_{CC}+0.3$	V	
V_{IL}	Input Low Voltage	-0.3		0.8	V	
V_{OH1}	Output High Voltage	2.4			V	$I_{OH} = -1.6 \text{ mA}$
V_{OH2}	Output High Voltage	$V_{CC}-0.8$			V	$I_{OH} = -250 \mu\text{A}$
V_{OL}	Output Low Voltage			0.4	V	$I_{OL} = +2.0 \text{ mA}$
I_{IL}	Input Leakage			± 10.0	μA	$0.4 < V_{IN} < +2.4\text{V}$
I_{OL}	Output Leakage			± 10.0	μA	$0.4 < V_{OUT} < +2.4\text{V}$
I_{CC1}	V_{CC} Supply Current		4	8 (10 MHz)	mA	$V_{CC}=5\text{V}$ $V_{IH}=4.8$ $V_{IL}=0.2\text{V}$
			5	10 (16 MHz)	mA	Crystal Oscillators off
$I_{CC(\text{OSC})}$	Crystal OSC Current		6		mA	Current for each osc. in addition to I_{CC1}

Notes:

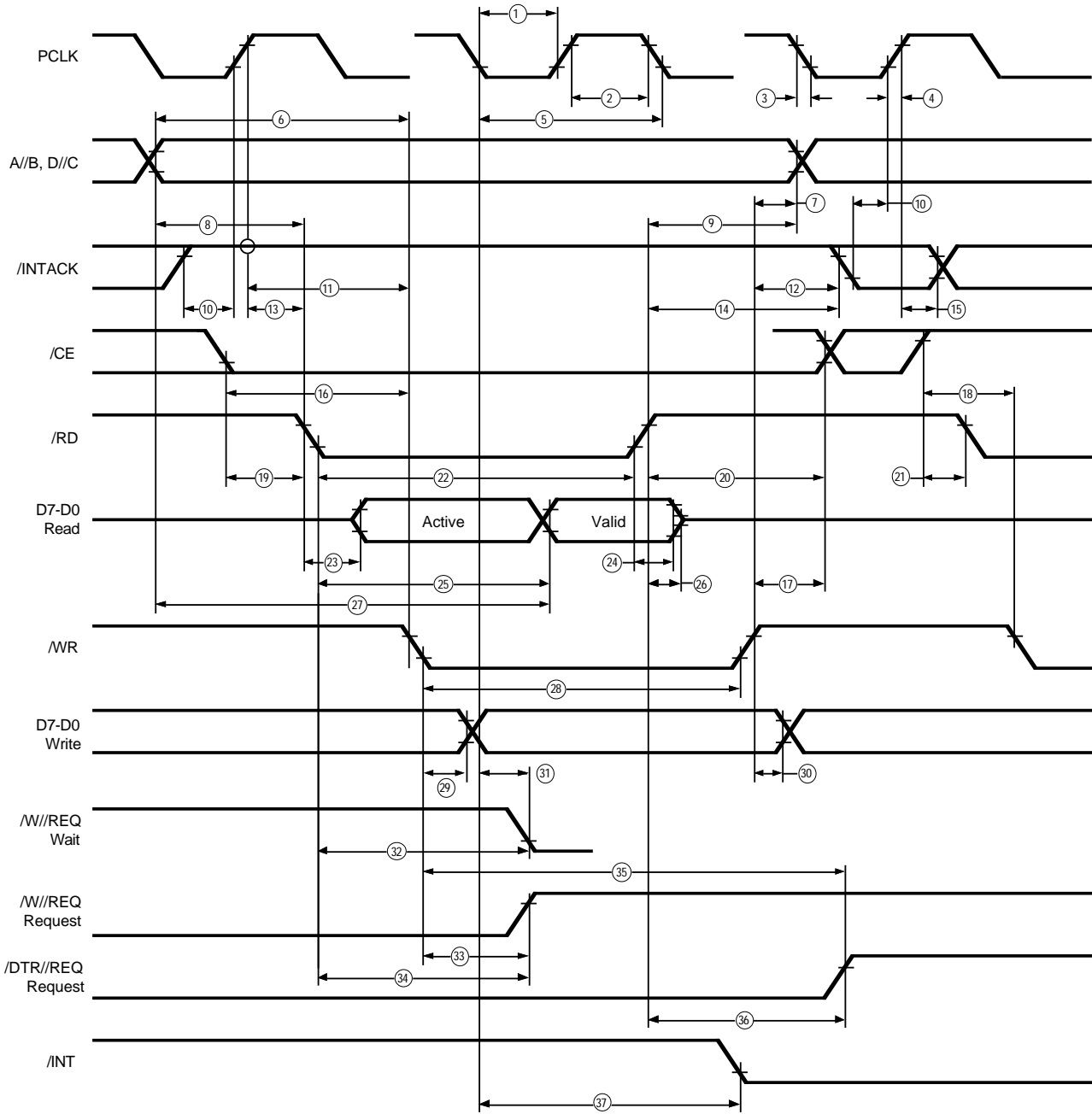
 [1] $V_{CC} = 5\text{V} \pm 10\%$ unless otherwise specified, over specified temperature range.

 [2] Typical I_{CC} was measured with oscillator off.

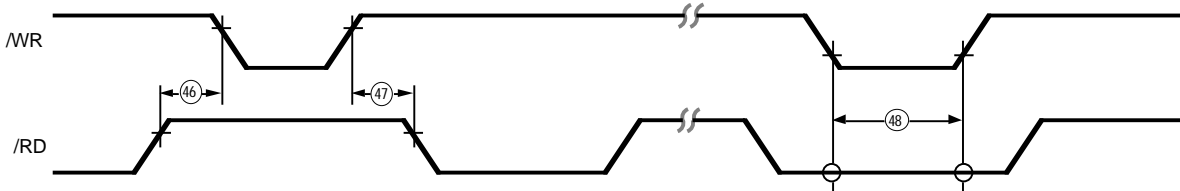
 [3] No $I_{CC(\text{osc})}$ max is specified due to dependency on the external circuit.

AC CHARACTERISTICS

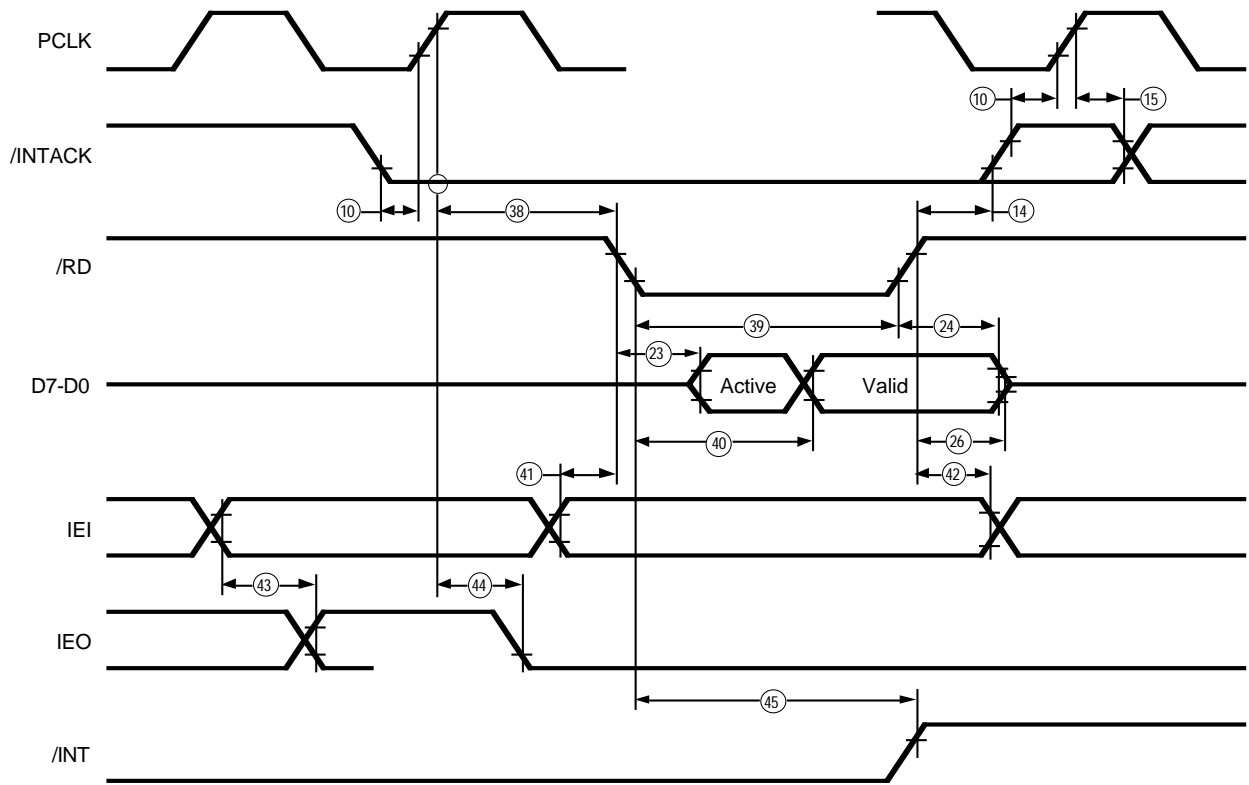
Z85233 Read and Write Timing Diagram



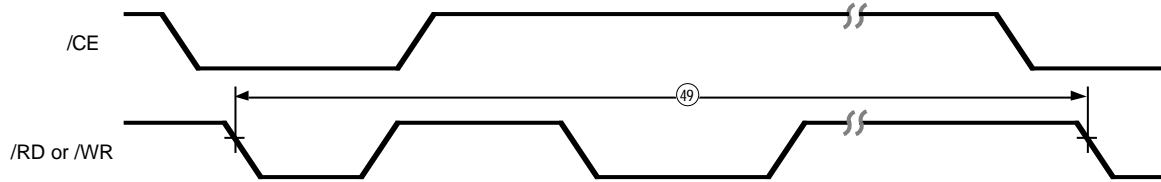
Read and Write Timing Diagram



Reset Timing Diagram



Interrupt Acknowledge Timing Diagram



Cycle Timing Diagram

AC CHARACTERISTICS

Z85233 Read and Write Timing Table

No	Symbol	Parameter	10 MHz		16 MHz		Notes
			Min	Max	Min	Max	
1	TwPCI	PCLK Low Width	40	1000	26	1000	
2	TwPCh	PCLK High Width	40	1000	26	1000	
3	TfPC	PCLK Fall Time		10		5	
4	TrPC	PCLK Rise Time		10		5	
5	TcPC	PCLK Cycle Time	100	2000	61	2000	
6	TsA(WR)	Address to /WR Fall Setup Time	50		35		
7	ThA(WR)	Address to /WR Rise Hold Time	0		0		
8	TsA(RD)	Address to /RD Fall Setup Time	50		35		
9	ThA(RD)	Address to /RD Rise Hold Time	0		0		
10	TsIA(PC)	/INTACK to PCLK Rise Setup Time	20		15		

AC CHARACTERISTICS

Z85233 Read and Write Timing Table

No	Symbol	Parameter	10 MHz		16 MHz		Notes
			Min	Max	Min	Max	
11	TsIAi(WR)	/INTACK to /WR Fall Setup Time	130		70		[1]
12	ThIA(WR)	/INTACK to /WR Rise Hold Time	0		0		
13	TsIAi(RD)	/INTACK to /RD Fall Setup Time	130		70		[1]
14	ThIA(RD)	/INTACK to /RD Rise Hold Time	0		0		
15	ThIA(PC)	/INTACK to PCLK Rise Hold Time	30		15		
16	TsCEI(WR)	/CE Low to /WR Fall Setup Time	0		0		
17	ThCE(WR)	/CE to /WR Rise Hold Time	0		0		
18	TsCEh(WR)	/CE High to /WR Fall Setup Time	50		30		
19	TsCEI(RD)	/CE Low to /RD Fall Setup Time	0		0		[1]
20	ThCE(RD)	/CE to /RD Rise Hold Time	0		0		[1]
21	TsCEh(RD)	/CE High to /RD Fall Setup Time	50		30		[1]
22	TwRDI	/RD Low Width	125	2TcPC	70	2TcPC	[1]
23	TdRD(DRA)	/RD Fall to Read Data Active Delay	0		0		
24	TdRD _r (DR)	/RD Rise to Data Not Valid Delay	0		0		
25	TdRDI(DR)	/RD Fall to Read Data Valid Delay		120		70	
26	TdRD(DRz)	/RD Rise to Read Data Float Delay		35		30	
27	TdA(DR)	Addr to Read Data Valid Delay		180		100	
28	TwWRI	/WR Low Width	125		75		
29	TdWR(DW)	/WR Fall to Write Data Valid Delay		20		20	
30	ThDW(WR)	Write Data to /WR Rise Hold Time	0		0		
31	TdWR(W)	/WR Fall to Wait Valid Delay		100		50	[4]
32	TdRD(W)	/RD Fall to Wait Valid Delay		100		50	[4]
33	TdWRf(REQ)	/WR Fall to /W//REQ Not Valid Delay		120		70	
34	TdRDf(REQ)	/RD Fall to /W//REQ Not Valid Delay		120		70	[6]
35a	TdWRr(REQ)	/WR Fall to /DTR//REQ Not Valid		4TcPc		4TcPc	
35b	TdWRr(REQ)	/WR Fall to /DTR//REQ Not Valid		100		70	[6]
36	TdRD _r (REQ)	/RD Rise to /DTR//REQ Not Valid Delay		NA		NA	
37	TdPC(INT)	PCLK Fall to /INT Valid Delay		320		175	
38	TdIAi(RD)	/INTACK to /RD Fall (Ack) Delay	90		50		[5]
39	TwRDA	/RD (Acknowledge) Width	125		75		
40	TdRDA(DR)	/RD Fall(Ack) to Read Data Valid Delay	120		70		
41	TsIEI(RDA)	IEI to /RD Fall (Ack) Setup Time	95		50		
42	ThIEI(RDA)	IEI to /RD Rise (Ack) Hold Time	0		0		
43	TdIEI(IEO)	IEI to IEO Delay Time		90		45	
44	TdPC(IEO)	PCLK Rise to IEO Delay		175		80	
45	TdRDA(INT)	/RD Fall to /INT Inactive Delay		320		200	[4]
46	TdRD(WRQ)	/RD Rise to /WR Fall Delay for No Reset	15		10		
47	TdWRQ(RD)	/WR Rise to /RD Fall Delay for No Reset	15		10		
48	TwRES	/WR and /RD Low for Reset	100		75		
49	Trc	Valid Access Recovery Time	4TcPc		4TcPc		[3]

Notes:

[1] Parameter does not apply to Interrupt Acknowledge transactions.

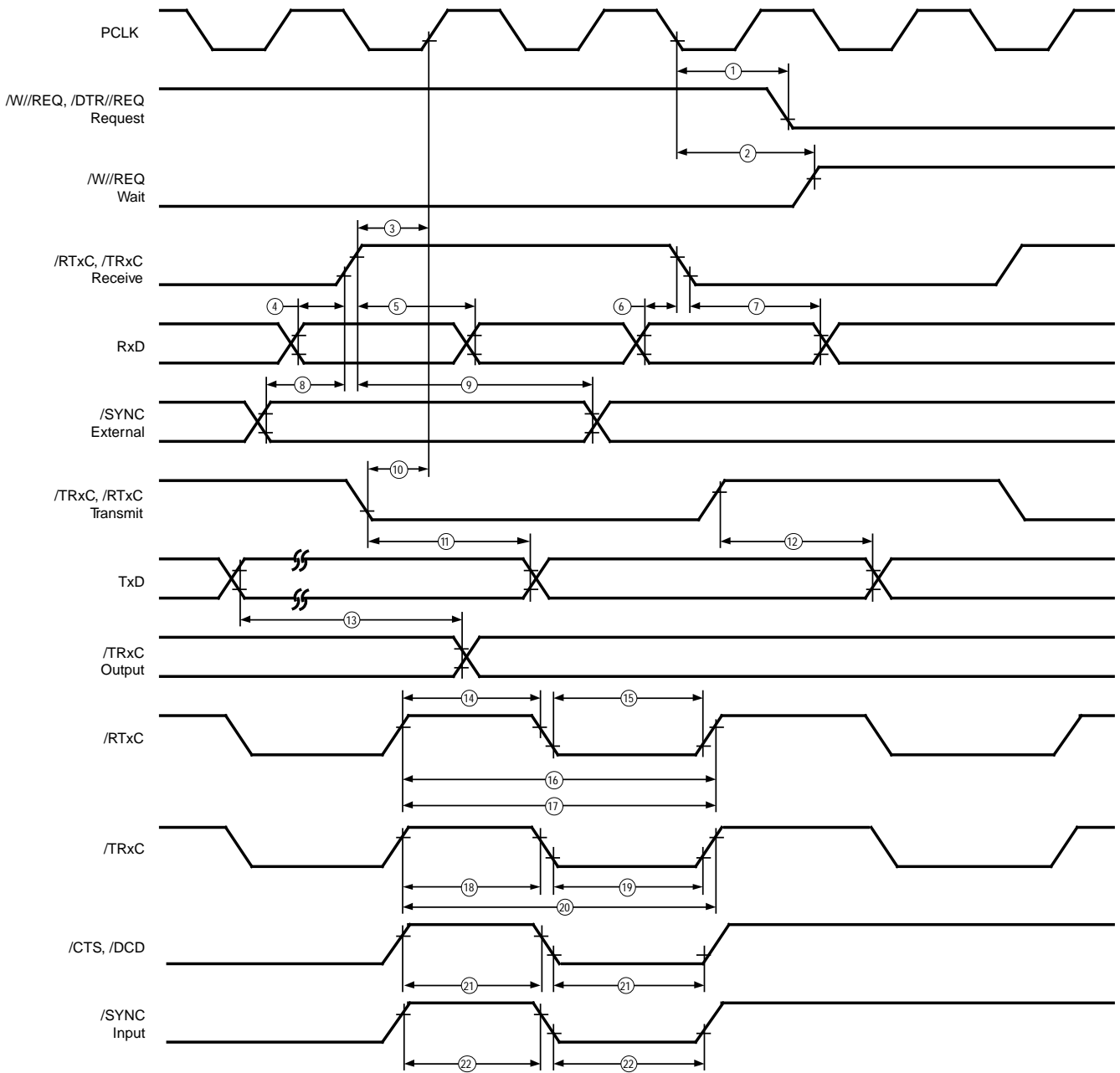
[3] Parameter applies only between transactions involving the EMSCC.

[4] Open-drain output, measured with open-drain test load.

[5] Parameter is system dependent. For any EMSCC in the daisy chain, TdIAi(RD) must be greater than the sum of TdPC(IEO) for the highest priority device in the daisy chain. TsIEI(RDA) for the EMSCC and TdIEI(IEO) for each device separating them in the daisy chain.

[6] Parameter applies to enhanced Request mode only (WR7' D4=1)

AC CHARACTERISTICS
Z85233 General Timing Diagram



General Timing Diagram

AC CHARACTERISTICS

Z85233 General Timing Table (Preliminary)

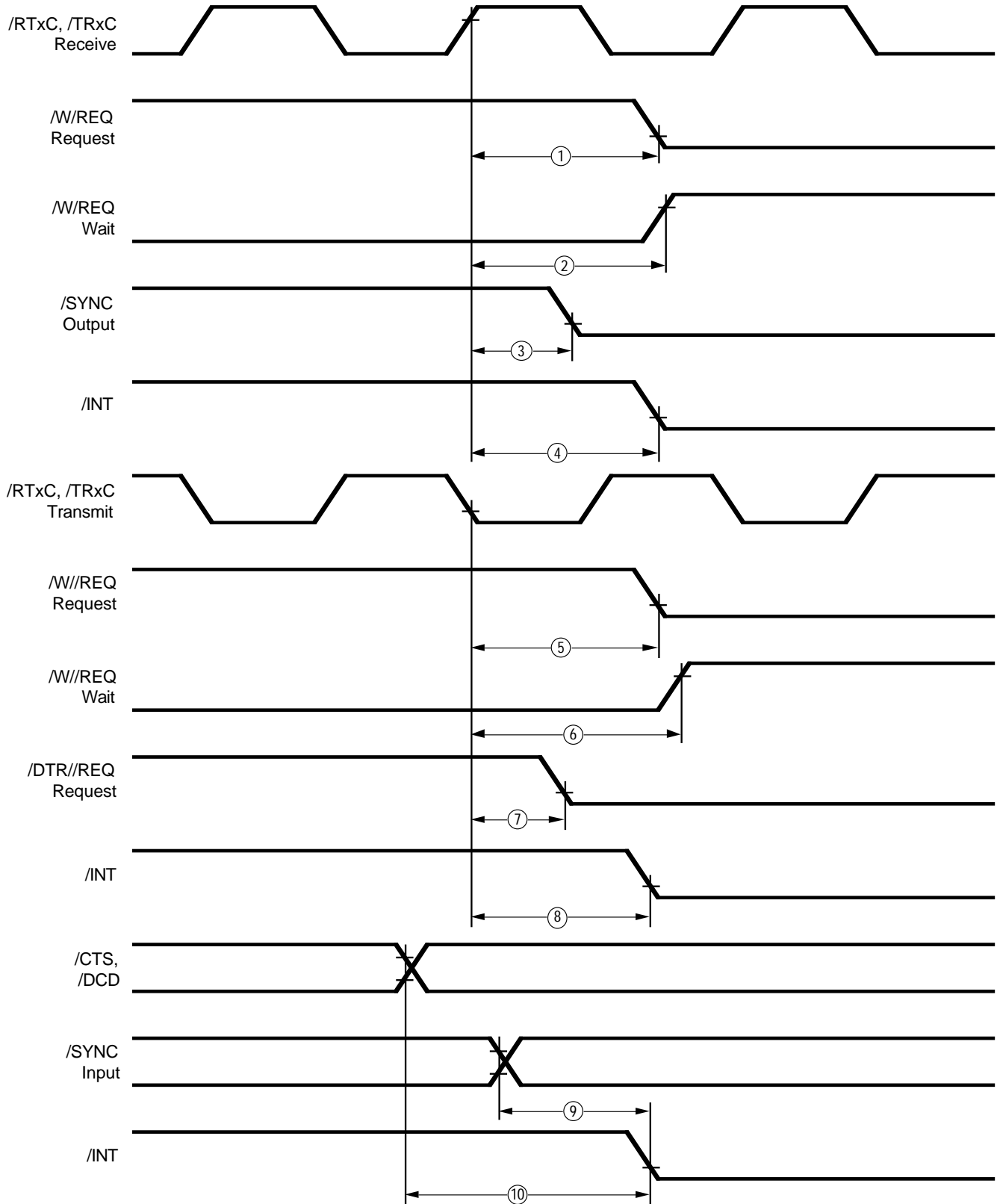
No	Symbol	Parameter	10 MHz		16 MHz		Notes
			Min	Max	Min	Max	
1a	TdPC(REQ)	/PCLK to W/REQ Valid		200		80	
1b	TdPC(REQ)	/PCLK to DTR/ REQ Valid		200		80	[9]
2	TdPC(W)	/PCLK to Wait Inactive		300		180	
3	TsRXC(PC)	/RxC to /PCLK Setup Time	NA	NA	NA	NA	[1,4]
4	TsRXD(RXCr)	RxD to /RxC Setup Time	0		0		[1]
5	ThRXD(RxCr)	RxD to /RXC Hold Time	125		50		[1]
6	TsRXD(RXCf)	RxD to /RXC Setup Time	0		0		[1,5]
7	ThRXD(RXCf)	RxD to /RXC Hold Time	125		50		[1,5]
8	TsSY(RXC)	/SYNC to /RxC Setup Time	-150		-100		[1]
9	ThSY(RXC)	/SYNC to/RXC Hold Time	5TcPc		5TcPc		[1]
10	TsTXC(PC)	/TxC to /PCLK Setup Time	NA		NA		[2,4]
11	TdTXCf(TXD)	/TxC to TxD Delay		150		80	[2]
12	TdTxCr(TXD)	/TxC to TxD Delay		150		80	[2,5]
13	TdTXD(TRX)	TxD to TRxC Delay		140		80	
14	TwRTXh	RTxC High Width	120		80		[6]
15	TwRTXI	TRxC Low Width	120		80		[6]
16a	TcRTX	RTxC Cycle Time	400		244		[6,7]
16b	TxRX(DPLL)	DPLL Cycle Time Min	50		31		[7,8]
17	TcRTXX	Crystal Osc. Period	100	1000	61	1000	[3]
18	TwTRXh	TRxC High Width	120		80		[6]
19	TwTRXI	TRxC Low Width	120		80		[6]
20	TcTRX	TRxC Cycle Time	400		244		[6,7]
21	TwEXT	DCD or CTS Pulse Width	120		70		
22	TwSY	SYNC Pulse Width	120		70		

Notes:

- [1] RxC is /RTxC or /TRxC, whichever is supplying the receive clock.
- [2] TxC is /TRxC or /RTxC, whichever is supplying the transmit clock.
- [3] Both /RTxC and /SYNC have 30 pF capacitors to ground connected to them.
- [4] Synchronization of RxC to PCLK is eliminated in divide by four operation.
- [5] Parameter applies only to FM encoding/decoding.
- [6] Parameter applies only for transmitter and receiver; DPLL and baud rate generator timing requirements are identical to case PCLK requirements.
- [7] The maximum receive or transmit data rate is 1/4 PCLK.
- [8] Applies to DPLL clock source only. Maximum data rate of 1/4 PCLK still applies. DPLL clock should have a 50% duty cycle.
- [9] Parameter applies only when WR7' D4 is set to '1'.

AC CHARACTERISTICS

Z85233 System Timing Diagram (Preliminary)



System Timing

AC CHARACTERISTICS

Z85233 System Timing Table (Preliminary)

No	Symbol	Parameter	10 MHz		16 MHz		Notes [4]
			Min	Max	Min	Max	
1	TdRXC(REQ)	/RXC to /W//REQ Valid	13	17	13	17	[2]
2	TdRXC(W)	/RxC to /Wait Inactive	13	17	13	17	[1,2]
3	TdRXC(SY)	/RxC to /SYNC Valid	4	7	4	7	[2]
4	TdRXC(INT)	/RxC to /INT Valid	15	21	15	21	[1,2]
5	TdTXC(REQ)	/TxC to /W//REQ Valid	11	14	11	14	[3]
6	TdTXC(W)	/TxC to /Wait Inactive	8	14	8	14	[1,3]
7	TdTXC(DRO)	/TxC to /DTR//REQ Valid	9	12	9	12	[3]
8	TdTXC(INT)	/TxC to /INT Valid	5	9	5	9	[1,3]
9	TdSY(INT)	/SYNC to /INT Valid	2	7	2	7	[1]
10	TdEXT(INT)	/DCD or /CTS to /INT Valid	3	8	3	8	[1]

Notes:

- [1] Open-drain output, measured with open-drain test load.
- [2] /RxC is /RTxC or /TRxC, whichever is supplying the receive clock.
- [3] /TxC is /TRxC or /RTxC, whichever is supplying the transmit clock.
- [4] Units equal to TcPc