409509

GEC PLESSEY

SEMICONDUCTORS

3093-1 0

ZN1034D, ZN1034E

PRECISION COUNTER TIMER

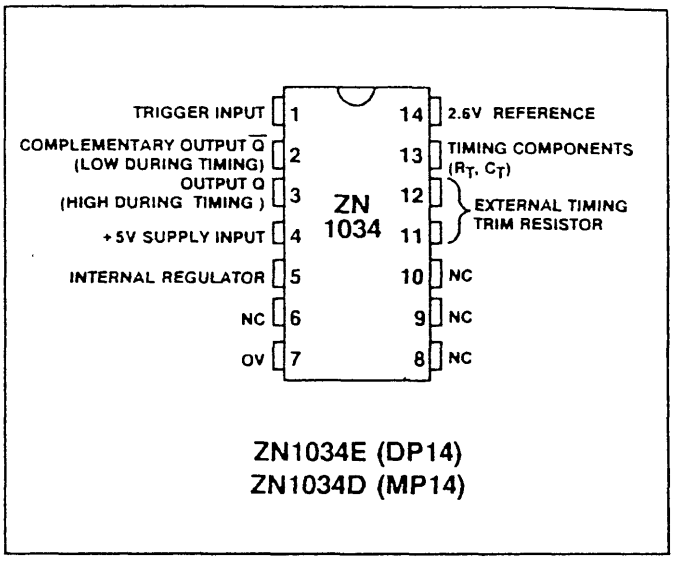
By combining complex linear and digital functions on the same chip, the ZN1034 enables the construction of simple precision timers using low cost components.

The frequency of an on-chip oscillator is determined by an externally connected capacitor and resistor. Fine adjustment of the frequency can be achieved by varying the value of an external trimming resistor. Pulses from the oscillator are fed into a 12 stage binary divider and the output changes state after 4095 pulses.

In this way precise time periods can be defined by timing capacitors and resistors of much smaller values than would be required by a single RC time constant timer.

A control circuit enables the division, or count, to begin when either (a) with trigger input LO the supply goes HI (supply initiation), or (b) with supply HI the trigger input goes LO (trigger initiation).

The IC can operate from normal +5V logic supplies or from any higher voltage by using a suitable voltage dropping resistor and by connecting the internal shunt regulator to the supply pin.



ZN1034E (DP14)
ZN1034D (MP14)

Fig.1 Pin connections - top view

FEATURES

- Time Periods up to 7500 CR
- Time Period Trimming Facility
- Repetitive Timing 0.01%
- Temperature Stability 0.01%/°C
- Complementary TTL Compatible Outputs
- Supply or Trigger Input Timing Initiation
- On-Chip Regulator or TTL Supply Option
- Available in Miniature Plastic DIL (MP14) Package

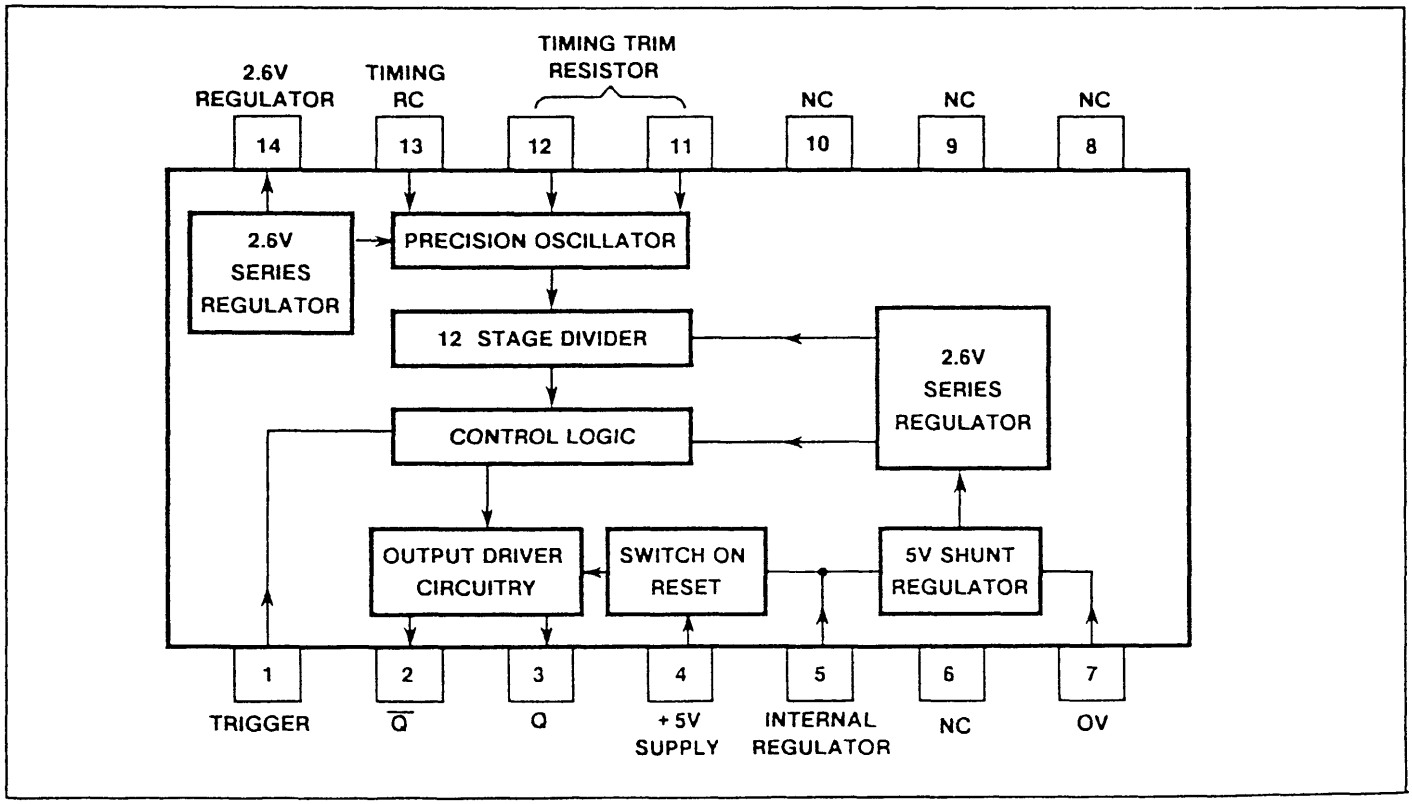


Fig.2 System diagram

ABSOLUTE MAXIMUM RATINGS

Dissipation	250mW derate above 30°C at 5mW/°C
Output source current	25mA
Output sink current	25mA
Operating temperature range	0°C to +70°C
Storage temperature range	-55°C to +125°C

ELECTRICAL CHARACTERISTICS

Test conditions unless otherwise :

T_{amb} = 25°C

		Value				
Characteristic	**Symbol**	**Min.**	**Typ.**	**Max.**	**Unit**	**Conditions**
Timing section						See Note 1
Timing resistor	R_T	3.3k		5M	Ω	See Figs.6 and 7
Timing capacitor	C_T	1			nF	See Figs.6 and 7
Time multiplying factor	K_0		2800			R_{TRIM} = 0
	K_{50}		3700			R_{TRIM} = 50kΩ
						R_T > 12kΩ, C_T > 33nF
Multiplying factor time resistor	R_{TRIM}	0		500	kΩ	See Note 2
Trimming range	T_P		±50		%	R_{TRIM} = 0 to 500kΩ
			±25		%	R_{TRIM} = 0 to 100kΩ
			±12		%	R_{TRIM} = 0 to 50kΩ
Multiplying factor temperature coefficient			±0.01		%/°C	R_{TRIM} = 0
			±0.08		%/°C	R_{TRIM} = 500kΩ
Repetitive timing error			0.01		%	
Multiplying factor linearity			±2		%	1MΩ > R_T > 12kΩ See Fig.7
Multiplying factor/supply voltage coefficient			1		%/V	
External clock input						
Frequency				250	kHz	Clock input to pin 12 via a 10kΩ resistor
Drive current	I_{clk}		0.1		mA	
Pulse width	t_{clk}	1			μs	
Pulse amplitude	V_{clk}	3.0		6	V	
Timing initiation and reset						
(a) Supply voltage initiation						
Voltage to initiate timing	V_{CC}	4.7			V	Supply applied to pin 4 with pin 1 connected to pin 7
Rate of change of V_{CC}				0.25	V/μs	
(b) Trigger input initiation						
Voltage to initiate timing	$V_{T(LO)}$			1	V	Trigger input applied to pin 1
Voltage to prevent initiation of timing	$V_{T(HI)}$	2.2			V	
Minimum pulse to trigger			2		μs	
(c) Supply voltage reset						
Voltage to reset	V_{CC}		3.6		V	See Note 3

ELECTRICAL CHARACTERISTICS (cont.)

		Value				
Characteristic	Symbol	Min.	Typ.	Max.	Unit	Conditions
Output drive Q to $\bar{Q}$						V_{CC} = 5V
Output voltage	$V_{O(HI)}$	2 5	3.6		V	$I_{O(HI)}$ = -25mA
	$V_{O(LO)}$		0.2	0.4	V	$I_{O(LO)}$ = 25mA
Output current	$I_{O(HI)}$			-25	mA	Source
	$I_{O(LO)}$			25	mA	Sink
Rise time	t_r		300		ns	I_O = 5mA, V_{CC} = 5V
Fall time	t_f		100		ns	I_O = 5mA, V_{CC} = 5V
Propagation delay V_T Low to V_O High	t_p		2		μs	
Power supply						
(a) Externally regulated						Connected to pin 4
Supply voltage	V_{CC}	4.7	5.0	5.3	V	
Supply current	I_{CC}		3.5	5.0	mA	V_{CC} = 5V Output unloaded
(b) Internally regulated (5V shunt regulator)						Connect pin 4 to pin 5
Operating current range	I_R	7		55	mA	See Note 4
Regulated voltage	V_R	4.7	5.0	5.3	V	I_R = 10mA
Slope resistance			1		Ω	I_R = 7 - 55mA
Regulated voltage change with temperature			35		mV	I_R = 7 - 55mA t = 0°C to +70°C
Reference voltage (2.6V series regulator)						
Regulated voltage	V_{REF}	2.4	2.6	2.8	V	V_{CC} = 5V pin 14 unloaded
Load current	I_{REF}			5	mA	V_{CC} = 5V
Output resistance			15	40	Ω	
Regulated voltage change with temperature			10		mV	V_{CC} = 5V, t = 0°C to +70°C pin 14 unloaded

NOTES
1. With R_{TRIM} = 100kΩ maximum.
2. For R_{TRIM} > 100kΩ the maximum value of R_T is 1MΩ.
3. In order to reset the timer the supply voltage should be reduced to 2V although reset may be typically achieved at 3.6V. Reset will not occur with the supply greater than 4V.
4. Since the +5V regulator cannot be used on its own without the rest of the circuit, the minimum operating current includes the 5mA maximum supply current taken by the timer circuits.

THE TIMING FUNCTION

Fixed Time Period

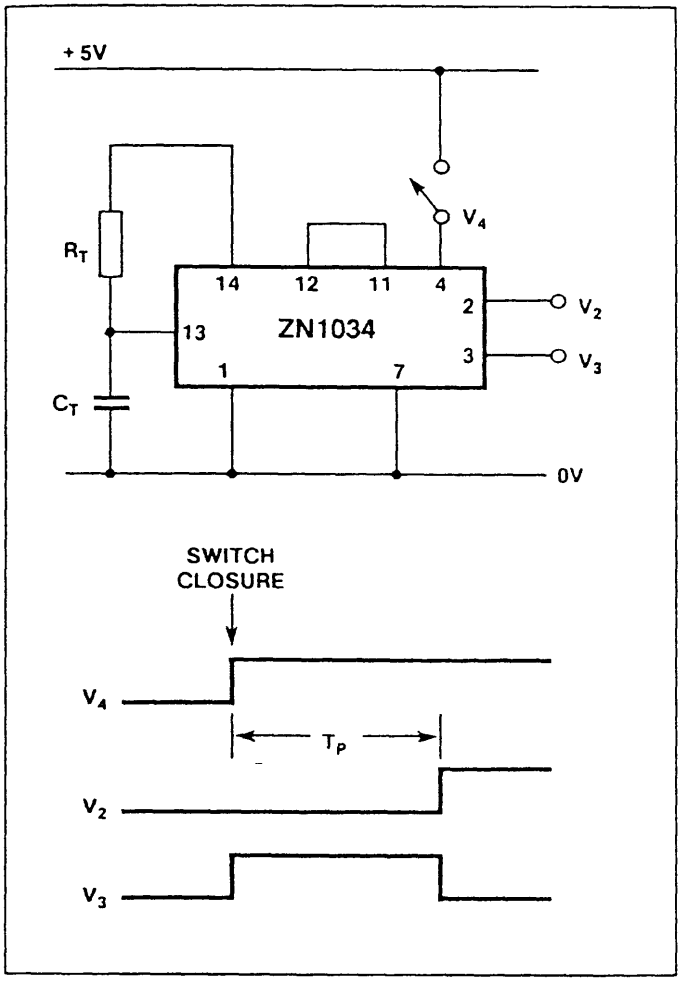


Fig.3

External components R_T and C_T determine the length of the period T_p and if values of R_T > 12kΩ and C_T > 33nF are used then the relationship $T_p = K C_T R_T$ applies and the time multiplying factor K = 2800 ± 10%

(The timing components set the period of an internal oscillator to 0.68 $C_T R_T$ ± 10% and an internal divider causes a change in the output state after 4095 oscillator cycles).

When the time period is initiated pin 3 goes HI for a time period T_p. On completion of the time period, pin 3 goes LO and pin 2, which was previously LO goes HI and remains HI until the timing sequence is re-initiated.

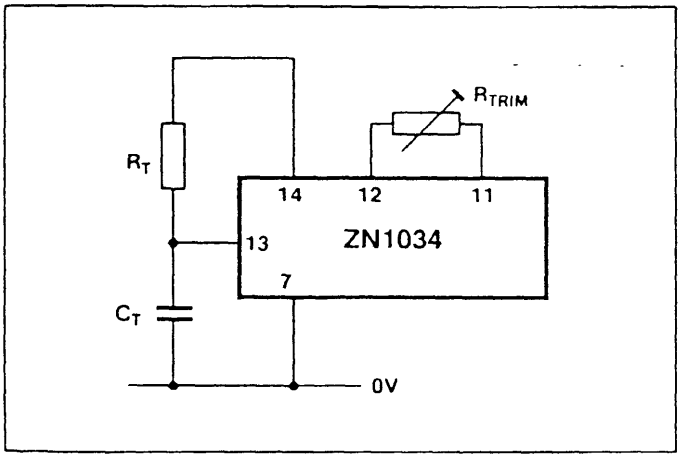


Fig.4

Trimming the Time Period

The time period multiplier K varies with the value of external resistance between pins 11 and 12 (R_{TRIM}). Hence the time period for given values of timing components R_T and C_T can be independently trimmed

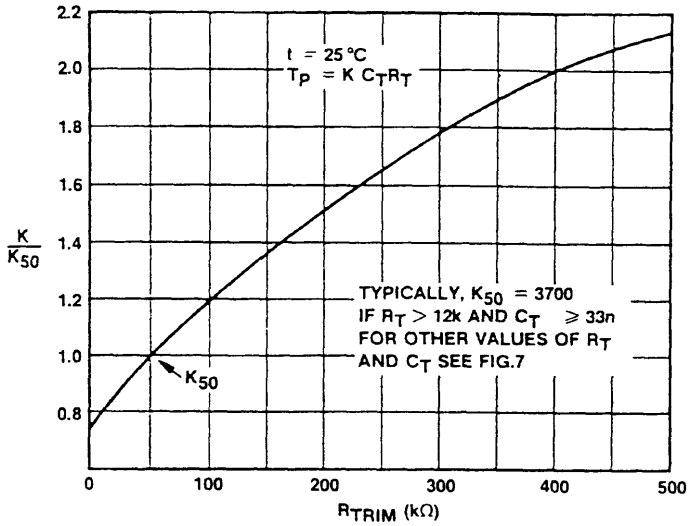


Fig.5

The graph Fig.5 gives the variation of time period multiplier with R_{TRIM} normalised to the value of multiplier obtained for R_{TRIM} = 50kΩ (referred to as K_{50}).

For values of R_T > 12kΩ and C_T > 33nF

Typically K_{50} = 3700 ± 10%

Choosing R_{TRIM} = 50kΩ makes it possible to provide a ±25% trim on the time period obtained when a 100kΩ potentiometer connected between pins 11 and 12 is set at mid-point. Such a trim would enable inexpensive wide tolerance timing components to be used in an accurate timer.

Design of Variable Period Timers

Time periods from 16ms to infinity theoretically may be obtained using the ZN1034 integrated timer circuit However the designer is usually limited by component availability and other restrictions to a narrower range than this. The following section should enable the designer to get the best possible circuit configuration to be achieved within the design limits. The necessary information is presented below in the form of a Timing component guide and a graph of Time period multiplier variation with the time period All graphs have been plotted using a 100k variable resistor set at mid-point for R_{TRIM}

For the component guide and the graph of multiplier against time period the value of R_{TRIM} has been chosen as a 100kΩ variable resistor at mid-point setting thus giving a possible change of approximately ±25% on time periods obtained from the graph

Timing Component Guide

The graph, Fig 6, gives an idea of the values of timing components necessary for a given time period It is plotted assuming a 100kΩ variable resistor between pins 11 and 12 is set at mid-point The periods obtained with the timing components selected from the graph may be trimmed with the variable resistors to the exact time required.

The maximum range possible for a particular value of timing capacitor can easily be obtained from the graph For example, a range of 50ms to 75 seconds can be achieved with a 3 3nF capacitor or 40 seconds to 1000 minutes with 3.3μF.

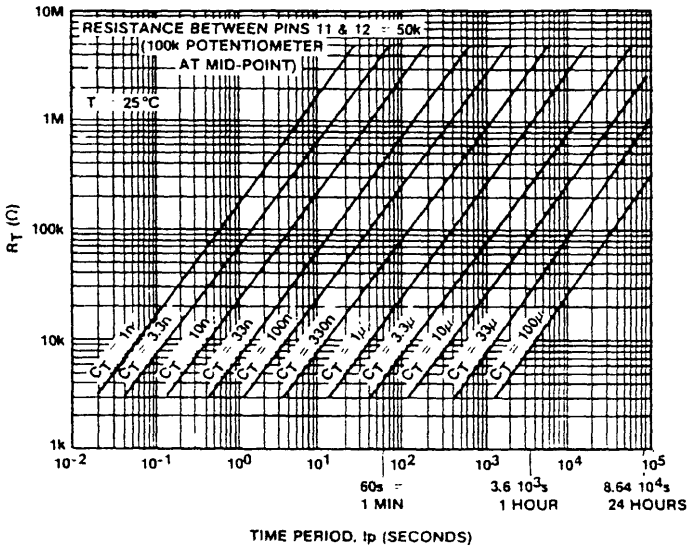


Fig.6

Variation of Time Period Multiplier with Time Period

The linear relationship implied by the equation

$$T_P = K\,C_T R_T$$

is modified when extreme values of timing components are used. Typical variations in the multiplier, K, are shown in Fig.7, again assuming that a 100kΩ variable resistor set at mid-point is connected between pins 11 and 12 Using this graph the example of the 3.3nF capacitor which was used to illustrate the timing component guide graph above will be seen to give a slightly different range, 52ms to 74 seconds for a 3.3kΩ to 5MΩ change in R_T

The multiplier (K_{50}), for this example, varies from a minimum of 4200 to a maximum of 4975, a total variation of ±8.5%.

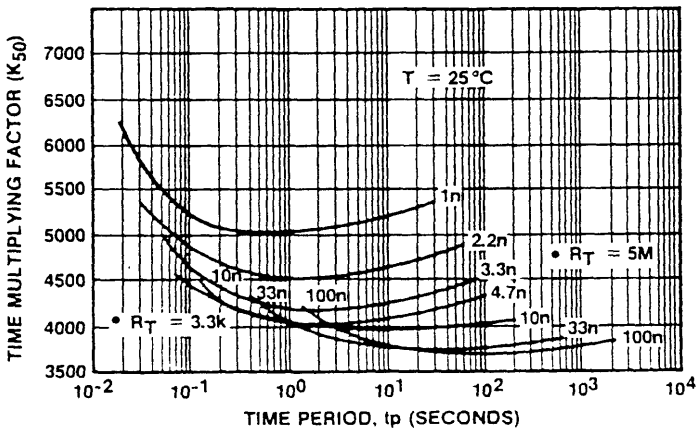


Fig.7

Fig.7 may be used to determine the linearity of the time period variation with timing resistance for various values of timing capacitor and for various ranges of time period as illustrated by the following examples.

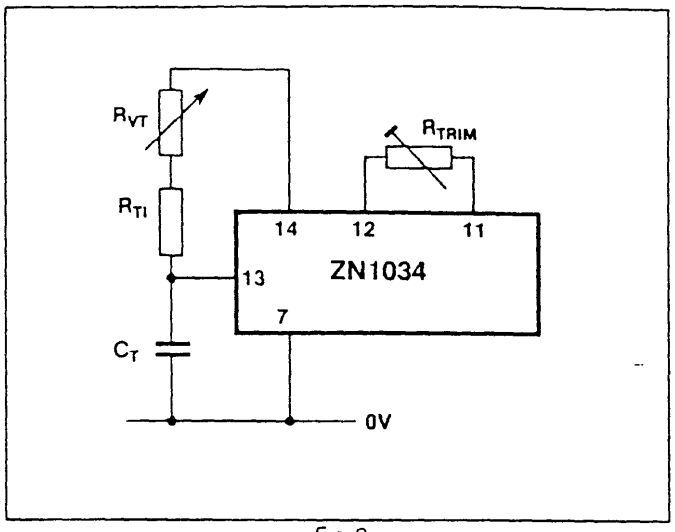


Fig.8

Designing a 1500 : 1 Variable Timer

A wide range continuously variable timer circuit is shown in Fig.8 and if the values of the above example are used then a variation of approximately 1 : 1500 is obtained (or 50ms : 75 seconds).

For $R_{TI} = 3.3k\Omega$
$R_{VT} = 5M\Omega$
$R_{TRIM} = 50k\Omega$ (100kΩ variable resistor set to mid-point)
$C_T = 3.3nF$

The maximum period $T_{P(MAX)} = K\,C_T (R_{VT} + R_{TI})$ and the minimum period $T_{P(MIN)} = K\,C_T R_{TI}$

$$\text{Hence the range is } 1 : \frac{T_{P(MAX)}}{T_{P(MIN)}}$$

$$\text{i.e. } 1 : \frac{R_{VT}}{R_{TI}} + 1$$

$$\text{approximately } 1 : \frac{R_{VT}}{R_{TI}}$$

If the variable resistor R_{VT} is scaled linearly in terms of time period then the predicted linearity error for Fig.7 will be ±8 5%.

A 400 : 1 Linearly Variable Timer

Restricting the range to about 400 : 1 enables the designer to achieve a better linearity than the 1500 : 1 timer. The design of the circuit of Fig.9 illustrates this point.

$R_{T(MAX)} = 5M\Omega$
$R_{T(MIN)} = 12k\Omega$
$C_T = 33nF$
$R_{TRIM} = 50k\Omega$

$$\text{range is } 1. \frac{5 \times 10^6}{12 \times 10^3} + 1$$

i e. 1 418

The values selected are such as to give approximately

$T_{P(MIN)}$ = 1 5 seconds from graph, Fig.6
and $T_{P(MAX)}$ = 10 minutes from graph, Fig.6

These values are used to obtain those of K_{50} from the graph of Fig.7.

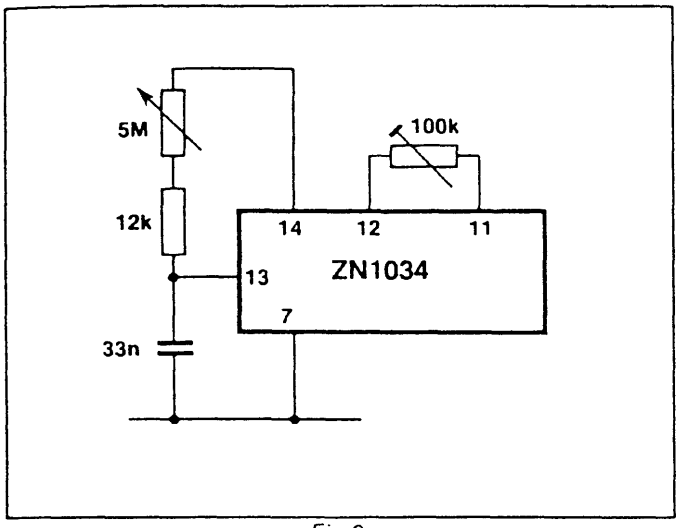


Fig.9

The maximum value of K_{50} = 3950 from Fig.7 and the minimum value of K_{50} = 3800 from Fig.7.

This indicates that the maximum linearity error is ±2%. (Excluding errors due to R_{VT} end resistance at minimum settings).

A wide range timer with switched timing resistors can be designed in a similar manner to the circuit shown in Fig.8.

Switched resistors are preferable in some circumstances for setting the time period of timer circuits. In addition to the ability to set a time precisely, advantage can be taken of the capability of the ZN1034 circuit of operating linearly over a wide range of values of timing resistor up to 5M. There is also the possibility of correcting for errors at the extremes of the range if this is thought worthwhile.

The design of the timer illustrated in Fig.10 can be taken as an example. Here the aim is to achieve a 0.1 to 99.9 second range with an accuracy consistent with the use of 1% resistors.

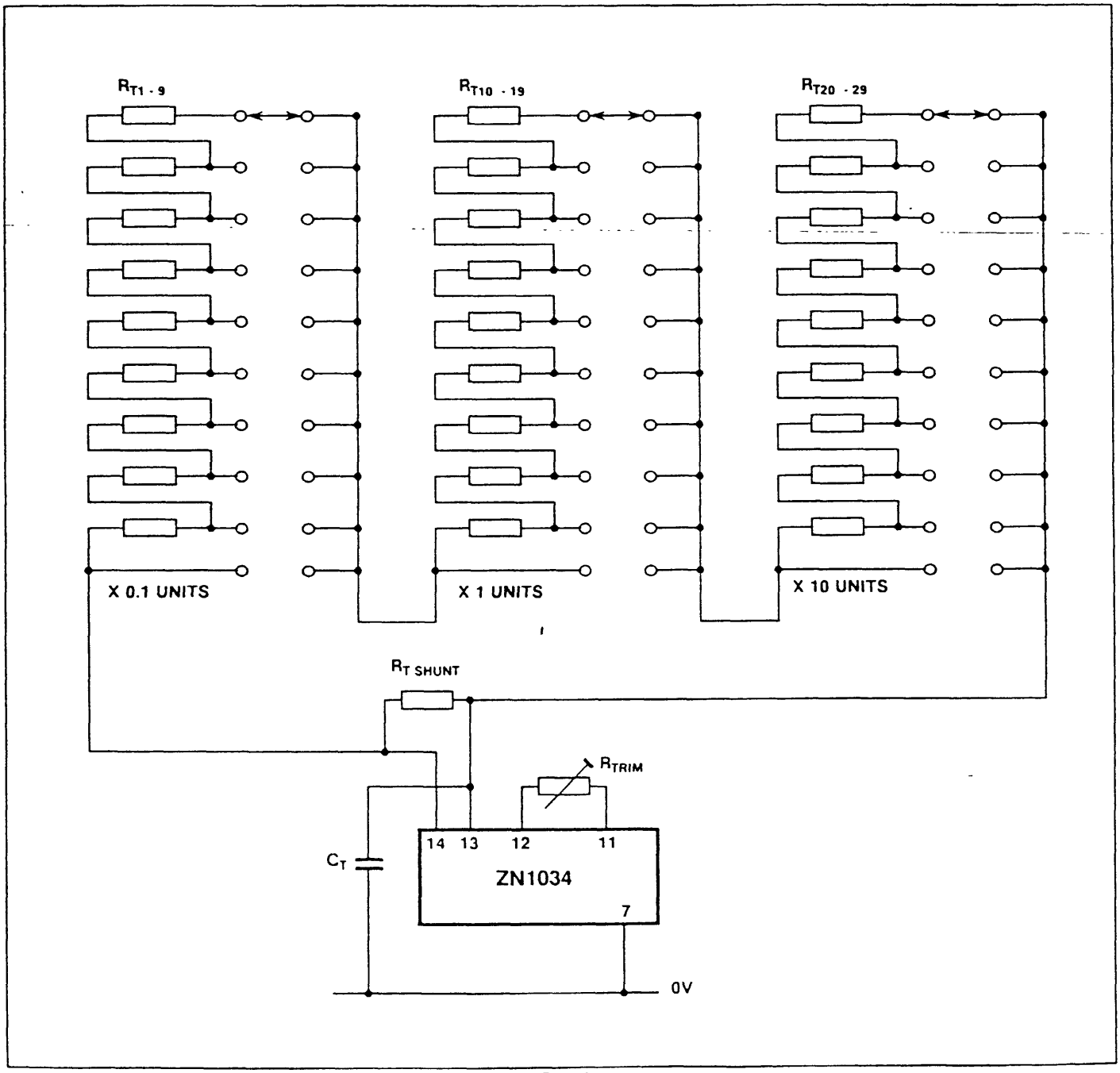


Fig.10

Fig.6 shows that for the maximum time of about 100 seconds R_T is required to be about 5MΩ and the value of C_T to be between 3.3nF and 10nF.

Fig.7 indicates that a 4.7nF capacitor will give 100 seconds with 5MΩ and the 4.7nF curve shows a minimum value of K_{50} of 4030 at 2 seconds and a value of 4280 at 100 seconds, an error of +7% on the linearity taking 2 seconds as standard.

Such a steady increase of time error can be corrected by shunting the switched resistors by the appropriate high value, $R_{T(SHUNT)}$. The value required in this particular case will be such as to reduce $R_{T(MAX)}$ by 6%.

$$\text{i.e. } R_{T(SHUNT)} = 5M\Omega\left[\frac{100-6}{6}\right]$$

$$= 82M\Omega \text{ (nearest preferred value)}$$

This will have no effect on the linearity error at the bottom end of the range.

Assuming the effect of the variation in multiplying factor over the production spread of devices and also the capacitor tolerance is trimmed out by R_{TRIM} we can specify the resistors as:

$$R_{T1} - R_{T9} = 5.1k\Omega \pm 0.5\%$$
$$R_{T10} - R_{T19} = 51k\Omega \pm 0.5\%$$
$$R_{T20} - R_{T29} = 510k\Omega \pm 0.5\%$$
$$\text{and } C_T = 4.7nF \pm 5\%$$

Typical errors derived from the graph shown in Fig.7 (multiplying factor against time), are shown in Table 1.

NOTES (See Table 1)

1. The timing resistance as specified above but allowing for the effect of an 82MΩ overall shunt resistor (Only the significant values shown).
2. The multiplying factor used in the calculation of the time period should strictly be that pertaining to the calculated time which will differ from the set time by the error. Since this error is small, the error in using the set time to derive the multiplying factor from the graph is negligible.
3. Normalising the error by adjusting the trim resistor to give correct timing on the 10 second setting.
4. The timing resistors as specified above but with 82MΩ overall shunt resistance and a 4.7kΩ in place of a 5.1kΩ for the 0.1 second position. (Only significant values shown).

Using shunt resistor correction						Using shunt and series resistor			
Timing period setting secs.	Multiplying factor	Timing resistance (Note 1) kΩ	Calculated time (Note 2) seconds	Calculated error %	Normalised error (Note 3) %	Timing resistance (Note 4) kΩ	Calculated time (Note 2) seconds	Calculated error %	Normalised error (Note 3) %
0.1	4475	5.1	0.107	+7	+10	4.7	0.099	-1.2	+1.8
0.2	4230	10.1	0.203	+1.5	+4.5	9.8	0.195	-2.6	+0.4
0.3	4150		0.298	-0.6	+2.4	14.9	0.291	-3.1	-0.1
0.4	4100		0.393	-1.8	+1.2	20.0	0.39	-3.7	-0.7
0.5	4080		0.489	-2.2	+0.8	25.1	0.48	-3.7	-0.7
0.6	4070		0.585	-2.4	+0.6	30.2	0.58	-3.7	-0.7
0.7	4062		0.681	-2.7	+0.3	35.3	0.67	-3.7	-0.7
0.8	4055		0.778	-2.8	+0.2	40.4	0.77	-3.8	-0.8
0.9	4050		0.873	-3.0	0	45.5	0.87	-3.8	-0.8
1.0	4045		0.970	-3.0	0	51.0	0.97	-3.0	0
1.1	4040		1.07	-3.2	-0.2	55.7	1.06	-3.9	-0.9
1.2	4040		1.16	-3.2	-0.2	60.8	1.15	-3.8	-0.8
1.3	4040		1.26	-3.2	-0.2	65.9	1.25	-3.7	-0.7
1.4	4040		1.36	-3.2	-0.2	71.0	1.35	-3.7	-0.7
1.5	4040		1.45	-3.2	-0.2	76.1	1.44	-3.7	-0.7
1.9	4040		1.84	-3.2	-0.2	96.5	1.83	-3.6	-0.6
2.0	4040		1.94	-3.2	-0.2	102.0	1.94	-3.2	-0.2
2.1	4040		2.03	-3.2	-0.2	106.7	2.03	-2.5	-0.5
3.0	4040		2.90	-3.2	-0.2	153.0	2.91	-3.2	-0.2
10.0	4070	507	9.70	-3.0	0	507.0	9.70	-3.0	0
11.0	4075	557	10.67	-3.0	0				0
13.0	4080	658	12.61	-3.0	0				0
20.0	4110	1008	19.46	-2.7	+3.0				+0.3
30.0	4150	1502	29.30	-2.3	+0.7				+0.7
80.0	4260	3889	77.86	-2.7	+0.3				+0.3
90.0	4275	4349	87.4	-2.9	+0.1				+0.1
99.9	4280	4800	96.6	-3.3	-0.3		96.6		-0.3

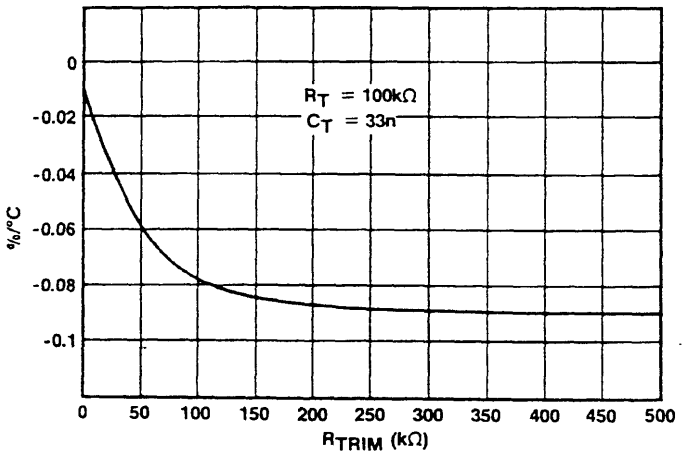
Table 1

The predicted maximum error is approximately ±5% of setting overall but with a shunt resistor across the switched resistors this can be reduced to ±0.5% for settings above 0.4 seconds. By altering one of the switched resistor values in addition to having a shunt resistor the overall predicted error becomes ±1.5% of setting.

N.B. Setting all three decade switches to zero should be avoided since this will disable the oscillator and stop the timer

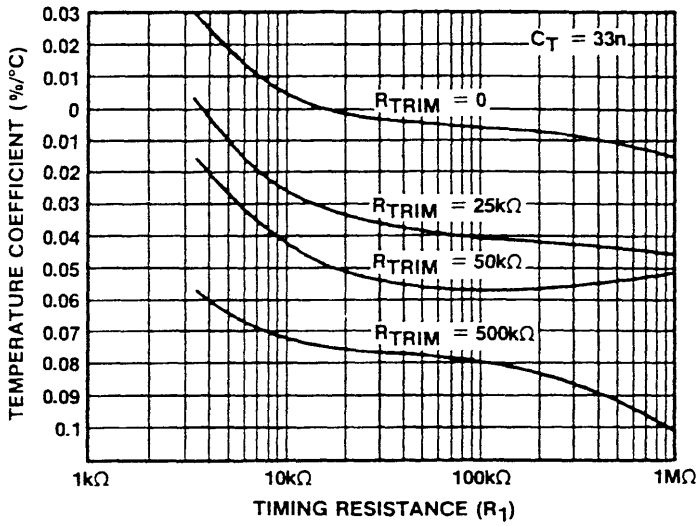
Effect of Temperature on Time Period

For optimum temperature coefficient of time period it is necessary to use as low a resistance as possible between pins 11 and 12 (R_{TRIM}) consistent with the maximum amount of adjustment of the time period required. This is illustrated by the graph Fig.11.



The effect of varying the value of the timing resistance on the time period temperature coefficient is shown in Fig.12.

Optimum temperature coefficient may be obtained with R_{TRIM} = 0, R_T = 20kΩ and C_T > 33nF



INPUT AND OUTPUT CIRCUITS

External Clock

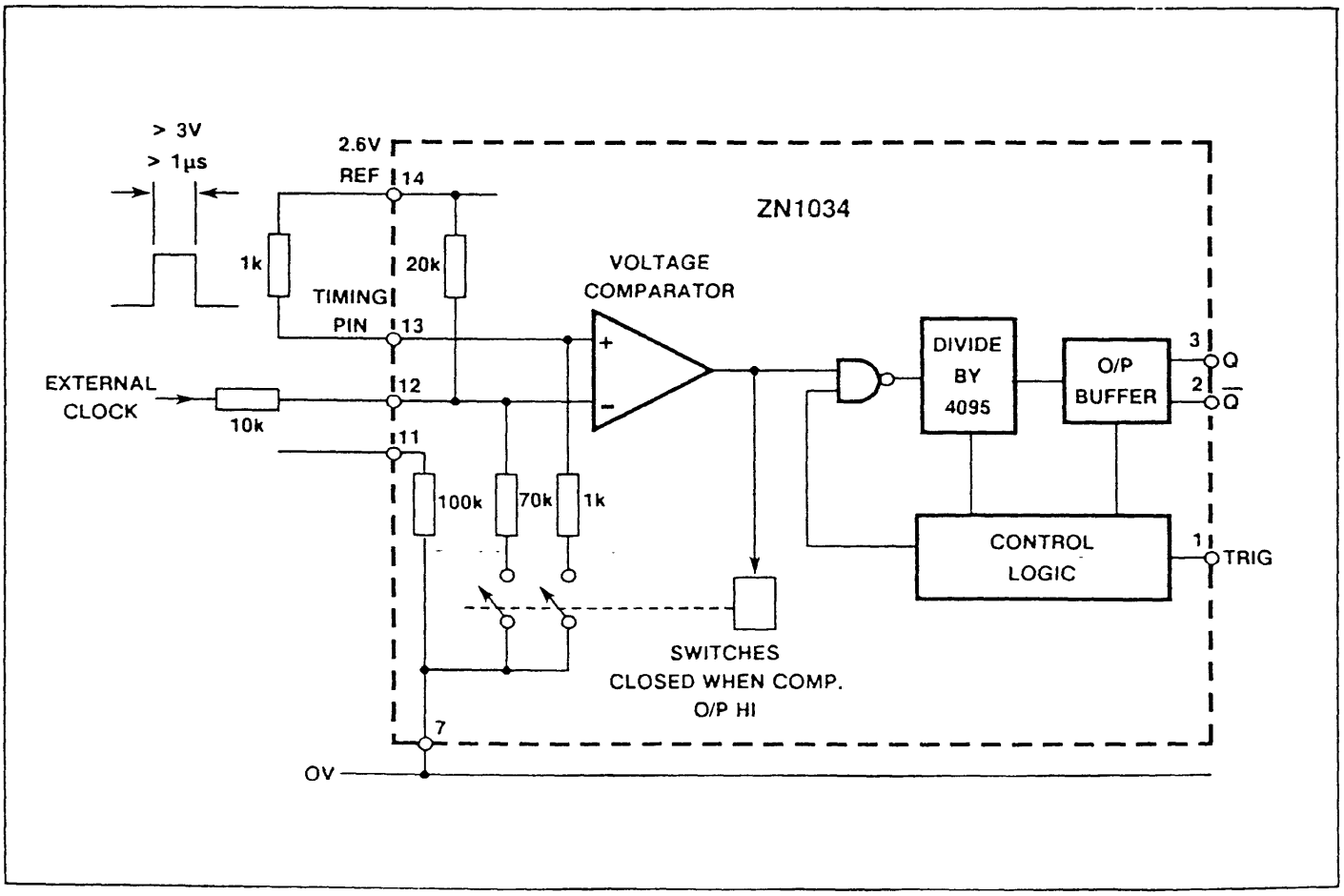


Fig. 13

The ZN1034 can be used with an external clock as shown in the circuit of Fig 13

The internal clock is disabled by connecting a 1k resistor from the timing pin 13 to the +2.5V reference pin 14 thus preventing the non-inverting input to the amplifier dropping below the inverting input voltage. The amplifier output is therefore HI and the internal switches are closed.

An external clock pulse, provided it meets the limits defined in the characteristics, will override the disabling on pin 13 and, if the trigger input on pin 1 is LO, will cause a pulse to be passed to the divider circuit.

The output Q and $\overline{Q}$ will change from LO to HI and vice versa at the end of 4095 external clock pulses.

Timing Initiation and Reset (Fig.14)

Supply Initiated

When pin 1 is held LO and the supply is switched on, the control logic and counter are automatically reset as the supply rises to its ON voltage. This also initiates timing at the same instant by gating the oscillator output into the counter. After the set time (period 1), the outputs change state and remain thus until the supply is switched off or another period is initiated.

If, during such a timing cycle (period 2), the trigger input is taken HI, no matter how many times or for how long, the condition of the outputs and the length of the timing period will not be affected. If the supply drops below the reset level even for a few microseconds then the timing period will be terminated. It will be reset and restarted when the supply rises again above the reset level. Thus a supply drop-out has the effect of increasing the time period, Q output remains low for (period 2) plus (period 3).

Trigger Initiated

Allowing pin 1 to rise with the supply prevents timer initiation by the supply.

Pulling the trigger input LO now initiates a normal timing period (period 4). A further period may be initiated by dropping the trigger LO again (period 5). As for supply initiation, this period is not affected either in duration or in the condition of the outputs when the trigger input level is altered during timing. Similarly the period is terminated by the supply falling below the reset level but since the normal condition of the trigger is HI the timing will not restart on restoration of the supply. A supply drop-out during a trigger initiation timing period has the effect of reducing the set time.

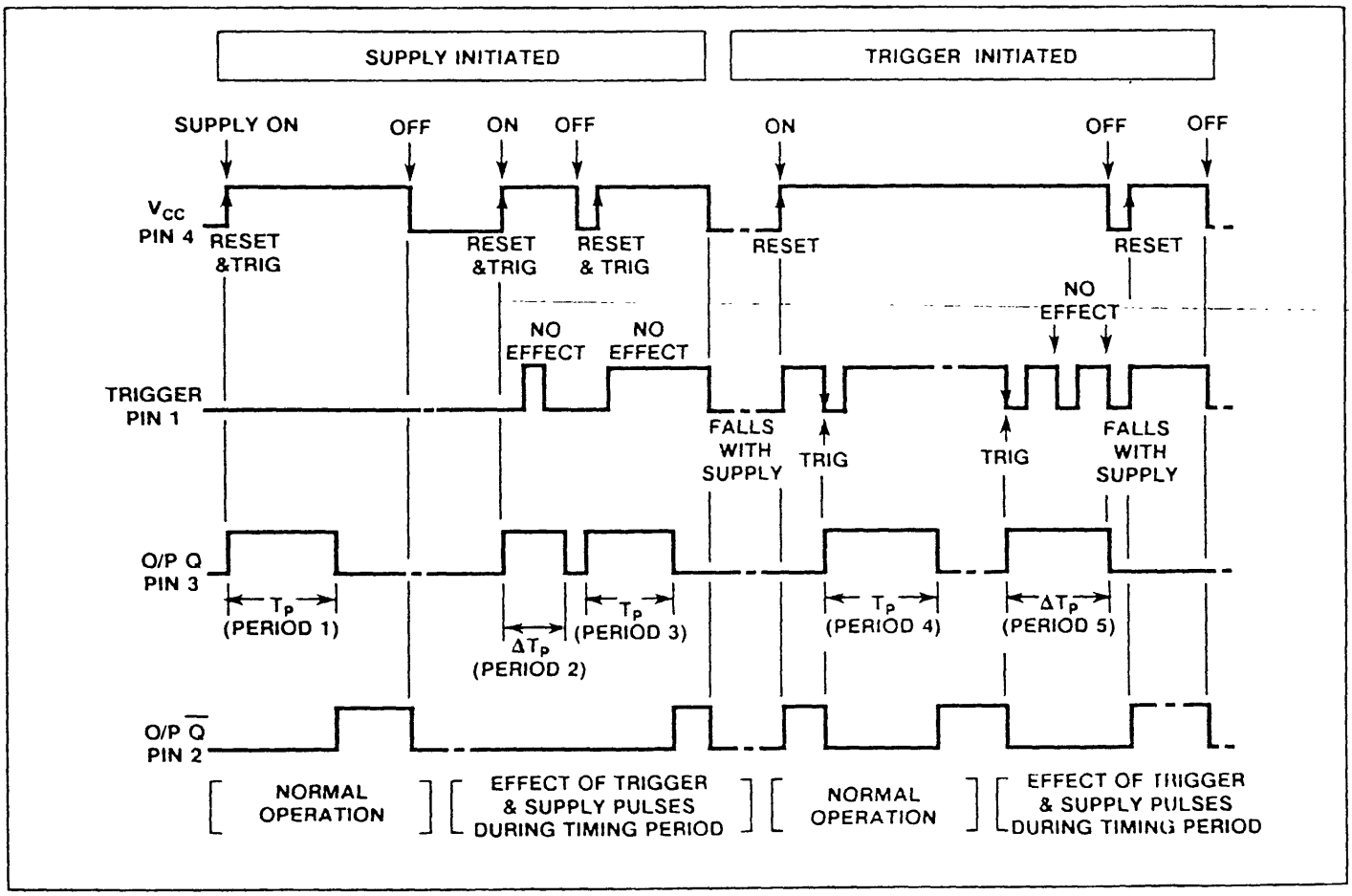


Fig. 14

Trigger Input Circuit (Fig.15)

The input is a Schmitt trigger circuit with a hysteresis of about 0.3V. With no input applied the input is pulled HI thus preventing initiation of the timer. When remote triggering is used with mechanical contacts it is advisable to provide a more positive pull-up of 10kΩ (shown dotted). A contact is then made between pins 1 and 7 to initiate timing.

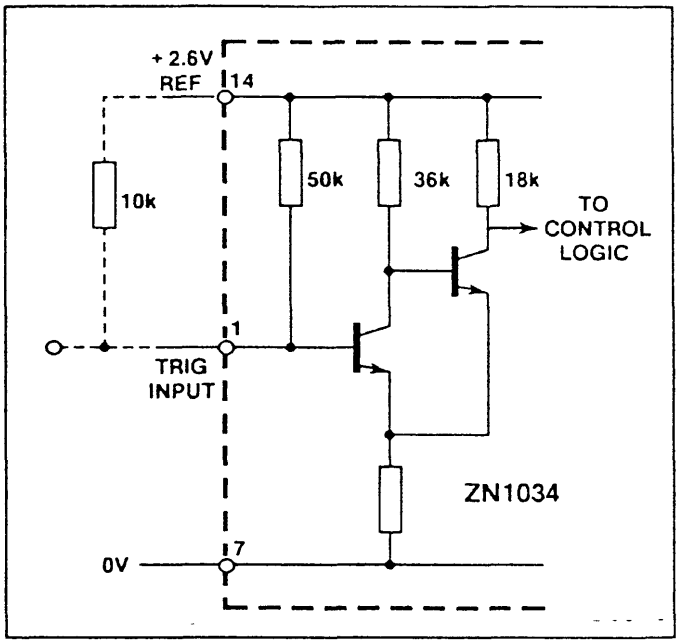


Fig. 15

Output Drive Circuits

The Q and $\overline{Q}$ output drive circuits both have the form illustrated in Fig.16.

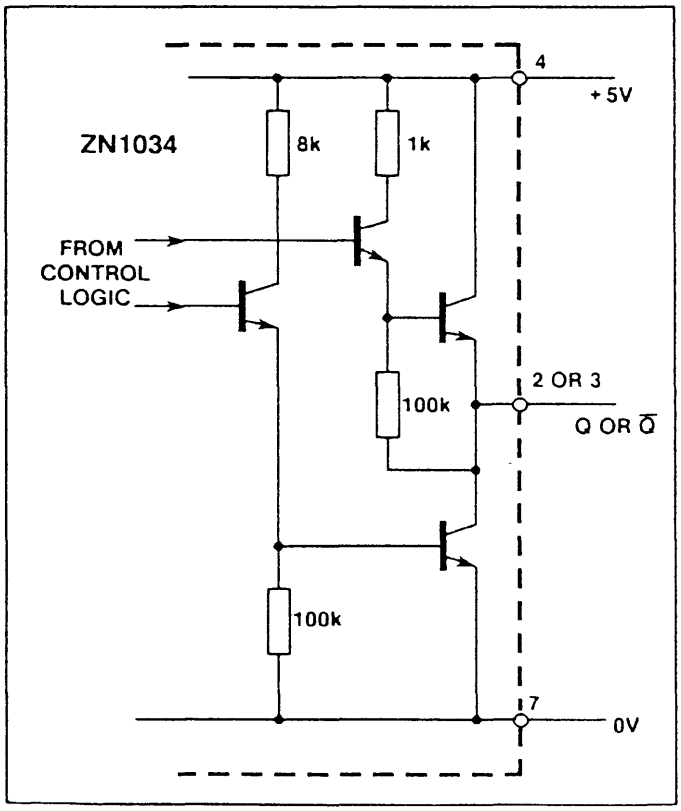
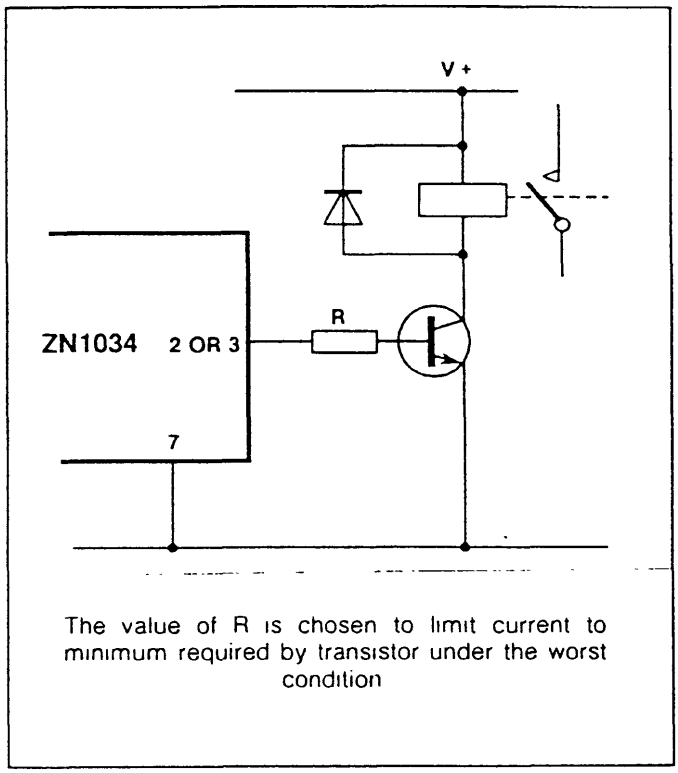


Fig 16

An external resistor is required to limit the drive current to the requirements of the load circuit and to the current capability of the +5V supply taking into account the needs of the ZN1034 itself (minimum 5mA externally regulated or 7mA internally regulated).

Load Circuits

Transistor Driven Relay (Fig.17)



The value of R is chosen to limit current to minimum required by transistor under the worst condition

Fig. 17

Thyristor Driven Relay (Fig.18)

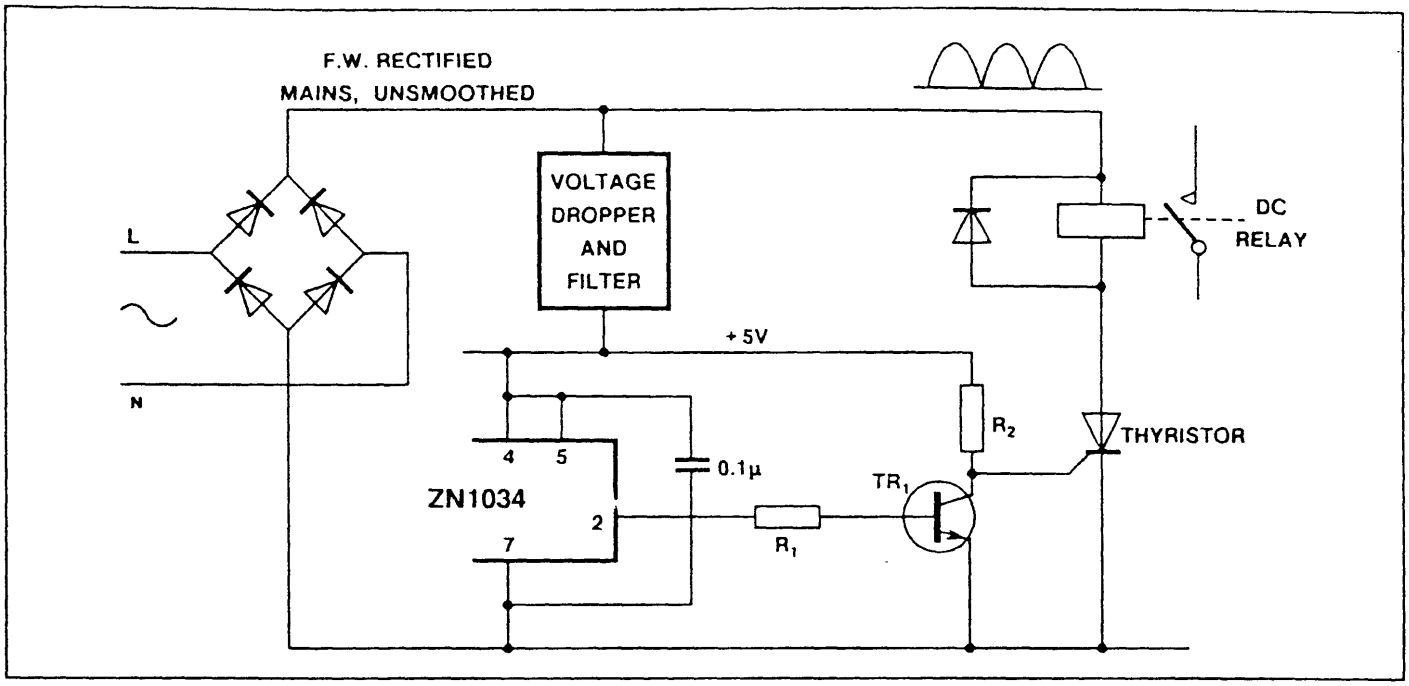


Fig.18

A thyristor gate may be driven via a limiting resistor directly from pin 2 for DELAY-TO-ON timers. Fig.18 illustrates a circuit for achieving DELAY-TO-OFF using a thyristor. R_2 can be as high as 10k for low gate current thyristors. The thyristor is chosen such that the reduction in gate-cathode impedance achieved with a saturated transistor is sufficient to increase the holding current to a value which ensures turn OFF and R_1 is chosen so that the transistor (T_{R1}) just reaches saturation

For 240V AC mains it may be necessary to use a 110V DC relay with a dropping resistor of equal resistance since 220V DC relays are not easily obtainable.

Triac AC Load Circuit Positive Firing (Fig.19)

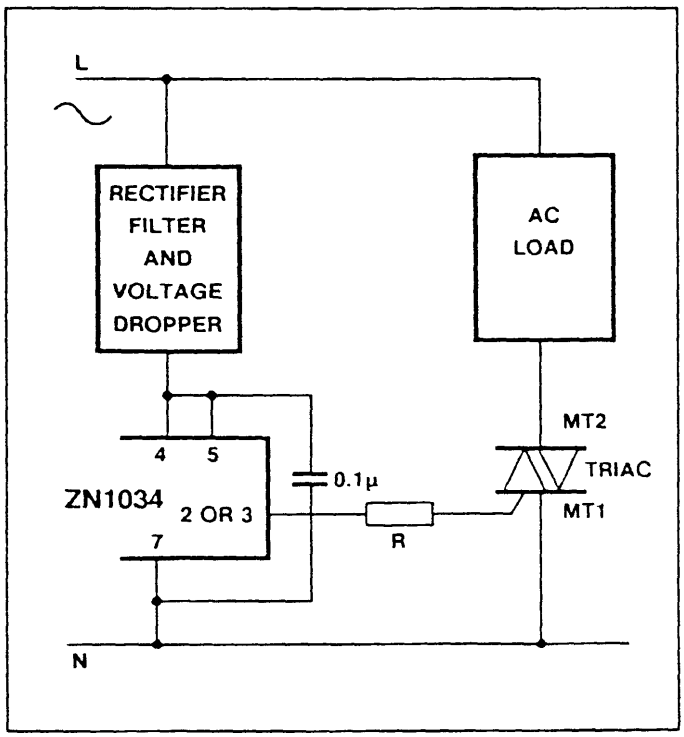


Fig.19

The value of R is chosen to limit the current to the minimum required by the triac for positive firing in both quadrants.

Triac AC Load Circuit Negative Firing (Fig.20)

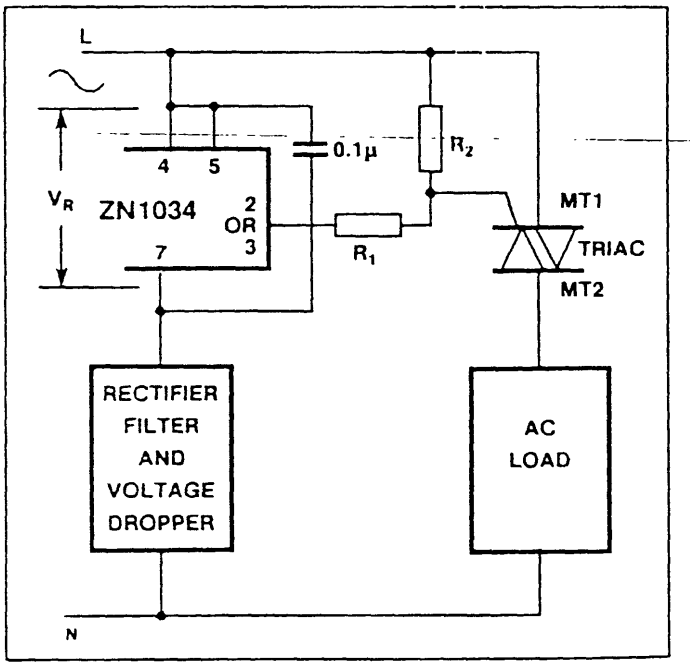
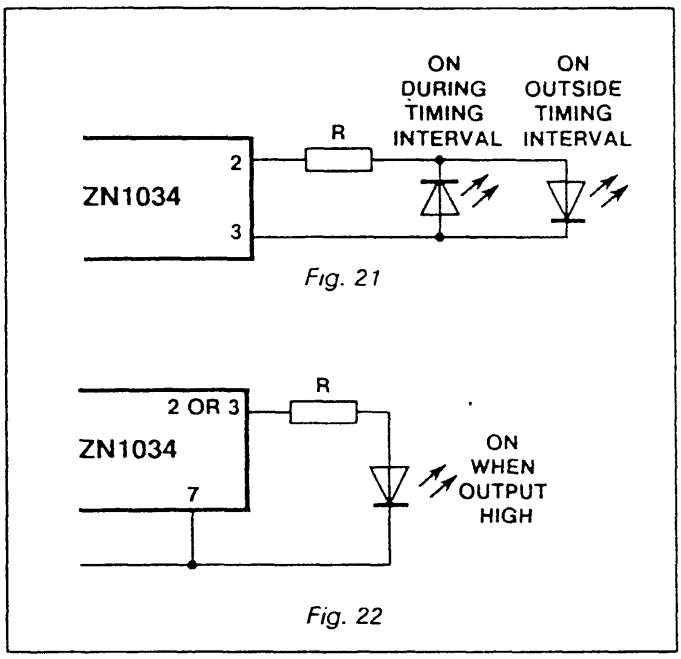


Fig.20

The value of R_2 is chosen to prevent any leakage currents biasing the triac gate ON during OFF periods. R_1 is chosen to limit the gate current to the maximum required by the triac for negative firing in both quadrants.

Triacs in general are easier to fire in the negative gate mode than the positive and in this configuration the ZN1034 output drive voltage is a maximum since the total output swing would be $V_{R\ Min} - V_{O(LO)\ Max}$ = 4.3V for a current of 25mA. Negative firing triac circuits therefore enable triacs of greater power to be driven directly from the ZN1034 outputs than would be the case for positive firing circuits.

Output State Indication (Figs.21 & 22)



The value of R is chosen to limit the current to the LED requirements. When mains supplies are used the extra power in the dropper resistor may make the use of neon indicators across the load preferable to LEDs

POWER SUPPLIES AND REFERENCES

Externally Regulated Supplies (Fig.23)

If a 5V ± 6% supply rail is available then the internal shunt regulator is not necessary and by leaving pin 5 unconnected the minimum current drain of 2mA required is avoided. The current available from the supply should not fall below a level of:

I_{CC} = (5mA + the output current from pins 3 or 2)

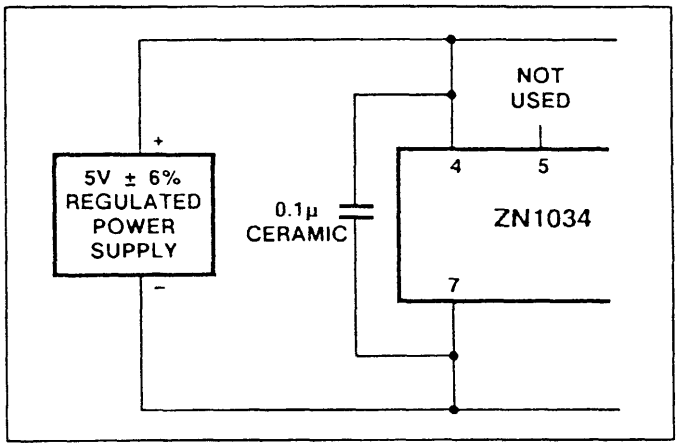


Fig. 23

N.B. The supply should be decoupled by 0.1µF capacitor connected as close as possible to pins 4 and 7.

Internally Regulated Supplies

DC Supplies Greater Than 5V (Fig.24)

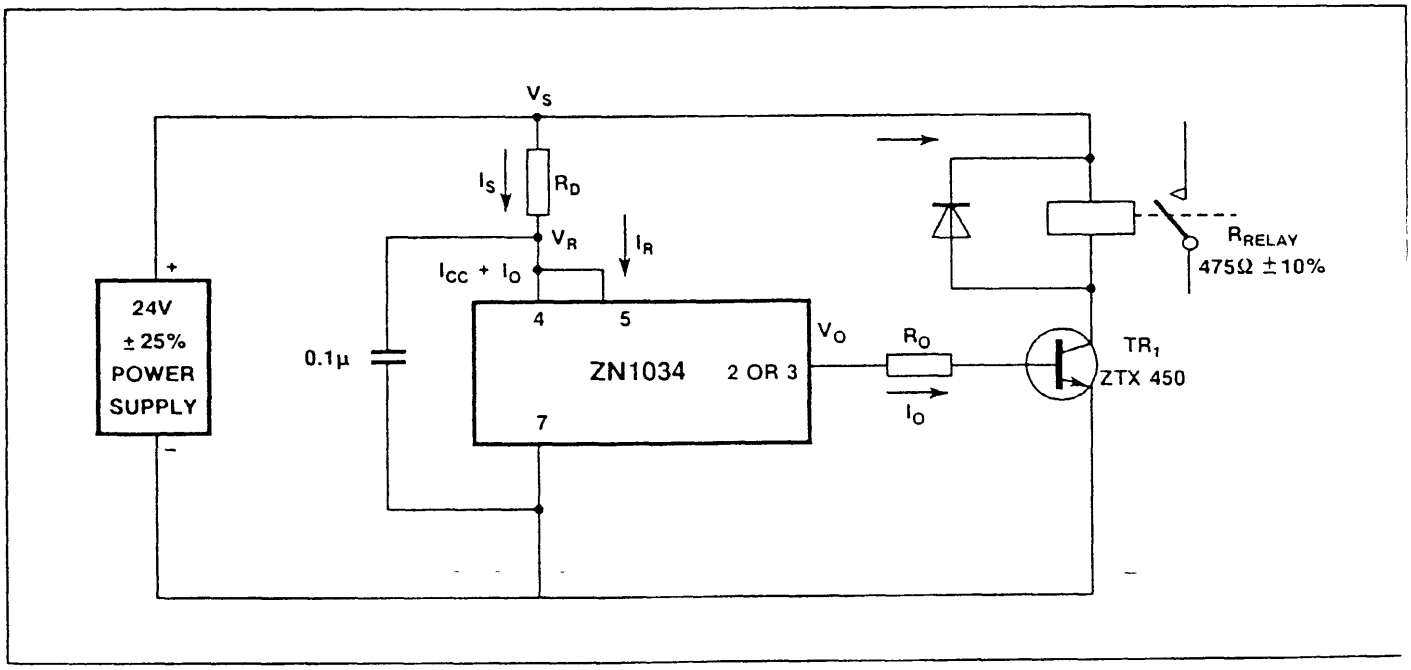


Fig.24

By connecting pin 5 to pin 4 an on-chip shunt regulator allows the use of unregulated DC supplies higher than 5V. To illustrate the use of the shunt regulator a supply circuit design for operation with a typical process equipment supply of +24V and ±25% is shown in Fig. 24

N.B. The supply decoupling capacitor also acts a stabilisation for the internal regulator and the connectio between pins 4 and 5 should therefore be as short a possible

The values of R_O and R_D used in the circuit of Fig.24 are calculated as follows. For R_O we need $I_{O(Min)}$, the minimum current required into the base of TR_1 for worst case conditions.

$$I_{O(Min)} = I_{B(Max)}$$

$$= \frac{1}{h_{FE(Min)}} \times \frac{24\ (+25\%)}{475\ (-10\%)}$$

$$= \frac{1}{50} \times \frac{30}{427}$$

$$\mathbf{I_{O(Min)} = 1.4mA}$$

Deriving $V_{O(Min)}$ for the output circuit (Fig 16)

$$V_{O(Min)} = V_{R(Min)} - 2 \times (\text{Internal } V_{BE})$$

$$= 4.7 - 1.4$$

$$\mathbf{V_{O(Min)} = 3.3V}$$

Hence $$R_O = \frac{3.3 - V_{BE}}{1.4}\ k\Omega \quad (V_{BE} = 0.6V)$$

$$= 1.9k$$

Choose $\mathbf{R_O}$ = **1.8kΩ** (Nearest lower preferred value)

To calculate R_D we need $V_{O(Max)}$ and $I_{S(Min)}$

As above

$$V_{O(Max)} = V_{R(Max)} - 2 \times (\text{Internal } V_{BE})$$

$$= 5.3 - 1.4V$$

$$\mathbf{V_{O(Max)} = 3.9V}$$

and with the value of R_O chosen the actual current is

$$I_{O(Max)} = \frac{3.9 - V_{BE}}{1.8} = 1.8mA$$

From which the minimum allowable supply current can be obtained

$$I_{S(Min)} = I_{CC(Max)} + I_{R(Min)} + I_{O(Max)}$$

$$= 5 + 1 + 1.8$$

$$\mathbf{I_{S(Min)} = 8.8mA}$$

Hence $$R_D = \frac{V_{S(Min)} - V_{R(Max)}}{I_{S(Min)}}$$

$$= \frac{18 - 5.3}{8.8}\ k\Omega$$

$$\mathbf{R_D = 1.5k\Omega}$$ (Nearest preferred value)

The power dissipated in the dropping resistor and the ZN1034 can be obtained also from

$$I_{S(Max)} = \frac{V_{S(Max)} - V_{R(Min)}}{1.5k\ (-5\%)}$$

$$= \frac{30 - 4.7}{1.425}\ mA$$

$$\mathbf{I_{SMax)} = 18mA}$$

Hence the ZN1034 dissipation = **90mW** max. and power dissipation by dropping resistor = **450mW** max.

The calculations assume ±2% tolerance resistors.

AC Mains Supplies (Fig.25)

A transformer may be used to drop the voltage from the mains and a rectified DC supply provided as discussed above.

However the on-chip shunt regulator makes the transformer unnecessary since the supply may be obtained directly from the mains or from any other source of AC or DC higher than 5V With a load such as the directly driven triac (Figs.19 and 20) a half wave rectifier is used since either the line or neutral has a connection common to the load circuit and the IC supply thus preventing the use of a bridge rectifier.

The calculation of the smoothing and voltage dropping components is described below.

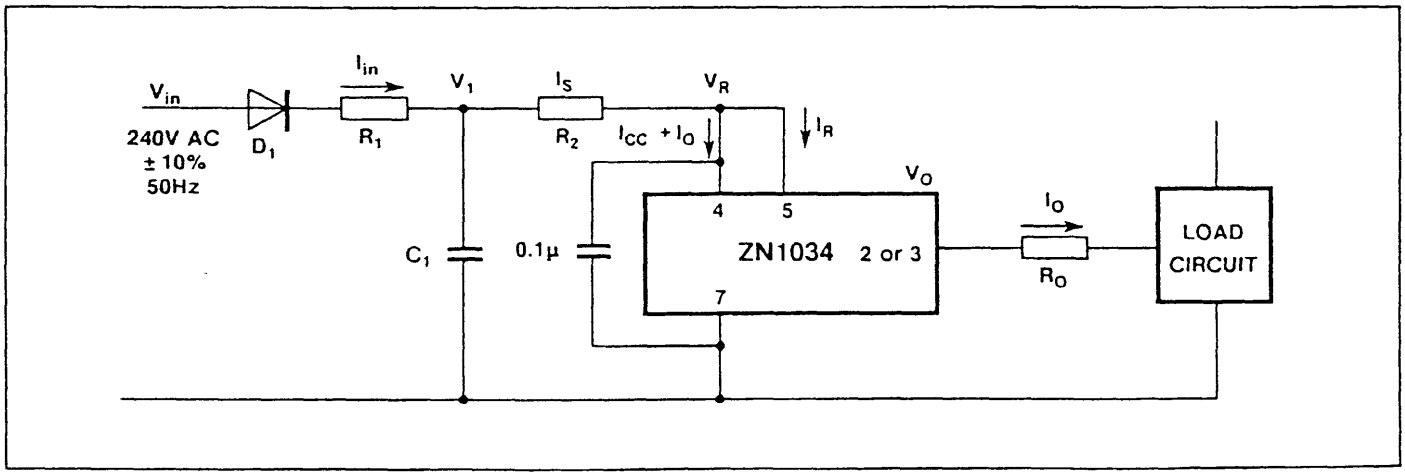


Fig. 25

The value of R_O and $I_{O(Max)}$ are calculated above and as an example a current $I_{O(Min)}$ of 10mA is assumed (the gate current for a 0.35A Triac, RS 202).

Therefore

$$V_{O(Min)} = 3.3V$$

$$R_O = \frac{3.3 - V_G}{10.10^{-3}} \ \Omega \ (V_G = 2V \text{ for RS 202})$$

$$\mathbf{R_O = 120\Omega} \quad \text{(Nearest lower preferred value)}$$

$$\mathbf{V_{O(Max)} = 3.9V}$$

Hence $$I_{O(Max)} = \frac{3.9 - V_G}{0.12} \ mA$$

$$\mathbf{I_{O(Max)} = 16mA}$$

And the minimum value of supply current for correct operation is therefore

$$I_{S(Min)} = I_{CC(Max)} + I_{R(Min)} + I_{O(Max)}$$

$$= 5 + 2 + 16$$

$$\mathbf{I_{S(Min)} = 23mA}$$

If we assume that C1 is a 25V working capacitor and that 3V peak to peak ripple is allowable then the highest value for $V_{1(Min)}$ will be

$$V_{1(Min)} = 25 \ (-20\%) - 3 \quad \text{(Allowing for } \pm 10\% \text{ variation in mains supply)}$$

$$\mathbf{V_{1(Min)} = 17V}$$

Therefore $$R_2 = \frac{17 - V_{R(Max)}}{23} \ k\Omega$$

$$\mathbf{R_2 = 510\Omega} \quad \text{(Nearest preferred value)}$$

The current I_{in} will flow for very nearly the full half cycle, 10ms in the case of 50Hz supplies, since V_1 is low compared to the peak mains voltage.

Now $$I_{in(avg)} = \frac{V_{in(pk)} - V_{1(avg)}}{\pi R_1}$$

and this current from the rectifier must be equal to the current into the timer circuit.

$$I_{in(avg)} = I_{S(avg)}$$

and the average value of this current is

$$I_{S(avg)} = \frac{V_{1(Min)} + V_{RIPPLE(avg)} + V_{R(Min)}}{R_2}$$

$$= \frac{17 + 1.5 + 4.7}{510}$$

$$= 27mA$$

Therefore $$R_1 = \frac{\sqrt{2} \times 240 \ (-10\%) - (17 + 1.5)}{\pi \times 27} \ k\Omega$$

$$= \mathbf{3.3k\Omega} \text{ (Nearest preferred value)}$$

For the required ripple of 3V pk-pk we can obtain

$$C_1 = \frac{I_{S(avg)} \times 10ms}{3}$$

$$C_1 = \frac{27 \times 10^{-5}}{3}$$

$$\mathbf{C_1 = 100\mu F} \quad \text{(Nearest higher preferred value)}$$

In order to calculate the maximum power dissipation in the dropping resistor we need to know $I_{in(avg)}$ for the upper limit of mains voltage.

Maximum value of

$$I_{in(avg)} = \frac{V_{in(pk)(Max)} - V_{1(Max)}}{\pi R_1}$$

$$= \frac{2 \times 240 \ (+10\%) - 20}{h \times 3.3 \times 10^3}$$

$$\mathbf{Max.\ I_{in(avg)} = 34mA}$$

and Max. dissipation in

$$R_1 = \frac{\pi^2}{4} \ I_{in}^2{}_{(avg)} \times R_1$$

$$\mathbf{P_{R1} = 9.4W}$$

When a DC load such as the thyristor relay driver of Fig.18 is required then a full wave bridge circuit can be used as shown in Fig.26.

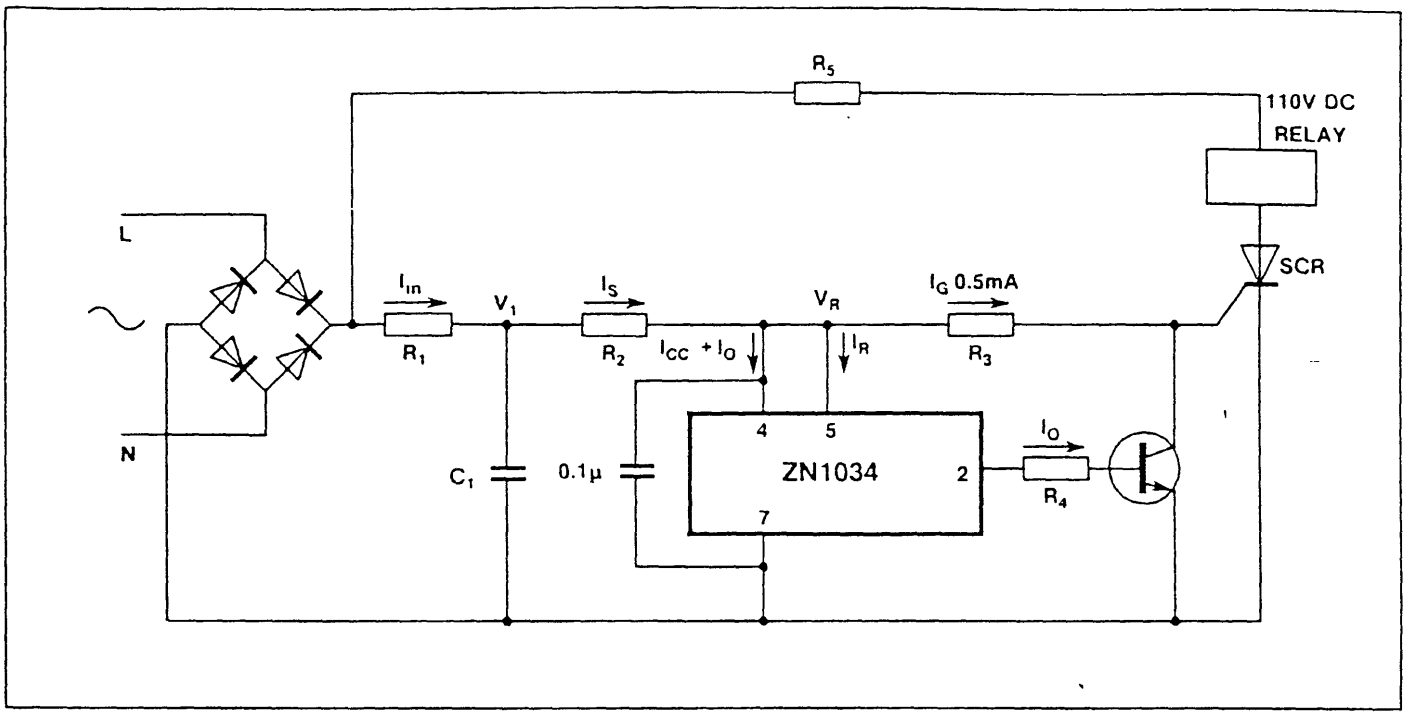


Fig. 26

The DELAY-TO-OFF timer circuit of Fig.18 has been taken as an example. A typical circuit might have the relay resistance equal to R_5 = 10k and for a 240V ± 10% mains supply the SCR could be a BRX49 which requires less than 0.5mA on gate current. To ensure gate turn-off a ZTX450 transistor with a base current of 0.5mA is sufficient with the above load.

Hence $I_{S(Min)} = I_{CC(Max)} + I_{R(Min)} + I_{O(Max)} + I_G$

$= 5 + 2 + 0.5 + 0.5$

$I_{SMin)} = \mathbf{8mA}$

Choosing C_1 to be 25V working and 3V peak to peak ripple as in the previous example. Then

$V_{1(Min)} = 25\ (-20\%) - 3$

$= \mathbf{17V}$

And $R_2 = \dfrac{17 - V_{R(Max)}}{8}$ kΩ

$= \mathbf{1.5k\Omega}$ (Nearest preferred value)

To find the required value of C_1 estimate the angle of conduction. Thus for a sine wave input conduction will change when the voltage on the smoothing capacitor is equal to the instantaneous value of the input voltage less the rectifier voltage drop.

So $V_1 + 1.2 = V_{in(pk)} \sin 0$

and for small values

$0 = \sin 0$

Hence $0 = \dfrac{V_1 + 1.2}{V_{in(pk)}}$

(assuming 1.2V drop across the bridge rectifier)

for the rising sine wave

$$\theta_r = \frac{V_{1(Min)} + 1.2}{V_{in(pk)}}$$

and for the falling sine wave

$$\theta_f = \frac{V_{1(Max)} + 1.2}{V_{in(pk)}}$$

$$\theta_{tot} = \frac{V_{1(Min)} + V_{1(Max)} + 2.4}{V_{in(pk)}}$$

$$= \frac{17 + 20 + 2.4}{305}$$ (Taking lowest mains input as worst case).

$= 0.13$ radian

The angle of non-conduction θ_{tot} = 8° and the capacitance will discharge by 3V in this period which in terms of time is

$$t = \frac{8}{180°} \times 10\text{ms}$$ (for 50Hz mains)

$= 0.44$ms

and since $C \simeq \dfrac{\Delta t}{\Delta V} \cdot I_{S(Max)}$.

where $I_{S(Max)} \simeq I_{S(Min)} + 20\%$.

$$= \frac{44 \times 10^{-5}}{3} \times 8 \times 10^{-3}\ (+20\%)$$

$= 1.4\mu$F

So we can choose a 2.2µF of 25V working or higher for C_1.

The mains dropping resistor can be simply obtained with sufficient accuracy by assuming 100% conduction. Thus

$$R_1 = \frac{2}{\pi} \times \frac{V_{in(pk)} - V_{1(Max)}}{I_{S(Min)}}$$

$$= \frac{2 \times (305 - 20)}{\pi \times 8 \times 10^{-3}}$$

(Lowest mains voltage gives worst case).

$$= 22k\Omega \text{ (Next lowest preferred value}$$

In order to calculate the power dissipated by the dropping resistor P_{R1} we need to know $I_{in(avg)}$ for the higher limit of the supply.

Maximum value of

$$I_{in(avg)} \simeq \left[\frac{2\,(V_{in(pk)(Max)} - V_{1(Max)})}{\pi R_1}\right]$$

$$= \frac{2}{\pi} \quad \frac{2 \times 240\ (+10\%) - 20}{22 \times 10^{-3}}$$

$$I_{in(avg)} = 10mA$$

Hence

$$P_{R1} = \frac{\pi^2}{8} \times 10^{-4} \times 22 \times 10^3$$

$$P_{R1} = 2.7W$$

The calculations have been performed using the 235V ± 10% 50Hz mains figures Similar calculations may be made for 110V 60Hz or whatever supplies are available.

Reference supply

The 2.6V reference on pin 14 may be used for an external reference other than for the timing components.

INTERFERENCE SUPPRESSION

Two types of interference, mains borne and electromagnetically radiated interference, can affect the operation of the timing circuit. In environments where such noise is encountered steps should be taken to reduce its effect on the timing circuit and the following notes should enable the circuit designer to avoid interference problems. The points discussed are illustrated by referring to a mains delay-to-on, plug-in module timer design, illustrated in Figs.27, 28, 29 and 30.

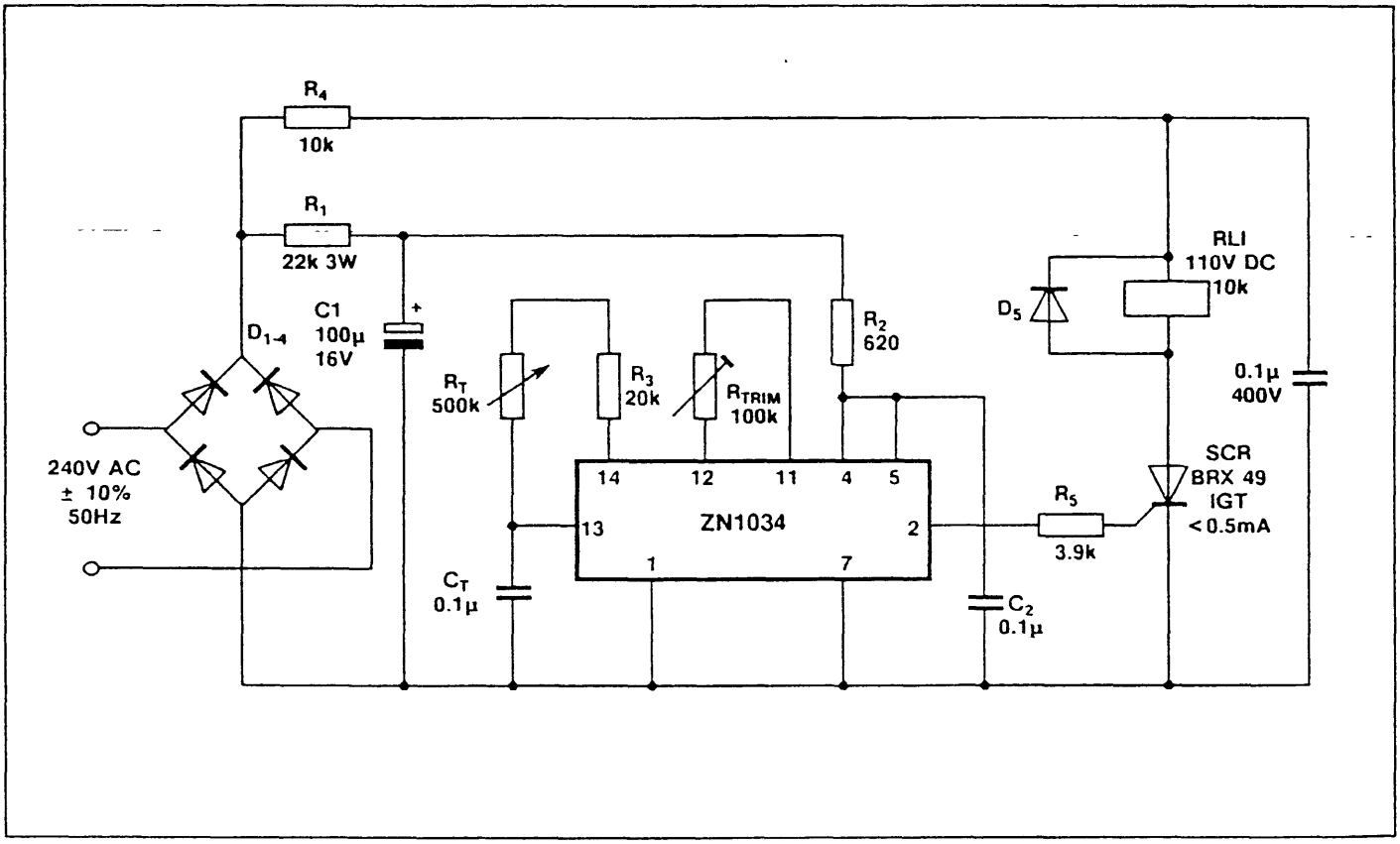


Fig. 27

Mains Borne Interference

If the supply is reduced below (typically) 3.6V at any time, even for less than a microsecond, the the ZN1034 counter section will be reset and restoration of the normal supply will initiate a new timing period or terminate the period depending on the initiation mode used. The effects of pulses on the supply are described above under 'Timing Initiation and Reset'.

Positive spikes are effective only when they produce a negative overshoot large enough to cause reset.

Negative spikes can be reduced by using a full diode bridge circuit, as in Fig.27 which rectifies the spikes as well as the AC supply, or a half bridge where an AC load is being driven and the timer ground cannot be separated from neutral. The dropping resistor R_1, with C_1, forms a low pass filter for mains smoothing and additional filtration is provided by R_2 and C_2. These filters will also attenuate noise spikes. The shunt regulator in conjunction with the dropping resistors R_1 and R_2 provides considerable spike attenuation as well as DC regulation. The circuit of Fig.27 for example, has an attenuation of supply spikes of 15000:1 due to the regulator alone. When a 5V supply designed for TTL, or similar requirements is available and the shunt regulator is not connected, protection against interference is not usually necessary since the supply itself should be capable of suppressing mains borne interference.

If a transformer is used to isolate the timer from the mains then the voltage drop can be divided between the transformer and the series resistor. The greater the series resistance then the greater the attenuation of noise by the shunt regulator and the smoothing capacitor. A transformer drop to 24V DC is a useful compromise allowing the use of 24V relays. The transformer itself will attenuate high frequency spikes.

Electromagnetically Induced Noise

The ZN1034 oscillator frequency is determined by the time taken to charge C_T via R_T from about 1.6 to 2.2V on pin 13. A single interference pulse of 0.1V on this pin could cause an error on a single time constant of 20% but since the timing period of a ZN1034 timer is made up of 4095 RC charging times then a large number of interference pulses in a timing period would be required to cause such a timing error. Where such inteference exists, and bearing in mind that for a constant rate of interference pulses the effect becomes greater for increasing length of time period, steps should be taken to screen pin 13 from electromagnetically induced noise. Since the oscillator is required to operate at

$$\frac{4095}{20 \times 10^{-3}} \text{ Hz},$$

i.e. 200kHz, pin 13 is sensitive to radiated high frequency interference. Mains Borne pulses can be equally troublesome if steps are not taken to isolate pin 13 from such interference. The method used in the design example of Fig.27 is effective against both EMI and Mains Borne noise. A ground plane is produced by leaving a large area of copper on the component side of a double sided PCB with clearance holes for the component connections. The ground pin (7) is connected to the ground plane and the ground side of components such as C_T and the decoupling capacitors are also connected directly to the ground plane. In this way the connections have a low impedance to pin 7 and the possibility of coupling interference pulses from the load or decoupling components into the oscillator circuit via common earth leads is reduced considerably. At the same time the printed circuit connections are screened from EMI.

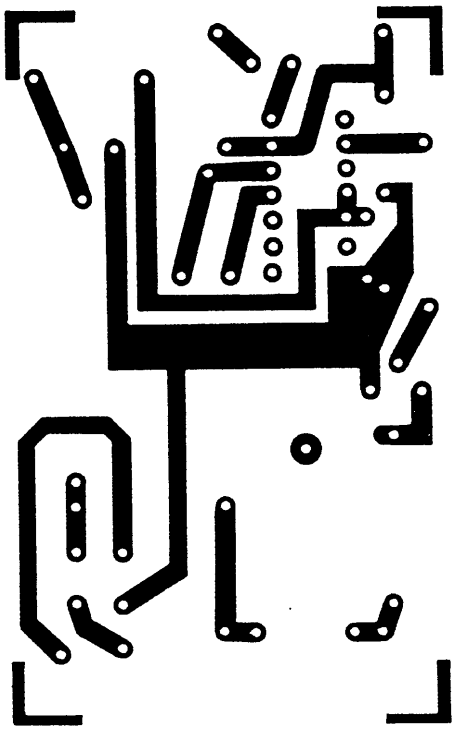


Fig.28 PCB for Fig.27 - track side

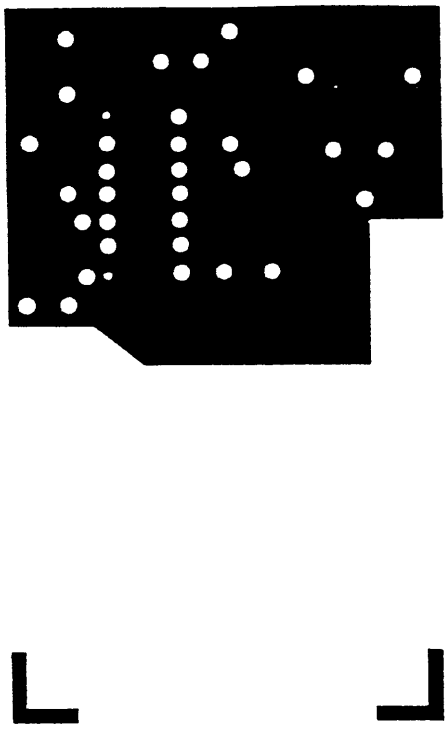


Fig.29 PCB for Fig.27 - ground plane

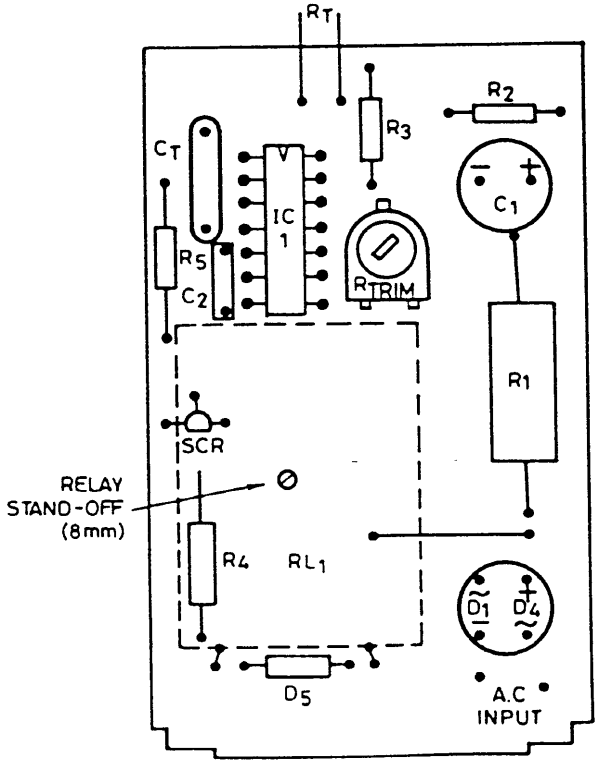


Fig.30 PCB component layout for Fig.27

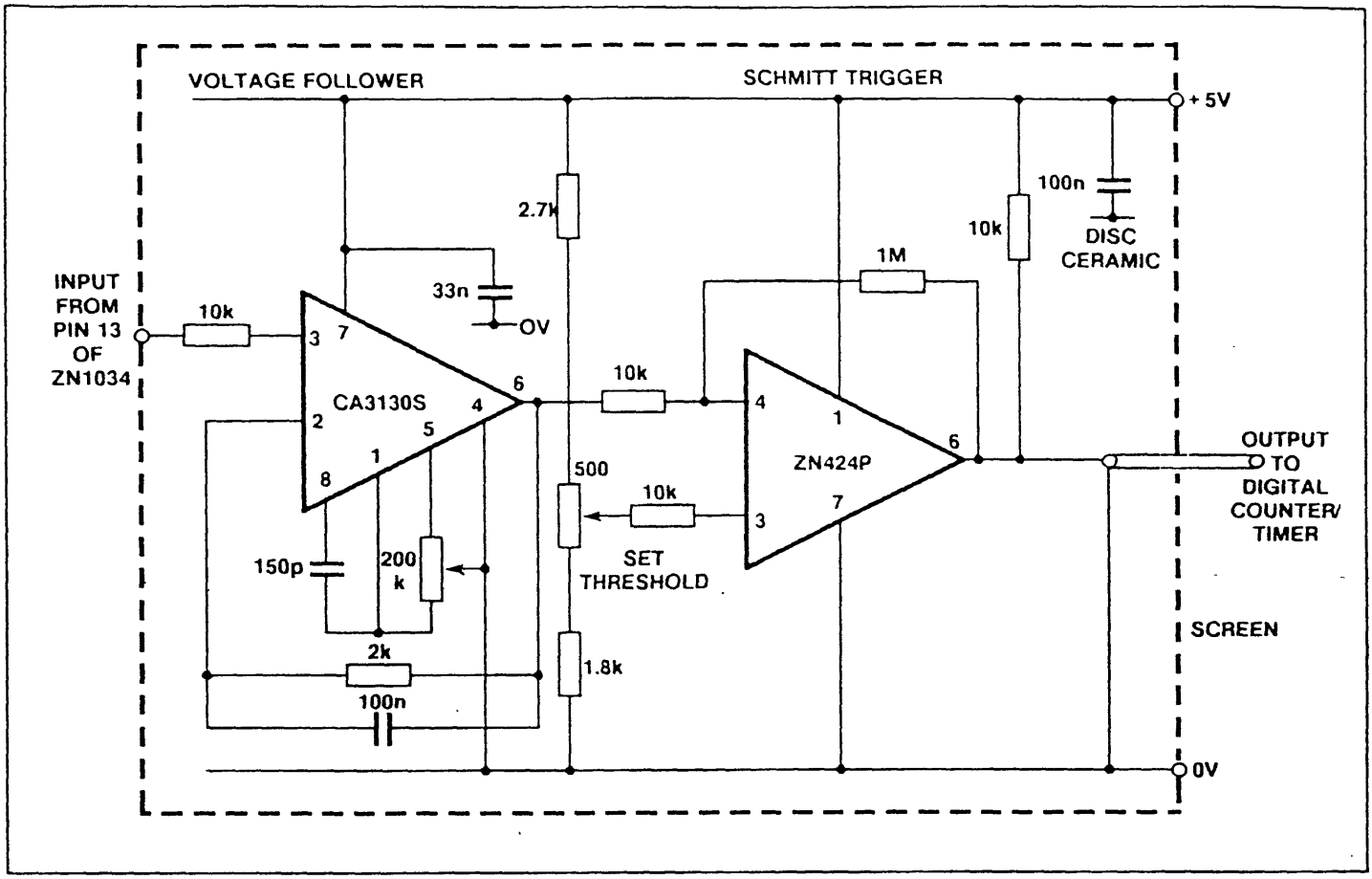

VOLTAGE FOLLOWER
SCHMITT TRIGGER
+5V
2.7k
100n
10k
DISC
CERAMIC
1M
INPUT
FROM
PIN 13
OF
ZN1034
10k
33n
0V
CA3130S
10k
ZN424P
OUTPUT
TO
DIGITAL
COUNTER/
TIMER
500
10k
150p
200
k
SET
THRESHOLD
2k
1.8k
100n
SCREEN
0V

Fig. 32

An external screen such as a metal case can be effective against radiated interference but it does not have the advantage of a ground plane with regard to the reduction of common earth lead interference.

Any leads connected to pin 13 are susceptible to interference pick-up and should be screened. A remote variable timing resistor can be connected to the PCB either by twin screened lead with the screen to ground or single screened with the screen connected to pin 14. It will be noticed that the fixed part of the timing resistance is connected very close to pin 13 to help decouple the connecting leads to the variable resistor.

When the ZN1034 oscillator frequency is near to that of the mains supply, or to low harmonics, care should be taken in the layout of the circuitry and in the position of components such as mains transformers to obviate this effect. Stray coupling of mains frequencies can have the effect of locking the oscillator to that frequency and producing a band over which variation in timing components will not cause a corresponding variation in timing period. The periods most susceptible to such interference are 82 and 41 seconds for 50Hz mains or 68 and 34 seconds for 60Hz mains.

TIMER CALIBRATION

Direct Measurement

Timer circuits may be calibrated directly by measuring the time period between changes of state on the output pins 2 or 3. This method should be used where accuracies of better than 0.2% are required.

Oscillator Period Measurement

The measurement of oscillator period is a much quicker method of calibration but it involves measurements at a high impedance point in the circuit where the loading due to the measuring instrument could effect the result. The following notes should assist in calibration by oscillator period measurement.

(a) A passive high impedance probe may be used to connect an oscillator or a digital frequency meter to pin 13 and if the probe resistance is greater than 100 R_T and the capacitance less than $C_t/100$ then an accuracy better than 2% should be obtainable. For lower accuracy these requirements may be relaxed proportionally. The period of the oscillator sawtooth waveform is measured and multiplied by 4095 to obtain the time period.

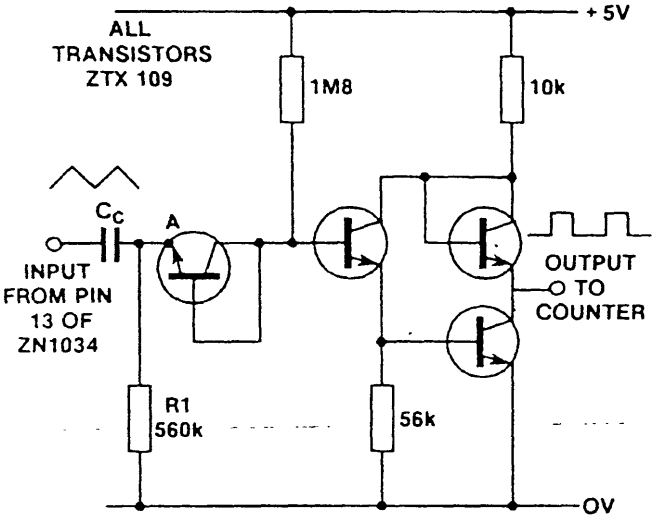
(b) A capacitively coupled probe illustrated in Fig. 31 enables calibration accuracies of better than 0.2% to be obtained.

The maximum value of coupling capacitance for this accuracy is tabulated against timing capacitance above.

(c) It may be advantageous to build-in the probe inp capacitor and resistor to the timer and have poi 'A' as the input to the external buffer.

An active voltage follower probe such as th illustrated in Fig. 32 may be used instead of th passive probe in (a) above.

(d) Connecting extra circuitry to pin 13 increases th possibility of incorrect operation due to interferenc and the precautions suggested under 'Interferenc Suppression' above should be borne in mind whe devising oscillator period calibration systems.



C_T (µF)	C_C (nF)
0.01	0.033
0.1	0.33
1.0	3.3
10.0	33.0
100.0	330.0

Fig. 31