

TL/G/10035-42

DESCRIPTION

Process 93 is a monolithic dual JFET with a diode isolated substrate. It is intended for wide band, low noise, single ended video amplifier input stages, and high slew rate op amps. Monolithic structure eliminates thermal transient errors, and provides freedom to pick operating current and voltage.

Electrical Characteristics (T_A = 25°C)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
BV _{GSS}	Gate-Source Breakdown Voltage	V _{DS} = 0V, I _G = -1 μA	-25	-30		V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = 10V, V _{GS} = 0V, Pulsed	3.0	18	40	mA
g _{fs}	Forward Transconductance	V _{DS} = 10V, V _{GS} = 0V, Pulsed		8.0		mmhos
g _{fs}	Forward Transconductance	V _{DG} = 10V, I _D = 5 mA	5.0	6.0	10	mmhos
g _{os}	Output Conductance	V _{DG} = 10V, I _D = 5 mA		50	100	μmhos
V _{GS(OFF)}	Pinch Off Voltage	V _{DS} = 10V, I _D = 1 nA	-1.5	-3.5	-6.0	V
r _{DS(ON)}	ON Resistance	V _{DS} = 100 mV, V _{GS} = 0V		100		Ω
I _G	Gate Current	V _{DG} = 10V, I _D = 5 mA		10	100	pA
e _n	Noise Voltage	V _{DG} = 10V, I _D = 5 mA, f = 100 Hz		9.0	30	nV/√Hz
V _{GS1} - V _{GS2}	Differential Match	V _{DG} = 10V, I _D = 5 mA		9.0	30	mV
ΔV _{GS1} - V _{GS2}	Differential Match Drift	V _{DG} = 10V, I _D = 5 mA		15	40	μV/°C
CMRR	Common-Mode Rejection	V _{DG} = 10V, I _D = 5 mA		90		dB
C _{rs}	Feedback Capacitance	V _{DG} = 10V, I _D = 5 mA, f = 1 MHz		1.0	1.2	pF
C _{is}	Input Capacitance	V _{DG} = 10V, I _D = 5 mA, f = 1 MHz		4.2	5.0	pF

This process is available in the following device types. *Denotes preferred parts.

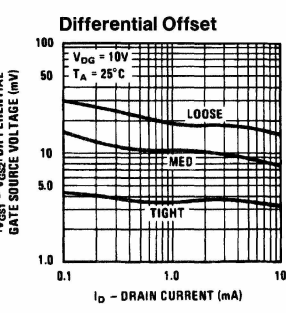
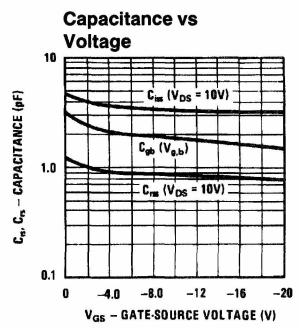
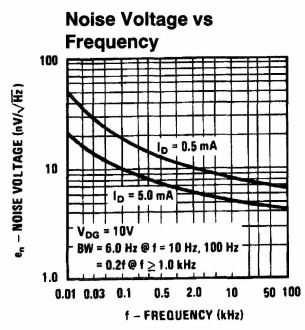
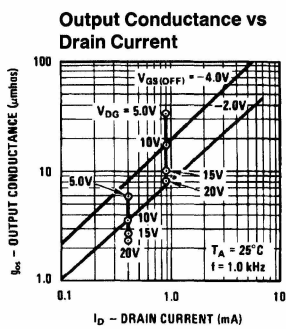
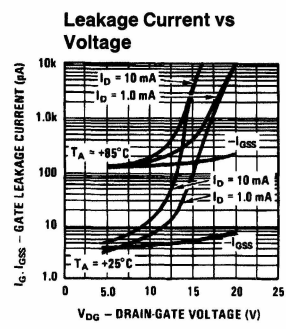
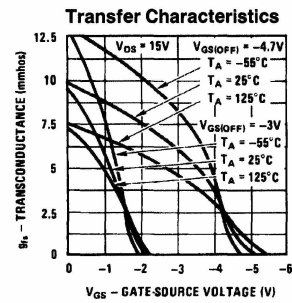
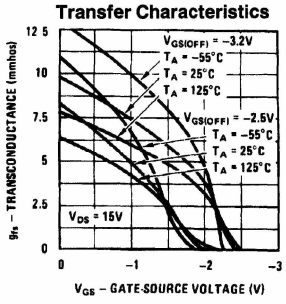
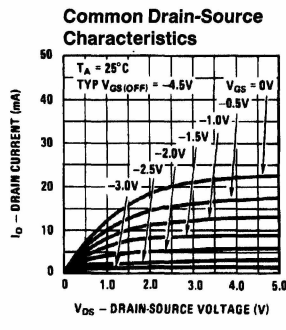
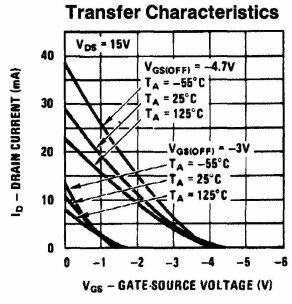
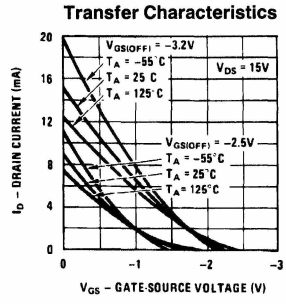
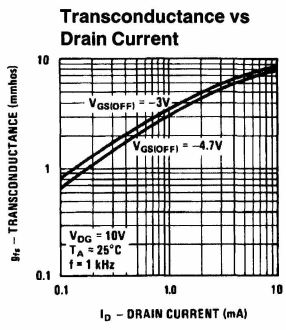
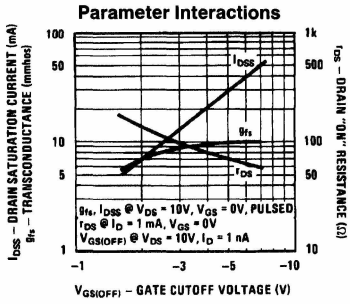
TO-78 (NS Package 24)

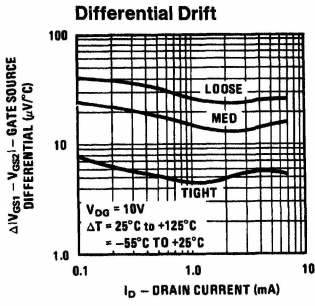
*2N5911
*2N5912
U257

TO-71 (NS Package 12)

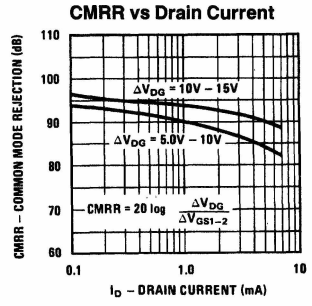
NF5911
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U440
U441

Note: SO-8 to be announced.





TL/G/10035-44



TL/G/10035-45