

TL/G/10035-53

DESCRIPTION

Process 96 is a monolithic dual JFET with a diode isolated substrate. It is intended for wide band, low noise, single ended video amplifier input stages. Also ideal for matched voltage variable resistor applications over 60 dB tracking range.

Electrical Characteristics (T_A = 25°C)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
BV _{GSS}	Gate-Source Breakdown Voltage	V _{DS} = 0V, I _G = -1 μA	-40	-55		V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = 15V, V _{GS} = 0V	5.0	15	30	mA
g _{fs}	Forward Transconductance	V _{DS} = 15V, V _{GS} = 0V	9.0	18	30	mmhos
g _{fs}	Forward Transconductance	V _{DG} = 15V, I _D = 2 mA	7.5	9.0		mmhos
g _{os}	Output Conductance	V _{DG} = 15V, I _D = 2 mA		15	45	μmhos
V _{GS(OFF)}	Pinch Off Voltage	V _{DS} = 15V, I _D = 1 nA	-0.5	-1.8	-3.0	V
r _{DS(ON)}	ON Resistance	V _{DS} = 100 mV, V _{GS} = 0V	35	70	120	Ω
I _{GSS}	Gate Current	V _{GS} = -20V, V _{DS} = 0V		-8.0	-100	pA
I _G	Gate Current	V _{DG} = 15V, I _D = 2 mA		15	200	pA
e _n	Noise Voltage	V _{DG} = 15V, I _D = 2 mA, f = 100 Hz		4.5	10	nV/√Hz
C _{rs}	Feedback Capacitance	V _{DG} = 15V, I _D = 2 mA, f = 1 MHz		2.5	3.0	pF
C _{is}	Input Capacitance	V _{DG} = 15V, I _D = 2 mA, f = 1 MHz		10	12	pF
V _{GS1} - V _{GS2}	Differential Voltage	V _{DG} = 15V, I _D = 2 mA		8.0	25	mV
ΔV _{GS1} - V _{GS2}	Differential Voltage Drift	V _{DG} = 15V, I _D = 2 mA		9.0	50	μV/°C
CMRR	Common-Mode Rejection	V _{DG} = 15V, I _D = 2 mA	76	95		dB

This process is available in the following device types. *Denotes preferred parts.

TO-71 (NS Package 12)

*2N5564

*2N5565

*2N5566

8-Pin DIP (NS Package 67)

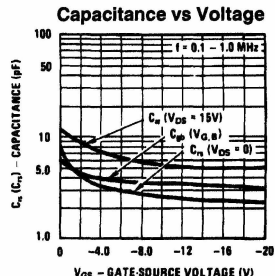
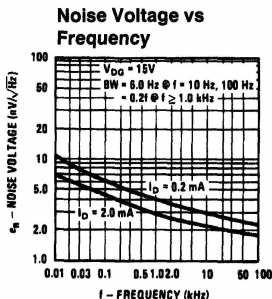
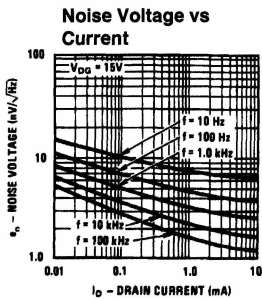
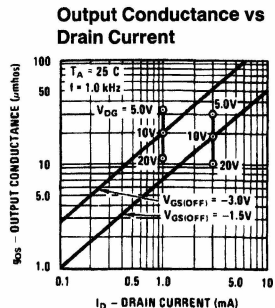
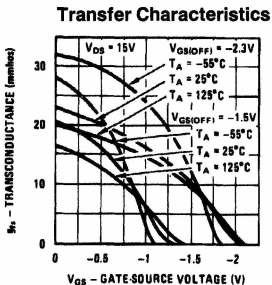
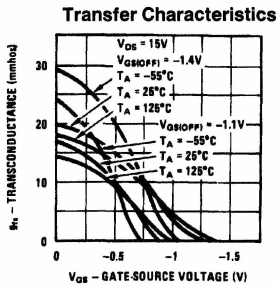
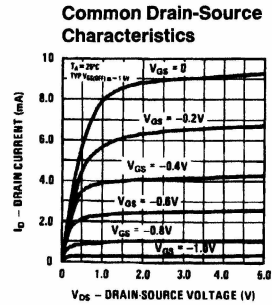
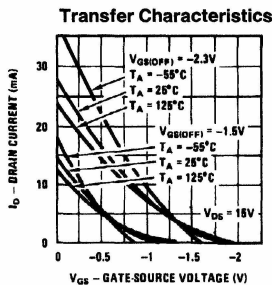
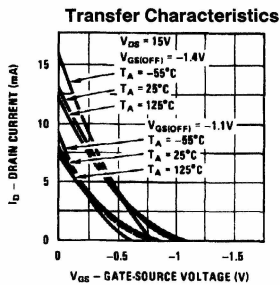
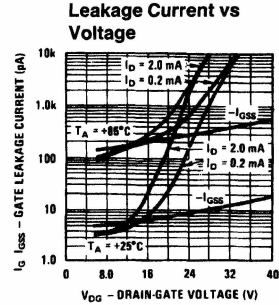
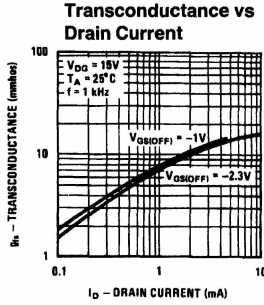
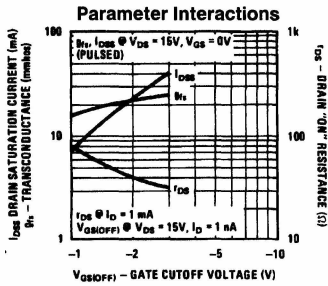
*NPD5564

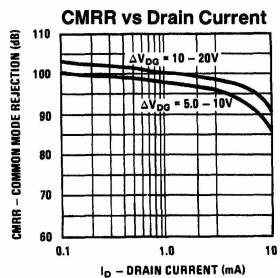
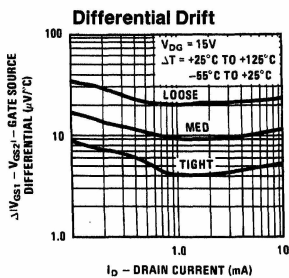
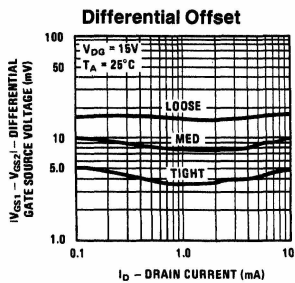
*NPD5565

*NPD5566

Pin	67
1	S1
2	D1
3	NC
4	G1
5	S2
6	D2
7	NC
8	G2

Note: SO-8 to be announced.





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