
**DESCRIPTION**

These dice are n-channel, enhancement mode, power MOSFETs designed especially for high power, high speed applications, such as power supplies, AC and DC motor control and high energy pulse circuits.

This process is available in the following device types:

TO-220 (Case 37)

FMP18N05

FMP20N05

FMP18N06

FMP20N06

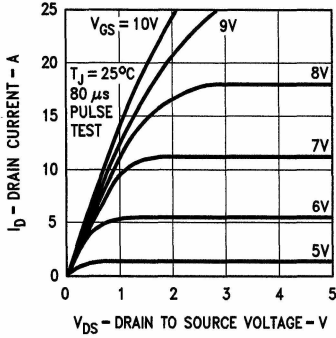
**Electrical Characteristics**  $T_C = 25^\circ\text{C}$  (unless otherwise noted)

| Symbol       | Parameter                        | Test Conditions  | Min | Max   | Units         |
|--------------|----------------------------------|--|-----|-------|---------------|
| $V_{DS}$     | Drain to Source Voltage (Note 1) | $I_D = 250 \mu\text{A}; V_{GS} = 0\text{V}$  | 50  |       | V             |
| $I_{DSS}$    | Zero Gate Voltage Drain          | $V_{DS} = \text{Rated Voltage}$<br>$V_{GS} = 0\text{V}$                              |     | 250   | $\mu\text{A}$ |
| $I_{GSS}$    | Gate Leakage Current             | $V_{DS} = \pm 20\text{V}; V_{GS} = 0\text{V}$  |     | 100   | nA            |
| $V_{GS(TH)}$ | Gate Threshold Voltage           | $I_D = 250 \mu\text{A}; V_{DS} = V_{GS}$   | 2.0 | 4.0   | V             |
| $R_{DS(ON)}$ | Static On-Resistance (Note 2)    | $V_{GS} = 10\text{V}; I_D = 10\text{A}$  |     | 0.085 | $\Omega$      |
| gFS          | Forward Transconductance         | $V_{DS} = 10\text{V}; I_D = 10\text{A}$  | 5   |       | Siemens       |
| $C_{iss}$    | Input Capacitance                | $V_{DS} = 25\text{V}; V_{GS} = 0\text{V}$<br>$f = 1 \text{ MHz}$                     |     | 850   | pF            |
| $C_{oss}$    | Output Capacitance               |  |     | 400   | pF            |
| $C_{rss}$    | Reverse Transfer                 |  |     | 150   | pF            |
| $t_{d(on)}$  | Turn-On Delay Time               | $V_{DD} = 40\text{V}; I_D = 10\text{A}$<br>$V_{GS} = 10\text{V}; R_{GEN} = 50\Omega$ |     | 50    | ns            |
| $t_r$        | Rise Time                        | $R_{GS} = 50\Omega$  |     | 90    | ns            |
| $t_{d(off)}$ | Turn-Off Delay Time              |  |     | 60    | ns            |
| $t_f$        | Fall Time                        |  |     | 75    | ns            |
| $Q_g$        | Total Gate Charge                | $V_{GS} = 10\text{V}; I_D = 25\text{A}$<br>$V_{DD} = 40\text{V}$                     |     | 20    | nC            |

Note 1:  $T_J = +25^\circ\text{C}$  to  $+150^\circ\text{C}$ .

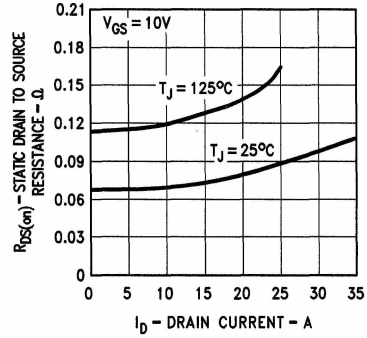
Note 2: Pulse Test: Pulse Width  $\leq 80 \mu\text{s}$ , Duty Cycle  $\leq 1\%$ .

Typical Performance Characteristics



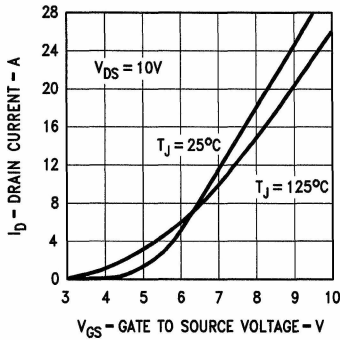
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FIGURE 1. Output Characteristics



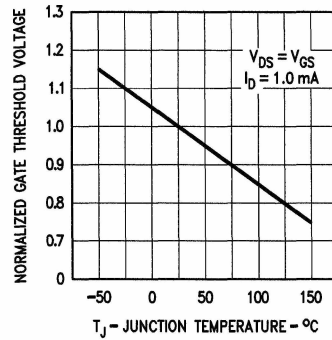
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FIGURE 2. Static Drain to Source Resistance vs Drain Current



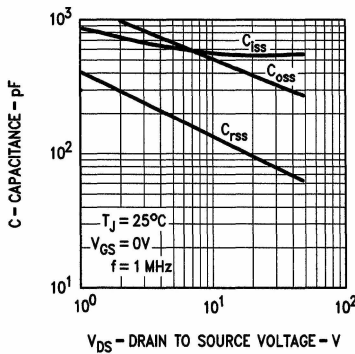
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FIGURE 3. Transfer Characteristics



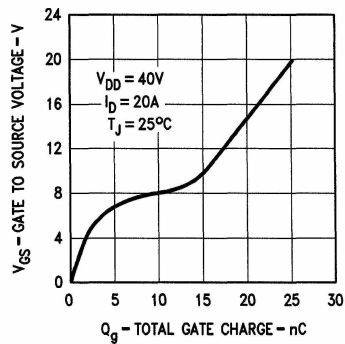
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FIGURE 4. Temperature Variation of Gate to Source Threshold Voltage



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FIGURE 5. Capacitance vs Drain to Source Voltage

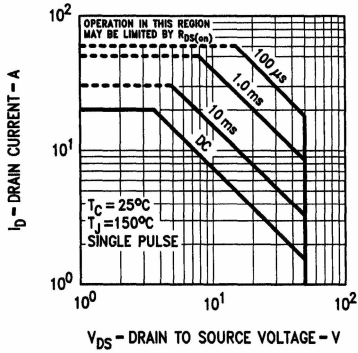


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FIGURE 6. Gate to Source Voltage vs Total Gate Charge

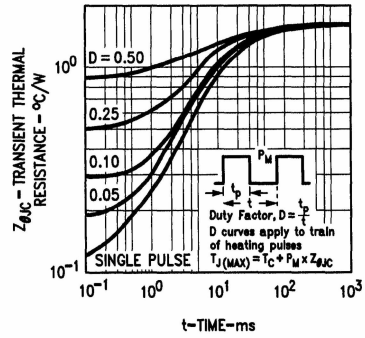
# Process B1

## Typical Performance Characteristics (Continued)



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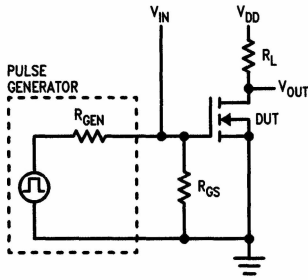
FIGURE 7. Forward Biased Safe Operating Area



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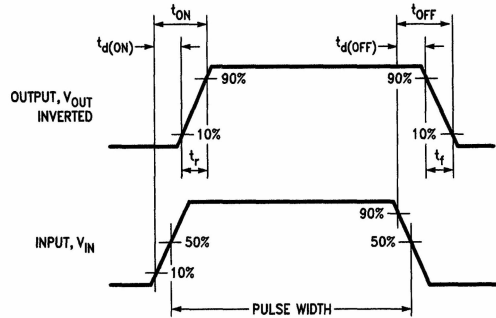
FIGURE 8. Transient Thermal Resistance vs Time

## Typical Electrical Characteristics



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FIGURE 9. Switching Test Circuit



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FIGURE 10. Switching Waveforms