

## 2N6504 Series

# Silicon Controlled Rectifiers

## Reverse Blocking Thyristors

Designed primarily for half-wave ac control applications, such as motor controls, heating controls and power supply crowbar circuits.

- Glass Passivated Junctions with Center Gate Fire for Greater Parameter Uniformity and Stability
- Small, Rugged, Thermowatt Constructed for Low Thermal Resistance, High Heat Dissipation and Durability
- Blocking Voltage to 800 Volts
- 300 A Surge Current Capability
- Device Marking: Logo, Device Type, e.g., 2N6504, Date Code

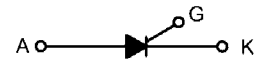
### MAXIMUM RATINGS ( $T_J = 25^\circ\text{C}$ unless otherwise noted)

Rating	Symbol	Value	Unit
*Peak Repetitive Off-State Voltage (Note 1.) (Gate Open, Sine Wave 50 to 60 Hz, $T_J = 25$ to $125^\circ\text{C}$ )	$V_{DRM}$ , $V_{RRM}$	50 100 400 600 800	Volts
On-State RMS Current ( $180^\circ$ Conduction Angles; $T_C = 85^\circ\text{C}$ )	$I_{T(RMS)}$	25	A
Average On-State Current ( $180^\circ$ Conduction Angles; $T_C = 85^\circ\text{C}$ )	$I_{T(AV)}$	16	A
Peak Non-repetitive Surge Current (1/2 Cycle, Sine Wave 60 Hz, $T_J = 100^\circ\text{C}$ )	$I_{TSM}$	250	A
Forward Peak Gate Power (Pulse Width $\leq 1.0 \mu\text{s}$ , $T_C = 85^\circ\text{C}$ )	$P_{GM}$	20	Watts
Forward Average Gate Power ( $t = 8.3 \text{ ms}$ , $T_C = 85^\circ\text{C}$ )	$P_{G(AV)}$	0.5	Watts
Forward Peak Gate Current (Pulse Width $\leq 1.0 \mu\text{s}$ , $T_C = 85^\circ\text{C}$ )	$I_{GM}$	2.0	A
Operating Junction Temperature Range	$T_J$	-40 to +125	$^\circ\text{C}$
Storage Temperature Range	$T_{stg}$	-40 to +150	$^\circ\text{C}$

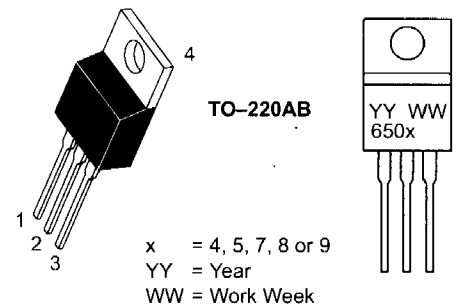
\*Indicates JEDEC Registered Data

1.  $V_{DRM}$  and  $V_{RRM}$  for all types can be applied on a continuous basis. Ratings apply for zero or negative gate voltage; however, positive gate voltage shall not be applied concurrent with negative potential on the anode. Blocking voltages shall not be tested with a constant current source such that the voltage ratings of the devices are exceeded.

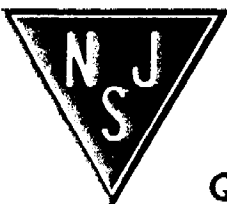
SCRs  
25 AMPERES RMS  
50 thru 800 VOLTS



### MARKING DIAGRAM



PIN ASSIGNMENT	
1	Cathode
2	Anode
3	Gate
4	Anode



NJ Semi-Condutors reserves the right to change test conditions, parameter limits and package dimensions without notice. Information furnished by NJ Semi-Condutors is believed to be both accurate and reliable at the time of going to press. However, NJ Semi-Condutors assumes no responsibility for any errors or omissions discovered in its use. NJ Semi-Condutors encourages customers to verify that datasheets are current before placing orders.

**\*THERMAL CHARACTERISTICS**

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.5	$^{\circ}C/W$
Maximum Lead Temperature for Soldering Purposes 1/8" from Case for 10 Seconds	$T_L$	260	$^{\circ}C$

**ELECTRICAL CHARACTERISTICS** ( $T_C = 25^{\circ}C$  unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
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**OFF CHARACTERISTICS**

*Peak Repetitive Forward or Reverse Blocking Current ( $V_{AK} = \text{Rated } V_{DRM} \text{ or } V_{RRM}$ , Gate Open)	$I_{DRM}, I_{RRM}$	$T_J = 25^{\circ}C$	-	-	10	$\mu A$
		$T_J = 125^{\circ}C$	-	-	2.0	mA

**ON CHARACTERISTICS**

*Forward On-State Voltage (Note 2.) ( $I_{TM} = 50 A$ )	$V_{TM}$	-	-	1.8	Volts
*Gate Trigger Current (Continuous dc) ( $V_{AK} = 12 V_{dc}$ , $R_L = 100 \text{ Ohms}$ )	$I_{GT}$	-	9.0	30	mA
		-	-	75	
*Gate Trigger Voltage (Continuous dc) ( $V_{AK} = 12 V_{dc}$ , $R_L = 100 \text{ Ohms}$ , $T_C = -40^{\circ}C$ )	$V_{GT}$	-	1.0	1.5	Volts
Gate Non-Trigger Voltage ( $V_{AK} = 12 V_{dc}$ , $R_L = 100 \text{ Ohms}$ , $T_J = 125^{\circ}C$ )	$V_{GD}$	0.2	-	-	Volts
*Holding Current ( $V_{AK} = 12 V_{dc}$ , Initiating Current = 200 mA, Gate Open)	$I_H$	-	18	40	mA
		-	-	80	
*Turn-On Time ( $I_{TM} = 25 A$ , $I_{GT} = 50 \text{ mAdc}$ )	$t_{gt}$	-	1.5	2.0	$\mu s$
Turn-Off Time ( $V_{DRM} = \text{rated voltage}$ ) ( $I_{TM} = 25 A$ , $I_R = 25 A$ ) ( $I_{TM} = 25 A$ , $I_R = 25 A$ , $T_J = 125^{\circ}C$ )	$t_q$	-	15	-	$\mu s$
		-	35	-	

**DYNAMIC CHARACTERISTICS**

Critical Rate of Rise of Off-State Voltage (Gate Open, Rated $V_{DRM}$ , Exponential Waveform)	$dv/dt$	-	50	-	$V/\mu s$
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\*Indicates JEDEC Registered Data.

2. Pulse Test: Pulse Width  $\leq 300 \mu s$ , Duty Cycle  $\leq 2\%$ .