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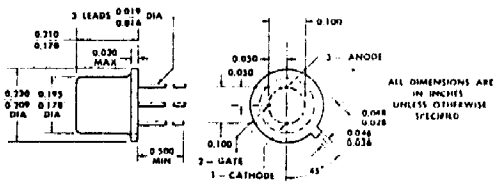
2N883

PNPN DIFFUSED SILICON REVERSE-BLOCKING TRIODE THYRISTOR

***mechanical data**



THE ANODE IS IN ELECTRICAL CONTACT WITH THE CASE.

THE GATE TERMINAL IS CONNECTED TO A P REGION.

ALL JEDEC TO-18 DIMENSIONS AND NOTES ARE APPLICABLE.

***absolute maximum ratings at (or below) 100°C case temperature (unless otherwise noted)**

		UNIT
Continuous Forward Blocking Voltage, V_{FR} (See Note 1)	400	v
Continuous Reverse Blocking Voltage, V_{RR} (See Note 2)	400	v
Continuous Anode Forward Current (See Note 3)	350	ma
Repetitive Peak Anode Forward Current (See Note 4)	20	a
Peak Anode Surge Current (See Note 5)	20	a
Peak Gate Reverse Voltage	5	v
Peak Gate Forward Current (Pulse width $\leq$ 8 msec)	250	ma
Operating Case Temperature Range	−65 to +150	°C
Storage Temperature Range	−65 to +150	°C
Lead Temperature 1/16 Inch from Case for 10 Seconds	230	°C

NOTES: 1. These values apply when the gate-cathode resistance $R_{GK} \leq 1\,k\Omega$.

2. These values apply when the gate-cathode resistance $R_{GK} \geq 1\,k\Omega$.

3. This value applies for continuous d-c operation with resistive load. Above 100°C derate according to Figure 1.

4. This value applies for square-wave pulses, PRR $\geq$ 60 pps, duty cycle $\leq$ 0.1%, when the device is operating at (or below) rated values of peak reverse blocking voltage and anode forward current.

5. This value applies for one 200-μsec square wave when the device is operating at (or below) rated values of peak reverse blocking voltage and anode forward current. Surge may be repeated after the device has returned to original thermal equilibrium.

*Indicates JEDEC registered data.

***electrical characteristics at 25°C case temperature (unless otherwise noted)**

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
I_{FR}	Static Anode Forward Blocking Current	V_F = Rated V_{FR}, R_{GK} = 1 kΩ		10	μa
		V_F = Rated V_{FR}, R_{GK} = 1 kΩ, T_C = 125°C		100	μa
I_{RR}	Static Anode Reverse Blocking Current	V_R = Rated V_{RR}, R_{GK} = 1 kΩ		10	μa
		V_R = Rated V_{RR}, R_{GK} = 1 kΩ, T_C = 125°C		100	μa
I_{GR}	Gate Reverse Current	V_{GR} = 2 v, I_A = 0		10	μa
I_{GT}	Gate Trigger Current	V_{AA} = 5 v, R_L = 100 Ω, $PW_G \geq 10$ μsec		200	μa
V_{GT}	Gate Trigger Voltage	V_{AA} = 5 v, R_L = 100 Ω, $PW_G \geq 10$ μsec	0.4	0.8	v
I_H	Holding Current	V_{AA} = 5 v, I_G = −150 μa		5	ma
V_F	Forward Voltage	I_F = 0.2 a, $R_{GK} \geq 1\,k\Omega$, See Note 6		1.5	v