

TOSHIBA THYRISTOR SILICON PLANAR TYPE

SF3G48, SF3J48, USF3G48, USF3J48

MEDIUM POWER CONTROL APPLICATIONS

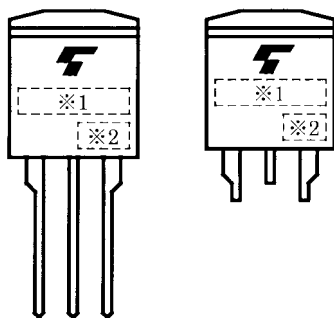
- Repetitive Peak Off-State Voltage : $V_{DRM} = 400,600V$
 Repetitive Peak Reverse Voltage : $V_{RRM} = 400,600V$
- Average On-State Current : $I_T (AV) = 3A$
- Gate Trigger Current : $I_{GT} = 10mA \text{ MAX.}$

Unit: mm

SF3G48-SF3J48		USF3G48-USF3J48	
<p>1. CATHODE 2. ANODE 3. GATE</p>		<p>1. CATHODE 2. ANODE (BACK SIDE) 3. GATE</p>	
JEDEC	—	JEDEC	—
JEITA	—	JEITA	—
TOSHIBA	13-10J1B	TOSHIBA	13-10J2B

Weight: 1.7g

MARKING



*1	MARK	F3G48	TYPE NAME	SF3G48, USF3G48
		F3J48		SF3J48, USF3J48
*2	Lot Number			
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MAXIMUM RATINGS

CHARACTERISTIC	SYMBOL	RATING	UNIT
Repetitive Peak Off-State Voltage and Repetitive Peak Reverse Voltage	SF3G48 USF3G48	400	V
	SF3J48 USF3J48	600	
Non-Repetitive Peak Reverse Voltage (Non-Repetitive <5ms, T _j = 0~125°C)	SF3G48 USF3G48	500	V
	SF3J48 USF3J48	720	
Average On-State Current	I _{T (AV)}	3	A
R.M.S On-State Current	I _{T (RMS)}	4.7	A
Peak One Cycle Surge On-State Current (Non-Repetitive)	I _{TSM}	50 (50Hz)	A
		55 (60Hz)	
I ² t Limit Value	I ² t	12.5	A ² s
Critical Rate of Rise of On-State Current (Note 1)	di / dt	100	A / μs
Peak Gate Power Dissipation	P _{GM}	5	W
Average Gate Power Dissipation	P _{G (AV)}	0.5	W
Peak Forward Gate Voltage	V _{FGM}	10	V
Peak Reverse Gate Voltage	V _{RGM}	-5	V
Peak Forward Gate Current	I _{GM}	2	A
Junction Temperature	T _j	-40~125	°C
Storage Temperature Range	T _{stg}	-40~125	°C

Note 1: V_{DRM} = 0.5 × Rated

I_{TM} ≤ 12A

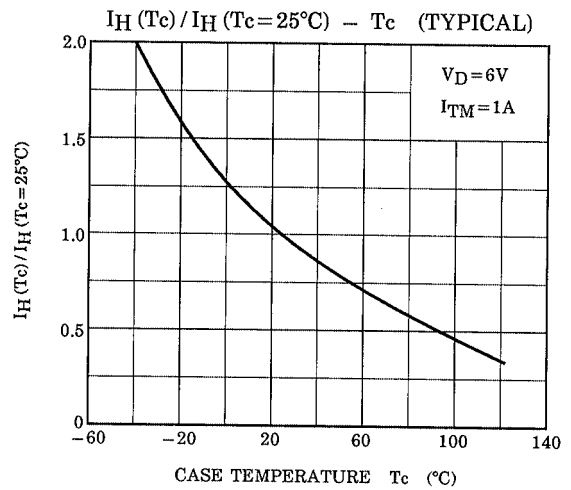
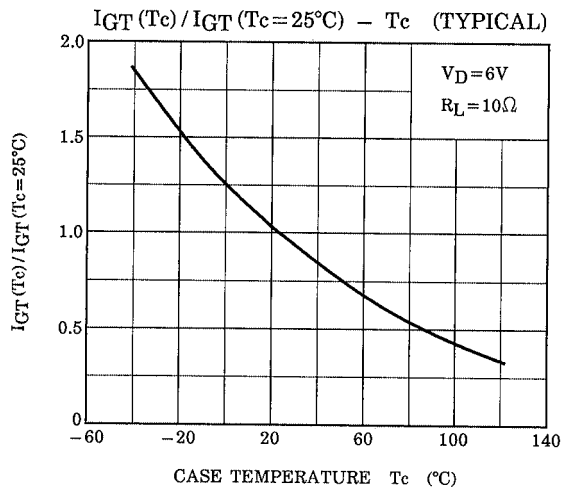
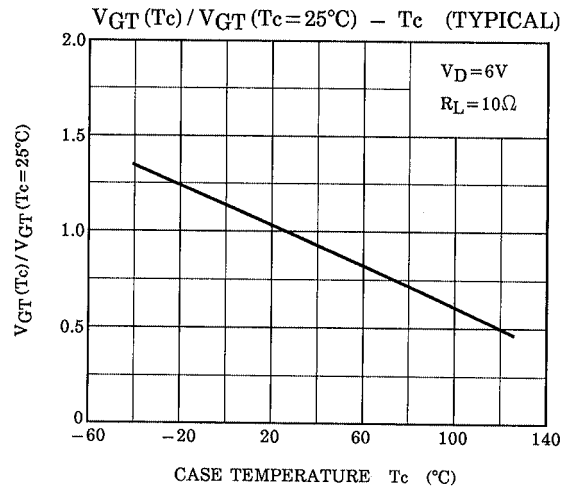
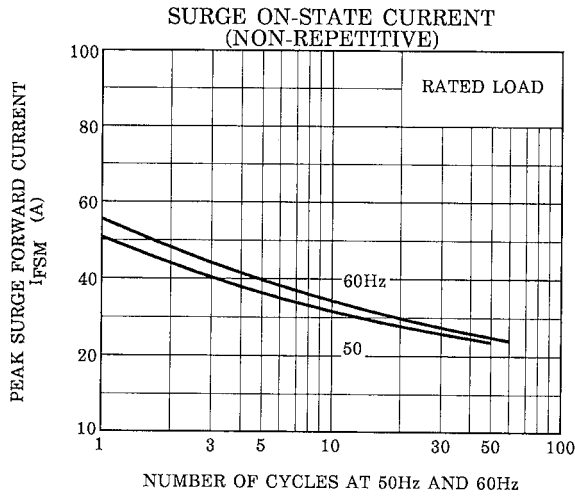
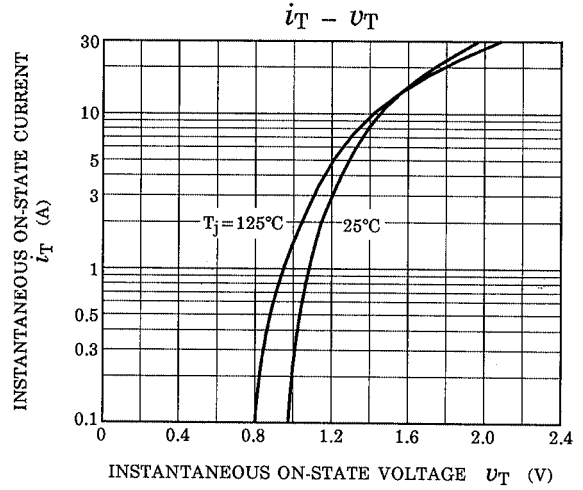
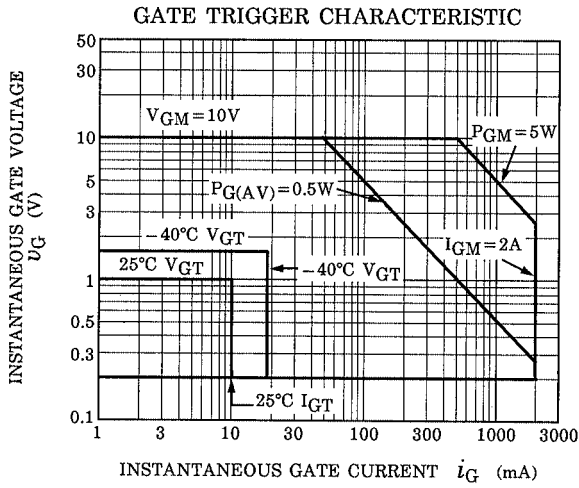
t_{gw} ≥ 10μs

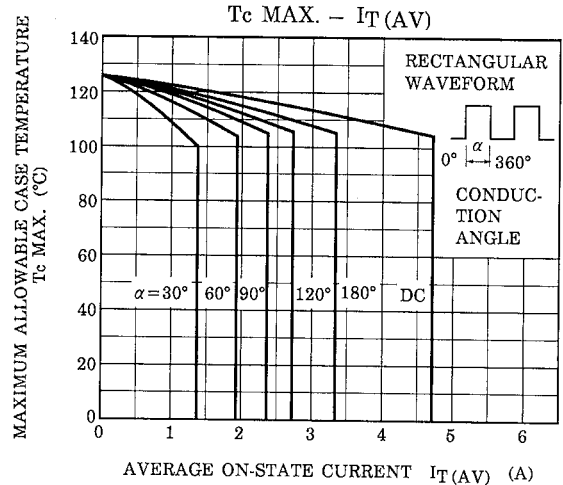
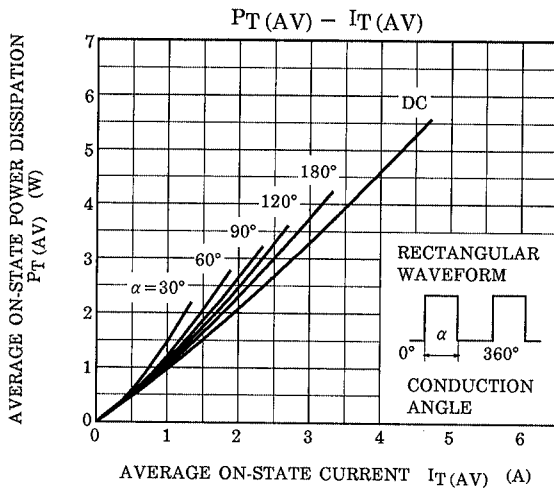
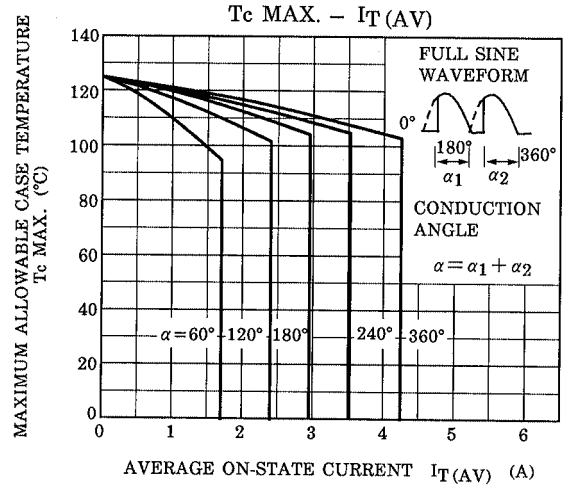
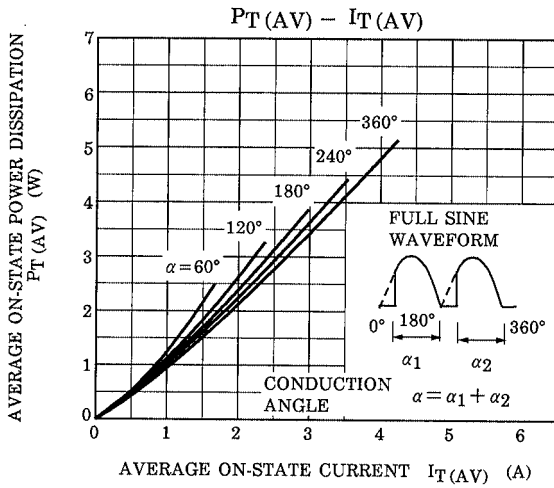
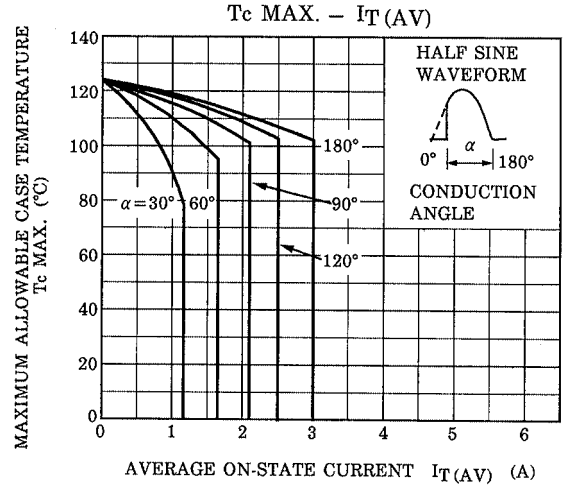
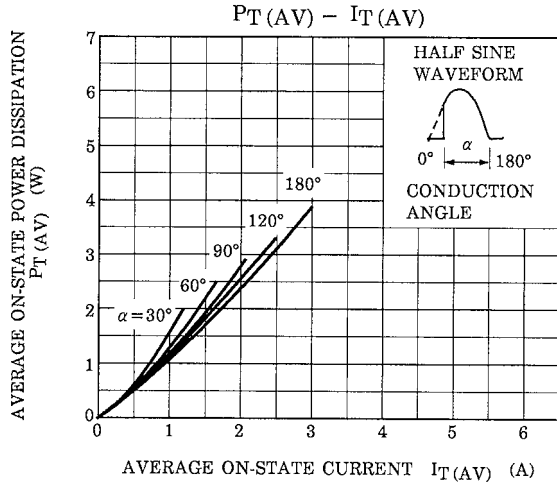
t_{gr} ≤ 250ns

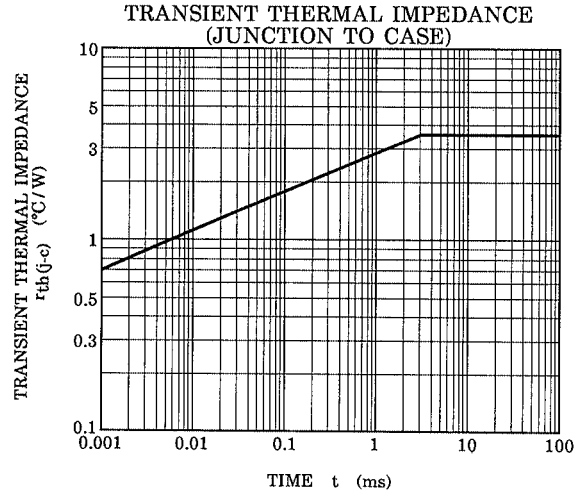
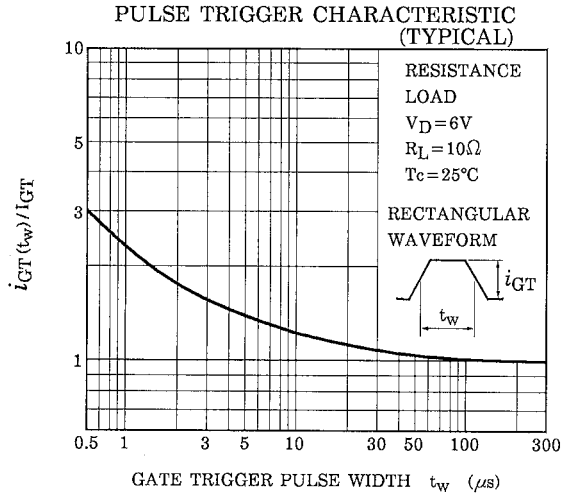
i_{gp} = I_{GT} × 2.0

ELECTRICAL CHARACTERISTICS (Ta = 25°C)

CHARACTERISTIC	SYMBOL	TEST CONDITION	MIN	TYP.	MAX	UNIT
Repetitive Peak Off-State Current and Repetitive Peak Reverse Current	I _{DRM} I _{RDM}	V _{DRM} = V _{RDM} = Rated	—	—	10	μA
Peak On-State Voltage	V _{TM}	I _{TM} = 12A	—	—	1.5	V
Gate Trigger Voltage	V _{GT}	V _D = 6V, R _L = 10Ω	—	—	1.0	V
Gate Trigger Current	I _{GT}		—	—	10	mA
Gate Non-Trigger Voltage	V _{GD}	V _D = Rated × 2 / 3, T _c = 125°C	0.2	—	—	V
Critical Rate of Rise of Off-State Voltage	dv / dt	V _{DRM} = Rated, T _c = 125°C Exponential Rise	—	50	—	V / μs
Holding Current	I _H	V _D = 6V, I _{TM} = 1A	—	—	40	mA
Latching Current	I _L	V _D = 6V, f = 50Hz t _{gw} = 50μs, i _G = 30mA	—	—	50	mA
Thermal Resistance	R _{th (j-c)}	Junction to Case, DC	—	—	3.6	°C / W







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