IBM

POWER8 Processor Datasheet for the Single-Chip Module

Revision Level DD 2.X

Advance

Version 1.7
5 April 2016

IBM ®

Contents

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Revision Log

Each release of this document supersedes all previously released versions. The revision log lists all significant changes made to the document since its initial release. In the rest of the document, change bars in the margin indicate that the adjacent text was modified from the previous release of this document.

Revision Date	Description
5 April 2016	Version 1.7. • Updated a note in *Table 3-4 Chip P0* on page 20.
11 March 2016	Version 1.6. • Corrected the MM_M1_P_PIN_CKC_DAT_15_N pin assignment in *Table 5-15 DMI Signals* on page 43. • Added notes 1 and 2 to *Table 5-19 JTAG Signals* on page 57.
29 February 2016	Version 1.5. • Changed dc to DC throughout. • Changed ac to AC throughout. • Revised *Section 3.3.4 PCIe Bus* on page 20. • Added a note to *Table 3-4 Chip P0* on page 20. • Reworded a sentence in *Section 4.2 Efficient Power Supply Oversubscription Capability* on page 23. • Revised a note in *Table 5-10 FSI Signals* on page 36. • Added a note to signals TS_CT_P_PIN_TDIODE_A5, TS_CT_P_PIN_TDIODE_C5, TS_CT_P_PIN_TDIODE_A13, and TS_CT_P_PIN_TDIODE_C13 in *Table 5-14 Thermal Diodes and Monitor Signals* on page 40. • Updated the *Glossary* on page 95.
4 January 2016	Version 1.4. • Revised *Section 1.1 Processor Feature Summary* on page 11. • Revised *Section 1.4 Power Management Support* on page 12. • Revised *Section 1.12 Related Documents and Models* on page 14. • Revised *Table 2-1 POWER8 SCM Technology* on page 15. • Added a note and the PE_PIN_P_E0_CK1_DAT_[00..07]_[P/N] pins to *Table 3-4 Chip P0* on page 20. • Revised *Section 3.3.4 PCIe Bus* on page 20. • Reworded the first paragraph in *Section 4 Power Management* on page 23. • Revised delta time range in *Table 4-1 System Power Sequencing* on page 26. • Added a note to the TS_PIN_P_CT_STBY_RESET_B signal in *Table 5-7 Test Signals* on page 33. • Added a note to the PV_CT_P_PIN_SPARE0 signal in *Table 5-7 Test Signals* on page 33. • Added a note to the PV_PIN_P_CT_FSI_IN_ENA1 signal in *Table 5-8 Control Signals* on page 34. • Added a note to the PV_PIN_P_CT_TPM_INTERRUPT signal in *Table 5-8 Control Signals* on page 34. • Revised a note in *Table 5-9 LPC Bus Signals* on page 35. • Revised the notes in *Table 5-10 FSI Signals* on page 36. • Revised *Section 5.2.7 SPI Signals* on page 38. • Revised *Section 5.2.8 I^{2}C Signals* on page 39. • Revised a note in *Table 5-12 I^{2}C Signals* on page 39. • Revised a note in *Table 5-13 Time-of-Day and Bus Synchronization Signal* on page 40. • Correction made to *Table 5-15 DMI Signals* on page 43. • Revised *Section 5.2.10 Thermal Diode and Monitor Signals* on page 40. • Updated cross-references to table notes in *Table 5-14 Thermal Diodes and Monitor Signals* on page 40. • Revised *Table 6-2 Frequencies and TDP* on page 61. • Revised a document name in *Section 6.2.2 Miscellaneous Signals* on page 61. • Changed "our systems" to "POWER systems" in *Section 6.3.1 Clock AC Specifications* on page 62. • Revised *Table 7-1 SCM Features* on page 71. • Revised the *Glossary* on page 95.

Revision Date	Description
24 July 2015	Version 1.3. • Revised *Section 1.12 Related Documents and Models* on page 14. • Revised *Table 2-1 POWER8 SCM Technology* on page 15. • Revised *Section 3.1 Service Interfaces* on page 17. • Revised *Section 3.3.4 PCIe Bus* on page 20. • Revised *Table 5-1 Signal Type Notation* on page 27. • Revised *Table 5-7 Test Signals* on page 33. • Revised *Table 5-8 Control Signals* on page 34. • Revised *Table 5-10 FSI Signals* on page 36. • Revised *Table 5-12 I^2C Signals* on page 39. • Revised *Table 5-17 PCIe Bus Signals* on page 53. • Revised *Table 6-2 Frequencies and TDP* on page 61. • Revised *Table 7-1 SCM Features* on page 71.
21 April 2015	Version 1.21. • Revised *Table 5-19 JTAG Signals* on page 57.
23 February 2015	Version 1.2. • Revised *Section 1.12 Related Documents and Models* on page 14. • Revised *Section 3.1 Service Interfaces* on page 17. • Removed unused signal definitions from *Section 5.1 Pin Naming Convention* on page 28. • Revised signal descriptions in *Section 5.2 Signals by Group* on page 29. • Removed the table previously known as *Table 5-5 Oscillator Switch Controls*. • Removed the table previously known as *Table 5-8 Pervasive Signals*. • Revised *Section 6.2 DC Electrical Characteristics* on page 61. • Removed the table previously known as *Table 6-2 Voltage Specifications*. • Removed the table previously known as *Table 6-3 Current Specifications.*. • Revised *Table 6-2 Frequencies and TDP* on page 61. • Added *Section 6.2.2 Miscellaneous Signals* on page 61. • Revised *Table 7-1 SCM Features* on page 71. • Revised pin descriptions for AE22, AE23, AG22, and AG23 in *Table 7-3 SCM Pin List* on page 73. • Revised *Glossary* on page 95.
17 June 2014	Version 1.1. • Removed the table previously known as *Table 5-4. Voltage Control Signals*. • Removed the table previously known as *Table 5-6. POWER8 Memory Buffer Signals*. • Removed NC signals from the following tables: *Table 5-3 Voltage Signals* on page 31, *Table 5-5 Oscillator Switch Controls* on page 29, *Table 5-4 PLL Signals* on page 31, *Table 5-6 I/O Minikerf Test Signals* on page 32, *Table 5-10 FSI Signals* on page 36, *Table 5-11 SPI Signals* on page 38, *Table 5-13 Time-of-Day and Bus Synchronization Signal* on page 40, *Table 5-14 Thermal Diodes and Monitor Signals* on page 40, *Table 5-15 DMI Signals* on page 43. • Added *Section 6.3.3 FSI AC Specifications* on page 68. • Added *Section 6.3.4 SPI AC Specifications* on page 70.
22 April 2014	Version 1.0 (initial version).

1. Introduction

This datasheet describes the IBM® POWER8® processor for the single-chip module (SCM), which consists of a single POWER8 processor. Each processor can have up to 12 cores enabled. The 12-core POWER8 processor is designed for use in servers and large-cluster systems. It uses IBM's <u>CMOS</u> 22 nm <u>SOI</u> technology with 15 metal layers. Each core has eight threads using simultaneous multithreading (SMT8). The SMT is dynamically tunable, so that each core can have one, two, four, or eight threads.

Figure 1-1 illustrates the POWER8 pinout diagram.

Figure 1-1. POWER8 Pinout Map
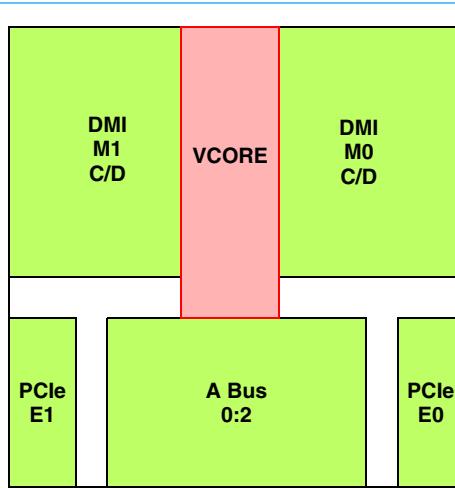
1.1 Processor Feature Summary

The POWER8 processor consists of the following main components:

- Twelve POWER8 chiplets, which contain a POWER8 core, an L2 cache, and an L3 cache.
- One on-chip accelerator engine
    - On chip: compression, encryption, data move initiated by the hypervisor
    - In core: user invocation encryption (<u>AES</u>, <u>SHA</u>)
- Two memory controllers that support the POWER8 memory buffer chip
- Processor bus interconnect
- Interface controllers that support three 1-byte differential A buses
- The interface controllers support the following interfaces:
    - Four differential memory buses (M0 - M3)
    - Three inter-node <u>SMP</u> buses (A0 - A2)
    - Configurable <u>PCIe</u> 3.0 buses: two ×16 lanes; one of the ×16 lanes can bifurcate into two ×8 lanes; the other ×16 lane is non-bifurcatible
- Power management
- Pervasive functions

1.2 Supported Technologies

The POWER8 processor supports the following technologies:

- Power ISA Book I, II, and III version 2.07

- PowerPC Architecture Platform Requirements (PAPR+), Version 2.1

- IEEE P754-2008 for binary and decimal floating-point compliant

- Big-endian, little-endian, strong-ordering support extension

- 50-bit real address, 68-bit virtual address

1.3 Interfaces

The primary service interface to the POWER8 processor is the flexible service interface (FSI) that runs at 166 MHz. See *Section 3.1 Service Interfaces* on page 17 for more information.

1.4 Power Management Support

Key features of the POWER8 processor in the SCM are:

- Hypervisor-directed power change requests using the Pstate mechanism

- Sensors

    - Digital thermal sensor (DTS2) $\pm5°C$

    - Off-chip analog thermal diode ±1 - $2°C$

    - Dedicated performance, microarchitecture, and event counters

- Accelerators

    - On-chip IBM PowerPC® 405 embedded processor core for real-time frequency and voltage modification

    - On-chiplet hardware assist (automated core chiplet management)

    - On-chip power management controls
        — Automated communications to the voltage regulation modules (VRMs)
        — Voltage and frequency sequencers for automated Pstate and idle state support

- Actuators

    - Per chiplet frequency control through the DPLL

    - Architected idle states: nap, sleep, and winkle; each with increasing power savings capability (and latency)

    - SPR Power Management Control Registers (PMCR, PMICR, PMSR) for hypervisor support

- Memory and DIMM throttling for memory subsystem power and thermal management

1.5 Thermal Specification

Thermal junction temperature (T_J) is measured by digital thermal sensors located on the chip. There are four sensors per core, which are averaged. The specified T_J is the worst case of these averages or the hottest core average. The maximum T_J is not allowed to exceed 85°C. The average T_J, at which the reliability is calculated, is 70°C. Margin does not need to be applied when measuring against the worst-case specification because the chip is sorted using the same thermal sensors. The digital thermal sensor has an absolute accuracy of ±5% and can be read out in Celsius (°C).

1.6 Signals

Section 5 Signals on page 27 describes the POWER8 processor signals.

1.7 Electrical

Section 6 Electrical Characteristics on page 59 discusses the DC and AC electrical characteristics of the POWER8 processor in the SCM.

1.8 Package Support

Section 7 Mechanical Specifications on page 71 describes the POWER8 SCM features and provides a pin list.

1.9 Processor Version Register

The POWER8 processor has the following Processor Version Register (PVR) values for the respective design revision levels.

Table 1-1. POWER8 Processor Version Register

POWER8 Design Revision Level	POWER8 PVR
DD 2.0	x'004D0200'

1.10 Marking Specification

The POWER8 Processor Single Chip Module Marking Drawing FC PLGA can be found on the IBM OpenPOWER Connect website.

1.11 Conventions

This section explains the number, bit field, instruction, and signal conventions that are used in this document.

1.11.1 Representation of Numbers

Numbers are generally shown in decimal format, unless designated as follows:

- Hexadecimal values are preceded by an "x" and enclosed in single quotation marks.
  For example: x'0A00'.
- Binary values in sentences are shown in single quotation marks.
  For example: '1010'.

Note: A bit value that is immaterial, which is called a "don't care" bit, is represented by an "x."

1.11.2 Bit Significance

The bit on the left represents the most-significant bit of a field. The bit on the right represents the least-significant bit of a field. For example, in CTL[0:31], 0 is the most-significant bit.

1.11.3 Other Conventions

- Instruction mnemonics are shown in lowercase, bold text. For example: **tlbivax**.
- I/O signal names are shown in uppercase.
- The notation [*] indicates all bits in a field or register.

An underscore indicates that a definition is displayed when you hoover your cursor over the underscored term.

1.12 Related Documents and Models

The documents available in OpenPOWER Connect, an online IBM technical library, are helpful in understanding the IBM POWER8 processor. Additional technical resources are available on the OpenPOWER Foundation web site. The following non-IBM documents are also useful:

- *For the Development of an Electrostatic Discharge Control Program for – Protection of Electrical and Electronic Parts, Assemblies and Equipment (Excluding Electrically Initiated Explosive Devices) (ANSI/ESD S20.20-2007)*
- *For the Protection of Electrostatic Discharge Susceptible Items - Packaging Materials for ESD Sensitive Items (ANSI/ESD S541-2008)*
- *I^2C Bus Specification (Version 2.1)*
- *PCI Local Bus Specification (Revision 3.0)*

2. Technologies

This section provides a high-level overview of the technologies implemented in the POWER8 processor.

2.1 General Parameters

Table 2-1 lists general parameters for the POWER8 processor.

Table 2-1. POWER8 SCM Technology

Feature	Description
Technology	22 nm silicon-on-insulator (SOI), 15 metal layers
Die Size	675 mm^2
Chip Package (SCM)	See *Table 7-1 SCM Features* on page 71 for details.
Signal I/O	2296
Frequency Range (nominal)	2.095 GHz (140 W and 145 W) 2.328 GHz (130 W and 135 W) 2.561 - 3.325 GHz (190 W)
Power	130 W, 135 W, 140W, 145 W, or 190 W

3. Interfaces

3.1 Service Interfaces

The POWER8 processor has multiple service interfaces that are used for initialization during boot. The service interfaces are also accessible by using the debug box. The primary entry point to the POWER8 processor service interface is the flexible service interface (FSI), a serial interface that runs at 166 MHz.

The POWER8 SCM provides the following FSIs:

- Two FSI slaves for connecting in the debug box and multichip SMP.

- Four FSI masters for communicating with the POWER8 memory buffer chip.

- Four FSI masters for communicating with other POWER8 chips in the system. One POWER8 chip is defined as the master and is responsible for initializing the other POWER8 chips over these FSIs.

The POWER8 SCM provides the following additional service interfaces:

- One serial peripheral interconnect (SPI) master for controlling the core and cache voltage regulators.

- One SPI master for on-chip controller (OCC) management.

- One LPC bus for connecting to the BMC.

- One I^{2}C slave for BMC-to-OCC communication.

- Two SEEPROM interfaces to load the on-chip SEEPROMs. This path can be disabled for secure boot reasons.

- Two I^{2}C masters for controlling LEDs, PCIe cards, and so on. The I^{2}C masters can be manipulated from the OCC or hostboot code.

- Two high-speed SPI master buses for off-chip VRM control and voltage slewing.

- One time-of-day clock.

3.2 Supported Processor Interfaces

This section gives an overview of the physical layer and on-chip initialization provided by the POWER8 processor.

The POWER8 SCM supports the following types of drivers and receivers:

- A Bus: High-speed differential at 6.4 Gb/s for the memory interface

- Memory I/O: High-speed differential at 9.6 Gb/s for the memory interface

Table 3-1 lists the requirements relative to the operational mode definitions.

Table 3-1. Interface Operational Mode Definitions

Mode Name	Definition
Initialization	The act of aligning and locking the data eye and bit lanes plus additional deltas relative to re-alignment and re-locking.
Functional	Passing workload data and maintaining signal integrity post-initialization.
Power Saving	All related capabilities for minimizing unused and idle lane power consumption.
Test	Capabilities related to hardware manufacturability.
Diagnostic	Bringup lab characterization of interface performance capabilities.

3.2.1 Bus Highlights

Table 3-2 highlights the differences between the A bus and memory I/O bus. See the [POWER8 Processor User's Manual for the Single-Chip Module](#) for additional information.

Table 3-2. A Bus and Memory Bus Highlights

	A Bus	Memory Bus
Frequency	6.4 Gb/s	9.6 Gb/s
Initialization Mode Requirement	6.4 - 4.8 Gb/s	9.6 - 8.0 Gb/s
Spare Lane Detect	Data failover One signal total per bus per port	Data failover Two signals total per bus per port
Functional Mode Specification	6.4 - 4.8 Gb/s	9.6 - 8.0 Gb/s
Power-Saving Mode Requirement	No power-saving mode support	No power-saving mode support
Test Mode Requirement	6.4 - 4.8 Gb/s[1]	9.6 - 8.0 Gb/s[1]
Driver Features	• 4:1 data serialization at 6.4 Gb/s • Programmable drive strengths • Impedance calibration • Post cursor FFE levels and amplitude margining • Feed forward equalization • Precompensation • DC test mode	• 4:1 data serialization at 9.6 Gb/s • Programmable drive strengths • Impedance calibration • Post cursor FFE levels and amplitude margining • Feed forward equalization • Precompensation • DC test mode
Receiver Features	• Input descrambler • 4:1 de-serializer • Phase interpolator • DC offset calibration	• Input descrambler • 4:1 de-serializer • Phase interpolator • DC offset calibration • DFE-1 (1-tap decision feedback equalizer)

1. Subject to PLL range limitations and a test frequency of 200 MHz.

3.3 PCI Express Controller

The PCI Express controller (PEC) bridges between the internal processor bus and the high-speed serial (HSS) links that drive the PCI Express I/O. The PEC acts as a processor bus master on behalf of the PCI Express port, converting inbound memory read and write packets into processor bus DMA traffic. The PEC also acts as a processor bus slave, transferring processor load and store commands to the PCI Express devices attached to the port.

3.3.1 Specification Compliance

The PEC is compliant with the following IBM and industry standards:

- *POWER Architecture Platform Requirements (PAPR+) Specification*, Version 2.1
- *I/O Design Architecture v2 (IODA2) Specification, Version 2.4+*
- *PCI Express Base Specification Revision 3.0*, v0.71

3.3.2 PEC Feature Summary

- PCI Express Generation 3 root complex (RC)

  - Backwards compatible with generation 1 and generation 2
  - 2.5, 5.0, and 8 GT/s signalling rate

- Thirty-two PCIe I/O lanes configurable to three independent root complexes

- Each root complex has 256 partitionable endpoints (PE) for LPAR support

- TCE-based address translation for DMA requests

  - 50-bit address support
  - Translation validation table based on PCI routing ID

- 2048 MSI interrupts per RC

- Eight LSI interrupts per RC

- IBM enhanced error handling (EEH) support

- Processor bus cache-inhibited space segmented by PEC

  - PCI 32-bit memory space segmented into 256 domains by the memory domain table
  - PCI 64-bit memory space segmented by 16 M64 BARs with 16 segments each

- Support for ECRC

- Support for lane wrapping

- Support for PCIe atomic operations and TLP hints

3.3.3 Supported Configuration

The 32 lanes of HSS I/O can be configured to support three independent PCIe buses. *Table 3-3* describes the maximum lane allocation. In addition to supporting PCI operations, the HSS I/O can be allocated for use by the processor bus SMP interface.

Table 3-3. Supported I/O Configurations

PEC0	PEC1	PEC2
16	16	Unused
16	8	8
8	16	Unused
8	8	8
Unused	16	Unused
Unused	8	8

3.3.4 PCIe Bus

The POWER8 SCM has a total of 32 PCIe Gen3 lanes. Each POWER8 processor provides two ×16 lanes. One of the ×16 lanes (E1) can bifurcate into two ×8 lanes; the other ×16 lane is non-bifurcatible. The PCIe Gen3 bandwidth is 1 GB/s per lane. The lanes can be reversed for easier routing if required. The polarity can also be reversed on a lane-by-lane basis.

Table 3-4. Chip P0 (Sheet 1 of 2)

Chip	Interface	Mode		Pins	Note
P0	E1	×16	Data Lanes	PE_PIN_P_E1_CK0_DAT_[00:07]_[P/N] PE_PIN_P_E1_CK1_DAT_[00:07]_[P/N]	
			Clocks	PE_CT_P_PIN_E1_SLOT_CLK0_[P/N] PE_CT_P_PIN_E1_SLOT_CLK1_[P/N]	
			Reset	PE_CT_P_PIN_E1_PERST0_B PE_CT_P_PIN_E1_PERST1_B	1
			Present	PE_PIN_P_CT_E1_PRSNT0_B PE_PIN_P_CT_E1_PRSNT1_B	2

1. IBM uses a 4.7 KΩ pull-up. Follow PCIe slot/device endpoint specifications. If the bus is not used, this pin can be a no connect. See *Table 5-17* on page 53 for additional information.
2. The PRSNT signal has an internal 1 KΩ pull-up to 1.1 V. An additional onboard pull-up of the specified value range is only required if the signal is part of a level-translation circuit. See *Table 5-17* on page 53 for additional information.
3. When wiring to a ×8 slot that supports a ×4 adapter, the following rules must be followed:
   - For E1_CK0_DAT[00:07], the bus cannot be reversed.
   - For E1_CK1_DAT[00:07], the bus must be reversed.
4. This bus is ×16 mode only (non-bifurcatible). Thus, there is only one slot clock.

Table 3-4. Chip P0 (Sheet 2 of 2)

Chip	Interface	Mode	Pins		Note
P0	E1	×8	Data Lanes	PE_PIN_P_E1_CK0_DAT_[00:07]_[P/N]	3
			Clocks	PE_CT_P_PIN_E1_SLOT_CLK0_[P/N] PE_CT_P_PIN_E1_SLOT_CLK1_[P/N]	
			Reset	PE_CT_P_PIN_E1_PERST0_B PE_CT_P_PIN_E1_PERST1_B	1
			Present	PE_PIN_P_CT_E1_PRSNT0_B PE_PIN_P_CT_E1_PRSNT1_B	2
P0	E1	×8	Data Lanes	PE_PIN_P_E1_CK1_DAT_[00:07]_[P/N]	3
			Clocks	PE_CT_P_PIN_E1_SLOT_CLK0_[P/N] PE_CT_P_PIN_E1_SLOT_CLK1_[P/N]	
			Reset	PE_CT_P_PIN_E1_PERST0_B PE_CT_P_PIN_E1_PERST1_B	1
			Present	PE_PIN_P_CT_E1_PRSNT0_B PE_PIN_P_CT_E1_PRSNT1_B	2
P0	E0	×16	Data Lanes	PE_PIN_P_E0_CK0_DAT_[00:07]_[P/N] PE_PIN_P_E0_CK1_DAT_[00:07]_[P/N]	
			Clocks	PE_CT_P_PIN_E0_SLOT_CLK0_[P/N]	4
			Reset	PE_CT_P_PIN_E0_PERST0_B PE_CT_P_PIN_E0_PERST1_B	1
			Present	PE_PIN_P_CT_E0_PRSNT0_B PE_PIN_P_CT_E0_PRSNT1_B	2

1. IBM uses a 4.7 KΩ pull-up. Follow PCIe slot/device endpoint specifications. If the bus is not used, this pin can be a no connect. See *Table 5-17* on page 53 for additional information.
2. The PRSNT signal has an internal 1 KΩ pull-up to 1.1 V. An additional onboard pull-up of the specified value range is only required if the signal is part of a level-translation circuit. See *Table 5-17* on page 53 for additional information.
3. When wiring to a ×8 slot that supports a ×4 adapter, the following rules must be followed:
   - For E1_CK0_DAT[00:07], the bus cannot be reversed.
   - For E1_CK1_DAT[00:07], the bus must be reversed.
4. This bus is ×16 mode only (non-bifurcatible). Thus, there is only one slot clock.

3.4 SMP Bus

The POWER8 SCM brings out a total of three 2-byte A buses (A0 - A2). The differential A bus runs at 6.4 Gb/s. For a two-socket system, connecting the two sockets with at least two of the three A buses is recommended. An A-bus port of socket 1 can go to any A-bus port of socket 2 in a two-socket system.

3.5 DMI Bus

The POWER8 SCM brings out a total of four DMI interfaces at 9.6 Gb/s. The total pin bandwidth of one DMI interface is 28.8 GB/s.

See the *POWER8 Memory Buffer Datasheet* for bandwidth requirements.

4. Power Management

The POWER8 processor chip uses several traditional power-saving techniques to reduce peak power and thermal design-point (TDP) power. For example, latches and arrays are clock gated when they are not needed. Also, individual cores, or full core chiplets, are dynamically power gated when the cores are not being used. That is, the power to the cores is turned off.

The POWER8 processor uses adaptive power management techniques to reduce average power. These techniques, collectively known as IBM EnergyScale™, proactively take advantage of variations in workload, environmental condition, and overall system utilization. Coupled with a policy direction from the customer and feedback from the hypervisor or operating system that is running on the machine, this is used to determine modes of operation and the best power and performance trade-off to implement during runtime to meet customer goals and achieve the best possible performance.

4.1 Power Gating and On-Chip, Per-Core Voltage Regulation

Offering competitive chip and system designs requires the capability to dynamically adjust power consumption and performance levels to meet the needs of changing workloads. The POWER8 processor offers industry-leading features to achieve this goal.

During idle periods, each chiplet can individually power gate or "turn off" the supply to either the core or to both the core and the associated L3 cache region to reduce chiplet idle power. The gating header in the POWER8 processor is driven to an elevated voltage when off by using an on-chip charge pump. This technique increases the leakage power reduction, bringing the total DC power reduction achieved by power gating to 50 - 100x. As a result, the power-gated power consumption is less than 1% of the chiplet idle power.

Power gating can also be used to virtually eliminate the parasitic leakage power of deconfigured cores in a partial-good product offering by leaving the headers for unconfigured cores in an always gated state.

The idle power saved by power gating can be used to boost the frequency of the remaining operational cores. Using this technique, the nominal frequency of operating four cores can exceed the 12-core operating frequency by almost 30%.

4.2 Efficient Power Supply Oversubscription Capability

System bulk power supplies redundantly deliver worst-case power, which is significantly more power than is typically consumed. Typical workloads, parts, and environments are much less power hungry than the worst case. Also, power delivery failure is very uncommon.

This excess power capacity can be converted into performance by using oversubscription. By oversubscribing the power supply, the processor is allowed to run at voltages and frequencies that exceed the power limit of the system under a worst-case workload and with failure of one of the redundant supplies.

Robust system operation must be maintained in spite of oversubscription. To do this, the processor must be able to throttle back power quickly enough to avoid an overcurrent condition in the remaining bulk power supply in case of a failure in the redundant supply or a sudden power spike.

POWER8 systems increase oversubscription capabilities to 1.5x resulting in performance gains. The fundamental limit to power supply oversubscription is the circuit breakers in the utility or UPS when the redundant power fails. The system must be able to throttle back to consuming power less than the non-oversubscribed limit before the EXP(Current) × Time limit of the breaker is violated. *Figure 4-1* shows a representative curve of allowed oversubscription versus response time.

Figure 4-1. Oversubscriptions versus Response Time
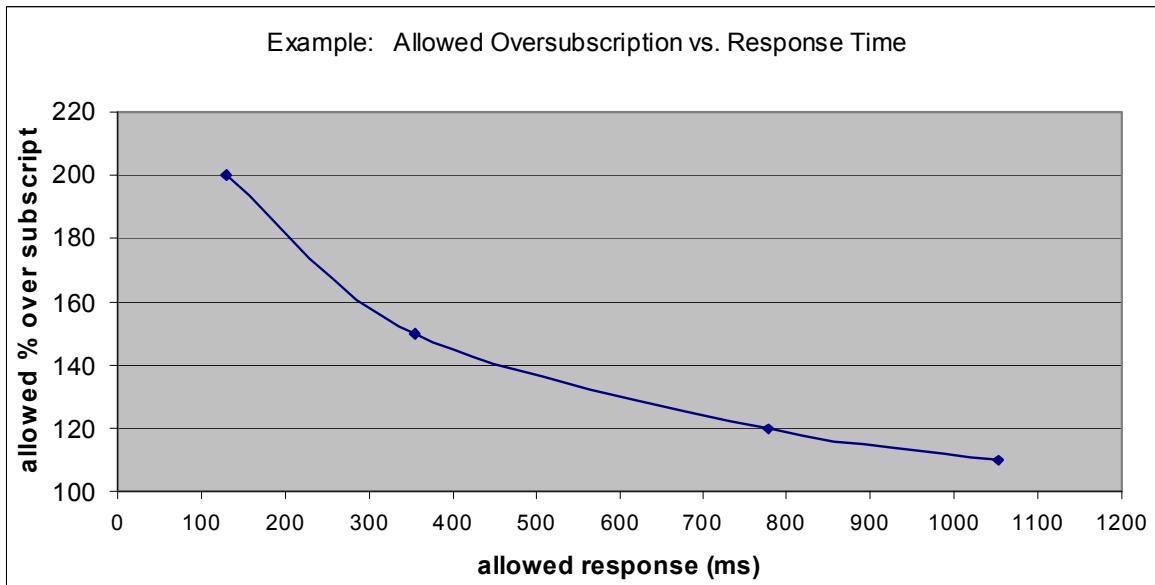
To improve response time, a dedicated C4 pin directly signals a power-supply error to the on-chip controller (OCC).

The OCC engine can then use its internal power-actuation capabilities to rapidly reduce power. The POWER8 processor offers the following forms of power reduction:

- The OCC can force a halt in the fetch or issue of instructions to significantly reduce AC power within approximately 10 cycles.

- The OCC can use the DPLL to reduce frequency at a rate of approximately 25 MHz/μs. The AC power reduces linearly with the frequency reduction.

Based on these capabilities, the POWER8 processor can throttle its power to a small fraction of the nominal operating power in less than 5 ms of receiving the system signal indicating a power supply failure.

The other key to enabling significant oversubscription is rapid detection of a power supply failure.

4.3 Chip Hardware Power-Management Features

4.3.1 Chiplet Voltage Control

The POWER8 processor supports several voltage regulator module (VRM) control mechanisms for multiple system configurations. The core chiplets are on a separate voltage plane than the other Nest components of the chip. The chip-level power-management control (PMC) macro and the OCC are, in combination, programmable to support these configurations.

Core chiplets all share the same voltage plane and must run with the "highest common denominator," which means that the core demanding the highest voltage sets the value of the voltage rail. The OCC is responsible for establishing the best frequency, and therefore voltage bounds based on the workload running, the power/performance efficiency policy selected by the customer, and the system budgets established by the thermal management component.

4.3.2 Chip-Level Voltage Control Sequencing

The external VRMs (eVRMs) sourcing the logic (V_{DD}) and array (V_{CS}) rails are controlled by voltage control interfaces from the POWER8 chip. These interfaces use serial peripheral interconnect (SPI) signaling to a VRM chipset that converts the addressed VID command to industry-standard Intel VRM-11 interface components or others, as implemented by the VRMs.

4.3.3 SPIVID VRM Control Sequencing

The V_{DD} target voltage and the relevant V_{CS} offset is sent in one command to the VRM set. The target might be the full voltage swing request (V_{MAX} to V_{MIN} or vice-versa) or any subset. With the V_{DD} target and associated V_{CS} offset value, the VRMs, through sampling of load lines, manage the offset of the two rails during the slew.

4.4 System Power Sequencing

The power sequencing design must check the PGOOD status before continuing to the next step. The sequencer must allow for some amount of minimum time after PGOOD issues before continuing as specified in *Table 4-1*.

Table 4-1. System Power Sequencing

Voltage Domain	Delta Time (ms)	Comments
Typically, system rails associated with service processors, I/O, and storage are enabled before the processor/memory power is enabled. This guide does not cover these specifics.		
AV_{DD}	0.1 - 20	The POWER8 memory buffer and the POWER8 processor can be combined.
V_{IO}	0.1 - 20	The POWER8 memory buffer and the POWER8 processor can be combined.
POWER8 V_{DD}	0.1 - 20	
POWER8 V_{CS}	0.1 - 20	
Additional processors can be added here in the same sequence or paralleled, so that all V_{DD} come on at the same time followed by all V_{CS}.		
V_{PCI}	0.1 - 20	The POWER8 memory buffer and POWER8 processor can be combined.
POWER8 memory buffer V_{DD}	0.1 - 20	
POWER8 memory buffer V_{CS}	0.1 - 20	
Additional POWER8 memory buffer chips can be added here in the same sequence or paralleled, so that all V_{DD} come on at the same time followed by all V_{CS}.		
Marks the beginning of the secondary sequence, memory initialization pause.[1]		
V_{PP}	0.1 - 20	DDR4 only. Must always be greater than V_{MEM}.
$V_{MEM/DDR}$	0.1 - 20	DDR3 or DDR4. Must be less than 200 ms after V_{PP}. V_{TERM} tracks this domain/2 and comes on at the same time.
Additional V_{PP}/V_{MEM} domains can be added in the same sequence or can be paralleled, so that they all come on together.		
1. The secondary sequence pause is required for the self-boot engine (SBE) to complete memory initialization tasks. At this step, the processor indicates to the service processor or power sequencer what the memory voltage must be programmed to and then indicates when to turn on the memory power rails. The memory voltage calculation is performed on the processor with information from the DIMM VPD and memory configuration.		

5. Signals

This section describes the POWER8 signal groups. They are arranged in functional groups according to their interface. *Table 5-1* lists the signal type notation.

Table 5-1. Signal Type Notation

Direction	Signal Type
Rec	Receiver (input).
RecDiff	Receiver differential pair signal polarity (P or N).
Drv	Driver (output).
DrvDiff	Driver differential pair signal polarity (P or N).
AnlgIn	Analog input.
AnlgOut	Analog output.
BiDi	Bi-directional input/output signal.
SH	Share test for manufacturing test only. No functional use.

Table 5-2 lists the buffer types.

Table 5-2. Signal Buffer Type Notation

Signal	Description
CMOS	CMOS buffers.
OD	Open drain.
Analog	Analog.
EI4	Elastic interface 4.
EDI	Elastic differential I/O.
PCIe	PCI Express interface signals. These signals are compatible with PCI Express 3.0.
Asynchronous	Signal has no timing relationship with any reference clock.
REF	Voltage reference signal.
PLL/CLK	PLL clock.

5.1 Pin Naming Convention

The general pin-naming pattern is:

prefix_source_connectionType_sink_clockGroup_sigType_bitNumber_diffBit

Prefix - the type of bus or signal type being connected. The following abbreviations are used:

DR	DDR memory bus
MM	Memory bus
NA	A bus
PE	PCIe
PV	Pervasive
TS	Test

Source and Sink - the specific component and bus being connected. The following abbreviations are used:

CT	Chip test or pervasive
M0	Memory channel 0 bus
E0	PCIe 0 bus
A0	A0 bus
PIN	Module pin

Connection Type

P	Point-to-point
B	Bidirectional
M	Multipoint

Clock Group

CK0	Clock group 0
CKA	Clock group A

Signal type (sigType)

CLK	Clock signal
DAT	Data signal

Bit Number - bit strand number, if needed; uses padding zeros.

Differential Bit (diffBit) - differential pair signal polarity (P or N), if needed.

5.2 Signals by Group

5.2.1 Voltage and Ground Signals

Table 5-3 lists the voltage and ground signals.

Table 5-3. Voltage and Ground Signals (Sheet 1 of 2)

Signal	Description	Pin
GND	Ground	A04, A07, A12, A13, A16, A21, A26, A29, A30, A33, A38, A39, A44, A45, A48, B03, B08, B13, B14, B15, B20, B25, B28, B29, B32, B37, B38, B43, B44, B47, C02, C03, C04, C09, C14, C19, C24, C27, C28, C29, C30, C31, C36, C37, C42, C43, C46, D02, D03, D04, D05, D10, D15, D18, D23, D24, D25, D26, D27, D28, D29, D30, D35, D36, D41, D42, D45, E03, E04, E06, E11, E16, E17, E22, E23, E24, E25, E26, E27, E28, E29, E30, E31, E36, E37, E42, E43, E44, F04, F05, F07, F12, F15, F16, F21, F22, F23, F24, F25, F26, F28, F29, F30, F35, F36, F41, F42, F43, F48, G05, G06, G08, G13, G14, G15, G20, G21, G22, G23, G24, G25, G26, G28, G29, G34, G35, G40, G41, G42, G47, H01, H06, H07, H09, H12, H13, H14, H15, H16, H17, H19, H20, H21, H22, H23, H24, H26, H27, H30, H31, H32, H34, H39, H40, H41, H46, J02, J07, J09, J10, J11, J12, J13, J14, J15, J16, J19, J22, J23, J24, J26, J27, J29, J31, J35, J36, J38, J39, J40, J45, K03, K08, K09, K11, K14, K16, K18, K20, K22, K24, K26, K28, K30, K32, K34, K36, K38, K39, K44, L01, L04, L08, L13, L15, L17, L19, L21, L23, L25, L27, L29, L31, L33, L38, L43, L48, M02, M05, M08, M10, M12, M14, M16, M18, M22, M26, M28, M30, M32, M34, M38, M42, M47, N03, N06, N08, N09, N11, N12, N13, N15, N17, N21, N25, N29, N31, N33, N36, N38, N39, N41, N46, P04, P07, P09, P14, P16, P18, P20, P22, P26, P28, P30, P32, P34, P39, P40, P45, R05, R10, R11, R12, R13, R15, R17, R21, R23, R25, R29, R31, R33, R36, R37, R39, R44, T01, T06, T10, T16, T18, T20, T22, T26, T28, T30, T32, T34, T38, T43, T48, U02, U07, U09, U10, U11, U12, U13, U15, U17, U19, U21, U25, U27, U29, U31, U33, U35, U37, U42, U47, V02, V03, V05, V08, V11, V14, V16, V18, V20, V26, V28, V32, V34, V35, V41, V46, W01, W02, W03, W04, W05, W06, W08, W09, W10, W13, W15, W17, W19, W21, W23, W25, W27, W29, W31, W33, W36, W37, W38, W40, W45, Y07, Y08, Y14, Y16, Y18, Y20, Y24, Y26, Y28, Y32, Y34, Y35, Y38, Y39, Y40, Y44, AA13, AA15, AA17, AA19, AA21, AA23, AA25, AA27, AA29, AA31, AA33, AA36, AA40, AA43, AA48, AB11, AB12, AB14, AB16, AB18, AB20, AB26, AB28, AB32, AB34, AB35, AB37, AB38, AB39, AB40, AB42, AB47, AC10, AC13, AC15, AC17, AC19, AC21, AC23, AC27, AC29, AC31, AC33, AC36, AC38, AC39, AC40, AC41, AC46, AC47, AD05, AD06, AD07, AD08, AD09, AD10, AD16, AD20, AD24, AD26, AD28, AD30, AD32, AD34, AD35, AD38, AD41, AD43, AD45, AD46, AD47, AD48, AE01, AE02, AE03, AE04, AE10, AE11, AE12, AE13, AE15, AE17, AE19, AE21, AE25, AE29, AE33, AE36, AE37, AE38, AE39, AE40, AE41, AE42, AE43, AE44, AE45, AE46, AE48, AF14, AF16, AF18, AF20, AF22, AF24, AF26, AF28, AF30, AF32, AF34, AF35, AF37, AF39, AF41, AF42, AF44, AF46, AG13, AG15, AG17, AG21, AG29, AG31, AG33, AG36, AG39, AG42, AG47, AH14, AH16, AH18, AH20, AH22, AH24, AH26, AH28, AH30, AH32, AH34, AH35, AH38, AH39, AH42, AH43, AH48, AJ07, AJ10, AJ11, AJ12, AJ13, AJ15, AJ17, AJ21, AJ23, AJ25, AJ29, AJ31, AJ33, AJ36, AJ37, AJ39, AJ42, AJ44, AK01, AK02, AK03, AK04, AK05, AK06, AK08, AK11, AK14, AK16, AK18, AK20, AK22, AK24, AK26, AK28, AK30, AK32, AK34, AK35, AK37, AK40, AK42, AK45, AL02, AL03, AL05, AL08, AL10, AL13, AL15, AL21, AL23, AL29, AL33, AL36, AL38, AL41, AL42, AL46, AM02, AM07, AM09, AM11, AM12, AM14, AM16, AM18, AM20, AM22, AM24, AM26, AM28, AM30, AM32, AM34, AM35, AM38, AM42, AM47, AN01, AN06, AN10, AN13, AN15, AN17, AN19, AN21, AN23, AN27, AN29, AN31, AN33, AN37, AN38, AN43, AN48, AP05, AP11, AP14, AP16, AP18, AP20, AP24, AP26, AP28, AP32, AP34, AP36, AP37, AP38, AP39, AP44, AR04, AR07, AR09, AR12, AR13, AR15, AR17, AR19, AR21, AR23, AR27, AR29, AR31, AR33, AR40, AR45, AT03, AT06, AT08, AT09, AT11, AT14, AT16, AT18, AT20, AT24, AT26, AT28, AT32, AT34, AT36, AT37, AT41, AT46, AU02, AU05, AU08, AU10, AU13, AU15, AU17, AU19, AU21, AU23, AU25, AU27, AU29, AU31, AU33, AU38, AU42, AU47, AV01, AV04, AV08, AV12, AV14, AV16, AV18, AV20, AV22, AV24, AV26, AV28, AV30, AV32, AV34, AV36, AV38, AV43, AV48, AW03, AW08, AW09, AW11, AW13, AW15, AW17, AW19, AW21, AW23, AW25, AW27, AW29, AW37, AW39, AW44, AY02, AY07, AY10, AY11, AY14, AY19, AY22, AY25, AY28, AY31, AY34, AY36, AY37, AY38, AY40, AY45, BA01, BA06, BA09, BA12, BA13, BA16, BA19, BA20, BA23, BA26, BA29, BA30, BA31, BA32, BA34, BA39, BA41, BA46, BB05, BB08, BB13, BB14, BB15, BB20, BB21, BB24, BB27, BB29, BB34, BB35, BB40, BB42, BB47, BC04, BC07, BC12, BC15, BC16, BC21, BC22, BC25, BC27, BC30, BC35, BC36, BC41, BC43, BC48, BD03, BD06, BD11, BD16, BD17, BD22, BD23, BD26, BD28, BD29, BD31, BD36, BD37, BD42, BD43, BD44, BE02, BE05, BE10, BE15, BE18, BE23, BE24, BE25, BE26, BE27, BE30, BE35, BE36, BE41, BE42, BE45, BF01, BF04, BF09, BF14, BF19, BF24, BF27, BF28, BF31, BF36,

Table 5-3. Voltage and Ground Signals (Sheet 2 of 2)

Signal	Description	Pin
GND (continued)	Ground	BF37, BF42, BF43, BF46, BG03, BG08, BG13, BG15, BG20, BG25, BG28, BG29, BG32, BG37, BG38, BG43, BG44, BG47, BH04, BH07, BH12, BH13, BH16, BH21, BH26, BH29, BH30, BH33, BH38, BH39, BH44, BH45, BH48
AVDD_1P50	Analog VDD	AD11, AD12
DVDD_1P50	Digital VDD	AC11, AC12
VCS_0P97	VCS	N19, N22, N27, N30, R19, R22, R27, R30, V19, V22, V27, V30, Y19, Y22, Y27, Y30, AB19, AB22, AB27, AB30, AG19, AG27, AG30, AJ19, AJ22, AJ27, AJ30, AL19, AL22, AL27, AL30, AP19, AP22, AP27, AP30, AT19, AT22, AT27, AT30
VDD_0P89	VDD	M15, M17, M19, M21, M23, M27, M29, M31, M33, N14, N16, N26, N28, N32, N34, P15, P17, P19, P21, P23, P25, P27, P29, P31, P33, R16, R18, R20, R24, R26, R28, R32, R34, T15, T17, T19, T21, T23, T27, T29, T31, T33, U14, U16, U18, U20, U22, U26, U28, U30, U32, U34, V15, V17, V21, V23, V25, V29, V31, V33, W14, W16, W18, W20, W22, W24, W26, W28, W30, W32, W34, Y15, Y17, Y21, Y23, Y29, Y31, Y33, AA14, AA16, AA18, AA20, AA22, AA24, AA26, AA28, AA30, AA32, AA34, AB15, AB17, AB21, AB23, AB29, AB31, AB33, AC14, AC16, AC18, AC20, AC22, AC26, AC28, AC30, AC32, AC34, AD15, AD17, AD19, AD21, AD23, AD27, AD31, AE14, AE18, AE26, AE28, AE30, AE32, AE34, AF15, AF17, AF19, AF21, AF23, AF25, AF27, AF29, AF31, AF33, AG14, AG16, AG18, AG20, AG24, AG26, AG28, AG32, AG34, AH15, AH17, AH19, AH21, AH23, AH25, AH27, AH29, AH31, AH33, AJ14, AJ16, AJ18, AJ20, AJ26, AJ28, AJ32, AJ34, AK15, AK17, AK19, AK21, AK23, AK25, AK27, AK29, AK31, AK33, AL14, AL16, AL20, AL24, AL26, AL28, AL34, AM15, AM17, AM19, AM21, AM23, AM27, AM29, AM31, AM33, AN14, AN16, AN18, AN20, AN22, AN26, AN28, AN30, AN32, AN34, AP15, AP17, AP21, AP23, AP29, AP31, AP33, AR14, AR16, AR18, AR20, AR22, AR24, AR26, AR28, AR30, AR32, AR34, AT15, AT17, AT21, AT23, AT25, AT29, AT31, AT33, AU14, AU16, AU18, AU20, AU22, AU26, AU28, AU30, AU32, AU34
VIO_1P10	VIO	K13, K15, K17, K19, K21, K23, K25, K27, K29, K31, K33, K35, L14, L16, L18, L20, L22, L24, L26, L28, L30, L32, L34, L36, M13, M25, M35, P13, P24, P35, T13, T25, T35, U36, V13, V24, V36, W35, Y13, Y25, Y36, AA35, AB24, AB36, AC35, AD13, AD14, AD18, AD22, AD25, AD29, AD33, AD36, AE16, AE20, AE24, AE27, AE31, AE35, AF36, AG25, AG35, AH13, AH36, AJ24, AJ35, AK13, AK36, AL25, AL35, AM13, AM36, AN24, AN35, AP13, AR25, AR35, AT13, AU24, AU35, AV13, AV15, AV17, AV19, AV21, AV23, AV25, AV27, AV29, AW14, AW16, AW18, AW20, AW22, AW24, AW28, AW30, AW35
VPCI_1P20	VPCI	L35, M36, N35, P36, R35, T36, AN36, AP35, AR36, AT35, AU36, AV35
VSB_1P20	VSB	AV31, AV33
VSB_3P30	VSB	AJ08, AJ09

5.2.2 PLL and Reference Clock Signals

Table 5-4 lists the PLL signals.

Table 5-4. PLL Signals

Signal	Pins	Description	Category	Family	Type	Board Pull-up/ Pull-down?	Rail for Pull-up/ Pull-down?	Industry Standard Compliant?	3.3 V Tolerant?
TS_CT_P_PIN_PXFM_PLL_ANATST	AP10	PLL analog test[1]	PLL/Clock	Analog	AnlgOut				
TS_CT_P_PIN_PXFM_PLL_HFC_P/N	AK10, AK09	PLL high-frequeny characterization[1]	PLL/Clock	CMOS	Drv				
TS_CT_P_PIN_M0_PLL_ANATST	J17	Memory 0 PLL analog test[1]	PLL/Clock	Analog	AnlgOut				
TS_CT_P_PIN_M1_PLL_ANATST	AY18	Memory 1 PLL analog test[1]	PLL/Clock	Analog	AnlgOut				
TS_CT_P_PIN_A_PLL_ANATST	T37	PLL analog test[1]	PLL/Clock	Analog	AnlgOut				
TS_CT_P_PIN_PE0_PLL_ANATST	P37	PCIe PLL analog test[2]	PLL/Clock	Analog	AnlgOut	No	N/A		
TS_CT_P_PIN_PE1_PLL_ANATST	AR37		PLL/Clock	Analog	AnlgOut	No	N/A		

1. Unused in OpenPOWER designs. No connect.
2. No connect.

Table 5-5 lists the reference clock signals.

Table 5-5. Reference Clocks

Signal	Pins	Description	Category	Family	Type	Board Pull-up/ Pull-down?	Rail for Pull-up/ Pull-down?	Industry Standard Compliant?	3.3 V Tolerant?
PV_PIN_P_CT_OSC0_C1_REFCLK_P/N	T11, T12	System Reference Clock [1]	PLL/Clock	CMOS	RecDiff				

1. No termination on chip. The clocking solution must include termination.

5.2.3 Test Signals

Table 5-6 lists the mini-kerf test signals.

Table 5-6. I/O Minikerf Test Signals

Signal	Pins	Description	Category	Family	Type	Board Pull-up/ Pull-down?	Rail for Pull-up/ Pull-down?	Industry Standard Compliant?	3.3 V Tolerant?
TS_CT_P_PIN_A1_MKERF_P/N	AK38, AJ38	I/O PHY test point[1]	Test	Analog	Anlgout	No			
TS_CT_P_PIN_M0_C_MKERF_P/N	H25, J25	I/O PHY test point[1]	Test	Analog	Anlgout	No			
TS_CT_P_PIN_M0_T_PLLHFC_MKERF_ P/N	J18, H18	I/O PHY test point[1]	Test	Analog	Anlgout	No			
TS_CT_P_PIN_A_PLLHFC_MKERF_P/N	R38, P38	I/O PHY test point[1]	Test	Analog	Anlgout	No			

1. No connect.

Table 5-7 lists additional test signals.

Table 5-7. Test Signals

Signal	Pins	Description	Category	Family	Type	Board Pull-up/ Pull-down?	Rail for Pull-up/ Pull-down?	Industry Standard Compliant?	3.3 V Tolerant?
TS_PIN_P_CT_TEST_LSSD_TE	BC26	LSSD test mode[1]	Pervasive	CMOS	Rec	Pull-down 50 Ω ±5%	GND	N/A	N/A
TS_PIN_P_CT_TST_FORCE_PWR_ON	AR11	Test force power-on[1]	Pervasive	CMOS	Rec	Pull-down 50 Ω ±5%	GND	N/A	N/A
TS_CT_P_PIN_VCAL	AC24	Used to calibrate the iVRM output transistor strength during wafer test.	Pervasive	Analog	AnlgOut		N/A	N/A	N/A
TS_PIN_P_CT_STBY_RESET_B	BC28	Standby reset for FSI. Active during the power-on process. Requires pull-up.[3]	Pervasive	CMOS	Rec	Pull-up 10 kΩ ±5%	1.2 V AUX	N/A	N/A
TS_CT_P_PIN_PROBE0_P/N	AY29, AY30	Probe Out 0 differential high/differential low	Pervasive	CMOS	DrvDiff				
TS_CT_P_PIN_PROBE1_P/N	J08, H08	Probe Out 1 differential high/differential low	Pervasive	CMOS	DrvDiff				
TS_CT_P_PIN_PROBE2	AY16	Probe Out 2	Pervasive	CMOS	Drv				
TS_CT_P_PIN_PROBE3	AY20	Probe Out 3	Pervasive	CMOS	Drv				
TS_CT_P_PIN_PROBE4	AY17	Probe Out 4	Pervasive	CMOS	Drv				
TS_PIN_P_CT_EFUSE_FSOURCE	AP25	eFuse V_{DD}[3]	Pervasive	Analog	Power	Pull-down 50 Ω ±5%	GND		
PV_CT_P_PIN_SPARE0	AY21	Spare 0[4]	Pervasive	CMOS	Drv	Pull-up 50 Ω ±5%	1.1 V		

1. Not used at the board or system level.
2. A 1 - 10 nF capacitor is recommended for noise dampering.
3. Not for use in a system; might be used at manufacturing test.
4. Signal can be left floating.

5.2.4 Control Signals

Table 5-8 lists the control signals.

Table 5-8. Control Signals

Signal	Pins	Description	Category	Family	Type	Board Pull-up/ Pull-down?	Rail for Pull-up/ Pull-down?	Industry Standard Compliant?	3.3 V Tolerant?
PV_CT_P_PIN_ATTENTION_B	BB28	Attention[1]	Pervasive	CMOS	Drv	Pull-up 4.7 KΩ	3.3 V AUX	N/A	Yes, up to 3.65 V
PV_PIN_P_CT_CHIP_ID0	BF30	Chip ID[2]	Pervasive	CMOS	Rec	50 Ω ±5%[3]	1.2 V AUX/GND		No
PV_PIN_P_CT_CHIP_ID1	BD30	Chip ID[2]	Pervasive	CMOS	Rec	50 Ω ±5%[3]	1.2 V AUX/GND		No
PV_PIN_P_CT_FSI_IN_ENA1	BC29	Enable incoming FSI clock[4, 5]	Pervasive	CMOS	Rec	Pull-up 1.2 KΩ	1.2 V AUX		No
PV_PIN_P_CT_VIO_PGOOD	AW26	V_{IO} power good[6]	Pervasive	CMOS	Rec	Pull-up[7] 1.2 KΩ	1.2 V AUX	N/A	No
PV_CT_P_PIN_TPM_RESET	AT10	TPM reset[1, 8]	Pervasive	OD	BiDi	Pull-down 10 KΩ	GND	No	No
PV_PIN_P_CT_TPM_INTERRUPT	AR10	TPM interrupt[9]	Pervasive	OD	Rec	Pull-up 1 KΩ ±5%	1.1 V	No	No

1. See the IBM reference design in OpenPOWER Connect for implementation details.
2. Use to configure MFSI slave network.
3. See the IBM 2-socket reference design in OpenPOWER Connect for implementation details.
4. An active signal that has an internal 10 KΩ pull-down. It requires a 1.2 KΩ pull-up to override.
5. This signal determines the source of the FSI clock, either internal or external. The signal must be asserted (driven high) by the BMC when the BMC is driving the FSI bus (for example. during the boot sequence to the POWER8 processor) and when the FSP2 debug box is being used.
6. Critical for boot/operation; use extra capacitance to GND for noise.
7. No pull-up is required if there is always an active driver on this signal. This signal should never be left floating.
8. System-dependent level shifting is required.
9. The actual pullup value might vary depending on the system implementation.

5.2.5 LPC Bus Signals

Table 5-9 lists the LPC bus signals.

Table 5-9. LPC Bus Signals

Signal	Pins	Description	Category	Family	Type	Board Pull-up/ Pull-down?	Rail for Pull-up/ Pull-down?	Industry Standard Compliant?	3.3 V Tolerant?
PV_CT_B_PIN_LPC_DATA_[00:03]	AY33, AW32, AY32, AW31	LPC Data. P/N of level shifter.[1]	Pervasive	CMOS	BiDi			No	No
PV_CT_P_PIN_LPC_FRAME_B	AW33	LPC Frame[1]	Pervasive	CMOS	Drv			No	No
PV_PIN_P_CT_LPC_RESET_B	AW34	LPC Reset[1]	Pervasive	CMOS	BIDI			No	No
PV_PIN_P_CT_LPC_CLK	AW36	LPC Clock[2]	Pervasive	CMOS	Rec			No	No

1. See the IBM reference design in OpenPOWER Connect for implementation details.
2. See the IBM reference design in OpenPOWER Connect for implementation details. V_{MAX} = 1.2 V for this pin.

5.2.6 FSI Signals

Table 5-10 lists the FSI signals.

Table 5-10. FSI Signals (Sheet 1 of 2)

Signal	Pins	Description	Category	Family	Type	Board Pull-up/ Pull-down?	Rail for Pull-up/ Pull-down?	Industry Standard Compliant?	3.3 V Tolerant?
PV_PIN_P_CT_FSP0_FSI_CLK	BE29	FSI0 Clock	FSI	CMOS	Rec	No			No
PV_PIN_B_CT_FSP0_FSI_DATA	BE28	FSI0 Data	FSI	CMOS	BiDi	No			No
SH_PIN_P_CT_FSP1_FSI_CLK	BA40	FSI1 Clock	FSI	CMOS	Rec	Pull-down 50 Ω ±5%	GND		No
SH_CT_P_PIN_MB_FSI0_CLK	BC42	FSI Master 0 Clock[1]	FSI	CMOS	Drv	No			No
SH_CT_B_PIN_MB_FSI0_DATA	BB41	FSI Master 0 Data[1]	FSI	CMOS	BiDi	No			No
SH_CT_P_PIN_MB_FSI1_CLK	AW38	FSI Master 1 Clock[1]	FSI	CMOS	Drv	No			No
SH_CT_B_PIN_MB_FSI1_DATA	AY39	FSI Master 1 Data[1]	FSI	CMOS	BiDi	No			No
MM_CT_P_PIN_MB_FSI2_CLK	BA25	FSI Master 2 Clock	FSI	CMOS	Drv				No
MM_CT_B_PIN_MB_FSI2_DATA	BA24	FSI Master 2 Data	FSI	CMOS	BiDi	750 Ω pull-up[2]	1.2 V AUX		No
MM_CT_P_PIN_MB_FSI3_CLK	AY23	FSI Master 3 Clock	FSI	CMOS	Drv				No
MM_CT_B_PIN_MB_FSI3_DATA	AT24	FSI Master 3 Data	FSI	CMOS	BiDi	750 Ω pull-up[2]	1.2 V AUX		No
MM_CT_P_PIN_MB_FSI6_CLK	BB22	FSI Master 6 Clock	FSI	CMOS	Drv				No
MM_CT_B_PIN_MB_FSI6_DATA	BB23	FSI Master 6 Data	FSI	CMOS	BiDi	750 Ω pull-up[2]	1.2 V AUX		No
MM_CT_P_PIN_MB_FSI7_CLK	BA22	FSI Master 7 Clock	FSI	CMOS	Drv				No
MM_CT_B_PIN_MB_FSI7_DATA	BA21	FSI Master 7 Data	FSI	CMOS	BiDi	750 Ω pull-up[2]	1.2 V AUX		No
PV_CT_P_PIN_FSI1_CLK	BB25	FSI Master CP Clock[3]	FSI	CMOS	Drv	No			No
PV_CT_B_PIN_FSI1_DATA	BB26	FSI Master CP Data[3]	FSI	CMOS	BiDi	No			No
PV_CT_P_PIN_FSI2_CLK	BC24	FSI Master CP Clock[3]	FSI	CMOS	Drv	No			No

1. No connect.
2. The pull-up is on the POWER8 memory buffer side of the net. If the POWER8 memory buffer is on a DIMM card, no additional pull-ups are required on the processor planar.
3. See the IBM 2-socket reference design in OpenPOWER Connect for implementation details.

Table 5-10. FSI Signals (Sheet 2 of 2)

Signal	Pins	Description	Category	Family	Type	Board Pull-up/ Pull-down?	Rail for Pull-up/ Pull-down?	Industry Standard Compliant?	3.3 V Tolerant?
PV_CT_B_PIN_FSI2_DATA	BC23	FSI Master CP Data[3]	FSI	CMOS	BiDi	No			No
PV_CT_P_PIN_FSI3_CLK	BD24	FSI Master CP Clock[3]	FSI	CMOS	Drv	No			No
PV_CT_B_PIN_FSI3_DATA	BD25	FSI Master CP Data[3]	FSI	CMOS	BiDi	No			No
PV_PIN_P_CT_FSI_SMD	BF29	FSI Secure Mode Disable[3]	Pervasive	CMOS	Rec	Pull-up 50 Ω ±5%	1.2 V AUX		No

1. No connect.
2. The pull-up is on the POWER8 memory buffer side of the net. If the POWER8 memory buffer is on a DIMM card, no additional pull-ups are required on the processor planar.
3. See the IBM 2-socket reference design in OpenPOWER Connect for implementation details.

IBM

5.2.7 SPI Signals

Table 5-11 lists the SPI signals. See the IBM reference design examples in <u>OpenPOWER Connect</u> and the <u>*POWER8 Systems Power Design and Validation Guide*</u> for implementation details.

Table 5-11. SPI Signals

Signal	Pins	Description	Category	Family	Type	Board Pull-up/ Pull-down?	Rail for Pull-up/ Pull-down?	Industry Standard Compliant?	3.3 V Tolerant?
PV_CT_P_PIN_SPIVID0_MOSI	H29	SPI VIDs (to VRM0)	SPI	CMOS	Drv	No			No
PV_PIN_P_CT_SPIVID0_MISO	J30	SPI VIDs (to VRM0)	SPI	CMOS	Rec	No			No
PV_CT_P_PIN_SPIVID0_SCLK	H28	SPI VIDs (to VRM0)	SPI	CMOS	Drv	No			No
PV_CT_P_PIN_SPIVID0_CS	J28	SPI VIDs (to VRM0)	SPI	CMOS	Drv	No			No
PV_CT_P_PIN_SPIADC_MOSI	Y37	SPISS MOSI	SPI	CMOS	Drv	No			No
PV_PIN_P_CT_SPIADC_MISO	V37	SPISS MISO	SPI	CMOS	Rec	No			No
PV_CT_P_PIN_SPIADC_SCLK	AA39	SPISS SCLK	SPI	CMOS	Drv	No			No
PV_CT_P_PIN_SPIADC_CS0	AA38	SPISS CS0	SPI	CMOS	Drv	No			No
PV_CT_P_PIN_SPIADC_CS1	AA37	SPISS CS1	SPI	CMOS	Drv	No			No

5.2.8 I^{2}C Signals

Table 5-12 lists the I^{2}C signals. See the IBM reference design examples in [OpenPOWER Connect](#) for implementation details.

Table 5-12. I^{2}C Signals

Signal	Pins	Description	Category	Family	Type	Board Pull-up/ Pull-down?	Rail for Pull-up/ Pull-down?	Industry Standard Compliant?	3.3 V Tolerant?
PV_PIN_B_CT_I2CSL_SCL	BA27	I^{2}C Slave Clock[1]	I^{2}C	OD	BiDi		3.3 V AUX	Yes	Yes
PV_PIN_B_CT_I2CSL_SDA	BA28	I^{2}C Slave Data[1]	I^{2}C	OD	BiDi		3.3 V AUX	Yes	Yes
PV_CT_M_PIN_SEEPROM0_CLK	AY08	SEEPROM Clock[2]	I^{2}C	OD	Drv	Pull-up 1.5 KΩ	3.3 V AUX	Yes	Yes
PV_CT_M_PIN_SEEPROM0_DATA	BA08	SEEPROM Data[2]	I^{2}C	OD	BiDi	Pull-up 1.5 KΩ	3.3 V AUX	Yes	Yes
PV_CT_M_PIN_SEEPROM1_CLK	N10	SEEPROM Clock[2]	I^{2}C	OD	Drv	Pull-up 1.5 KΩ	3.3 V AUX	Yes	Yes
PV_CT_M_PIN_SEEPROM1_DATA	P10	SEEPROM Data[2]	I^{2}C	OD	BiDi	Pull-up 1.5 KΩ	3.3 V AUX	Yes	Yes
PV_CT_B_PIN_LP_I2C_SCL_B	AY26	I^{2}C Master Data Lightpath	I^{2}C	OD	BiDi	See note 3	3.3 V AUX	Yes	Yes
PV_CT_B_PIN_LP_I2C_SDA_B	AY27	I^{2}C Master Clock Lightpath	I^{2}C	OD	BiDi	See note 3	3.3 V AUX	Yes	Yes
PV_CT_B_PIN_PCI_I2C_SCL_B	AM37	I^{2}C Master Data PCIe E1	I^{2}C	OD	BiDi	See note 3	3.3 V AUX	Yes	Yes
PV_CT_B_PIN_PCI_I2C_SDA_B	AL37	I^{2}C Master Data PCIe E1	I^{2}C	OD	BiDi	See note 3	3.3 V AUX	Yes	Yes

1. Alternate path into the chip FSI; connect to the BMC. See the IBM reference design examples in [OpenPOWER Connect](#) for implementation details.
2. Module VPD.
3. If the bus is unused, pull-down to GND through a 50 Ω resistor. If used, the total value of parallel resistance on each net must be greater than 1.2 KΩ including the tolerance.

5.2.9 Time-of-Day Signal

Table 5-13 lists the time-of-day (TOD) signal.

Table 5-13. Time-of-Day and Bus Synchronization Signal

Signal	Pins	Description	Category	Family	Type	Board Pull-up/ Pull-down?	Rail for Pull-up/ Pull-down?	Industry Standard Compliant?	3.3 V Tolerant?
PV_PIN_P_CT_OSC0_TODREFCLK	V10	TOD Reference Clock[1]	CLK	CMOS	Rec	No	No	N/A	No

1. See the IBM reference design in OpenPOWER Connect for implementation details. Signal pin V_{MAX} = 1.2 V.

5.2.10 Thermal Diode and Monitor Signals

Table 5-14 lists the thermal diode and monitor signals. See the IBM reference design examples in OpenPOWER Connect for implementation details.

Table 5-14. Thermal Diodes and Monitor Signals (Sheet 1 of 3)

Signal	Pins	Description	Category	Family	Type	Board Pull-up/ Pull-down?	Rail for Pull-up/ Pull-down?	Industry Standard Compliant?	3.3 V Tolerant?
TS_CT_P_PIN_TDIODE_A5	AL18	Core Thermal Diode Anode[1]	Thermal	Analog	AnlgOut	No			
TS_CT_P_PIN_TDIODE_C5	AL17	Core Thermal Diode Cathode[1]	Thermal	Analog	AnlgOut	No			
TS_CT_P_PIN_TDIODE_A13	AL31	Core Thermal Diode Anode[1]	Thermal	Analog	AnlgOut	No			
TS_CT_P_PIN_TDIODE_C13	AL32	Core Thermal Diode Cathode[1]	Thermal	Analog	AnlgOut	No			
TS_CT_P_PIN_DTS2_MONI	N18	Digital Thermal Sensor Monitor[2]	Thermal	Analog	AnlgOut	No	N/A	N/A	No
TS_CT_P_PIN_AMX0_VSENSE	G27	West Analog Muxed Sense[3]	Vsense	Analog	AnlgOut	No	N/A	N/A	No

1. IBM recommends that this signal be no connect (N/C) for OpenPOWER products. Accurate processor temperature readings are available from the OCC via the processor I^2C bus.
2. No connect.
3. Voltage sense signals are used only for characterization and debug.

Table 5-14. Thermal Diodes and Monitor Signals (Sheet 2 of 3)

Signal	Pins	Description	Category	Family	Type	Board Pull-up/ Pull-down?	Rail for Pull-up/ Pull-down?	Industry Standard Compliant?	3.3 V Tolerant?
TS_CT_P_PIN_AMX0_GSENSE	F27	West Analog Muxed Ground Sense[3]	Vsense	Analog	AnlgOut	No	N/A	N/A	No
TS_CT_P_PIN_AMX1_VSENSE	AN25	West Analog Muxed Sense[3]	Vsense	Analog	AnlgOut	No	N/A	N/A	No
TS_CT_P_PIN_AMX1_GSENSE	AM25	West Analog Muxed Ground Sense[3]	Vsense	Analog	AnlgOut	No	N/A	N/A	No
TS_CT_P_PIN_GDDCORE0_GSENSE	T14	Chiplet Core Logic Ground Sense[3]	Vsense	Analog	AnlgOut				
TS_CT_P_PIN_VDDCORE0_VSENSE	R14	Chiplet Core Logic Sense[3]	Vsense	Analog	AnlgOut				
TS_CT_P_PIN_GDSCORE0_GSENSE	N20	Chiplet Core SRAM Ground Sense[3]	Vsense	Analog	AnlgOut				
TS_CT_P_PIN_VCSCORE0_VSENSE	M20	Chiplet Core SRAM Sense[3]	Vsense	Analog	AnlgOut				
TS_CT_P_PIN_GDECO0_GSENSE	M24	Chiplet ECO Logic Ground Sense[3]	Vsense	Analog	AnlgOut				
TS_CT_P_PIN_VDDECO0_VSENSE	N23	Chiplet ECO Logic Sense[3]	Vsense	Analog	AnlgOut				
TS_CT_P_PIN_VCSECO0_VSENSE	N24	Chiplet ECO SRAM Sense[3]	Vsense	Analog	AnlgOut				
TS_CT_P_PIN_VDDEX0_VSENSE	U24	EX VDD Logic Voltage Sense[3]	Vsense	Analog	AnlgOut				
TS_CT_P_PIN_EX0_GSENSE	T24	EX VCS Ground Sense[3]	Vsense	Analog	AnlgOut				
TS_CT_P_PIN_VCSEX0_VSENSE	U23	EX VCS Logic Voltage Sense[3]	Vsense	Analog	AnlgOut				
TS_CT_P_PIN_VIO_VSENSE	J37	VIO Logic Voltage Sense[3]	Vsense	Analog	AnlgOut				
TS_CT_P_PIN_VIO_VPCI_GSENSE	K37	VIO VPCI Ground Sense[3]	Vsense	Analog	AnlgOut				

1. IBM recommends that this signal be no connect (N/C) for OpenPOWER products. Accurate processor temperature readings are available from the OCC via the processor I^2C bus.
2. No connect.
3. Voltage sense signals are used only for characterization and debug.

Table 5-14. Thermal Diodes and Monitor Signals (Sheet 3 of 3)

Signal	Pins	Description	Category	Family	Type	Board Pull-up/ Pull-down?	Rail for Pull-up/ Pull-down?	Industry Standard Compliant?	3.3 V Tolerant?
TS_CT_P_PIN_VPCI0_VSENSE	L37	VPCI Voltage Sense[3]	Vsense	Analog	AnlgOut				
TS_CT_P_PIN_PFAMX_VSENSE	AB25	PFET Analog Muxed Sense[3]	Vsense	Analog	AnlgOut				
TS_CT_P_PIN_PFAMX_GSENSE	AC25	PFET Analog Muxed Ground Sense[3]	Vsense	Analog	AnlgOut				
PV_MSOP_M_CT_VREF_P/N	AC09, AC08	Internal chip reference pins[2]	Pervasive	Analog	AnlgOut	No	N/A	No	N/A
VCS_SENSE_P	AG22	VCS Voltage Sense for the Voltage Regulators[3]	Vsense	Analog	AnlgOut	No-popped 100 Ω pull-up	V_{CS}		
VCS_SENSE_N	AG23	VCS Voltage Sense for the Voltage Regulators[3]	Vsense	Analog	AnlgOut	No-popped 100 Ω pull-down	GND		
VDD_SENSE_P	AE22	VDD Voltage Sense for the Voltage Regulators[3]	Vsense	Analog	AnlgOut	No-popped 100 Ω pull-up	V_{DD}		
VDD_SENSE_N	AE23	VDD Voltage Sense for the Voltage Regulators[3]	Vsense	Analog	AnlgOut	No-popped 100 Ω pull-down	GND		

1. IBM recommends that this signal be no connect (N/C) for OpenPOWER products. Accurate processor temperature readings are available from the OCC via the processor I^{2}C bus.
2. No connect.
3. Voltage sense signals are used only for characterization and debug.

5.2.11 DMI Signals

Table 5-15 lists the DMI signals.

Table 5-15. DMI Signals (Sheet 1 of 6)

Signal	Pins	Description	Category	Family	Type	Board Pull-up/ Pull-down?	Rail for Pull-up/ Pull-down?	Industry Standard Compliant?	3.3 V Tolerant?
PV_PIN_P_CT_M0_TERMREF_P/N	J20, J21	Memory Termination Reference[1]	DMI	Analog	AnlgIn	No			
MM_M0_P_PIN_CKC_CLK_P/N	G03, F03	Memory Channel Downstream Forwarded Clock	Data	EDI	DrvDiff				
MM_M0_P_PIN_CKC_DAT_[00:16]_P	N07, L07, M06, K06, L05, J05, K04, H04, H03, D01, E02, F01, G02, N04, J01, K02, L03	Memory Channel Downstream	Data	EDI	DrvDiff				
MM_M0_P_PIN_CKC_DAT_[00:16]_N	M07, K07, L06, J06, K05, H05, J04, G04, J03, E01, F02, G01, H02, M04, K01, L02, M03	Memory Channel Downstream	Data	EDI	DrvDiff				
MM_PIN_P_M0_CKC_CLK_P/N	A22, A23	Memory Channel Upstream Forwarded Clock	Data	EDI	RecDiff				
MM_PIN_P_M0_CKC_DAT_[00:23]_P	C15, D16, A14, B16, C17, A17, B18, G17, F18, A19, B21, C20, B23, C22, D19, A24, B27, C26, D22, A28, E19, E21, F19, G18	Memory Channel Upstream	Data	EDI	RecDiff				

1. Do not connect to any voltages or signals. Connect the P/N signals with a 169 Ω, 1% 0402 resistor.
2. Chip internally has a 1 KΩ pull-up.

Table 5-15. DMI Signals (Sheet 2 of 6)

Signal	Pins	Description	Category	Family	Type	Board Pull-up/ Pull-down?	Rail for Pull-up/ Pull-down?	Industry Standard Compliant?	3.3 V Tolerant?
MM_PIN_P_M0_CKC_DAT_[00:23]_N	C16, D17, A15, B17, C18, A18, B19, G16, F17, A20, B22, C21, B24, C23, D20, A25, B26, C25, D21, A27, E18, E20, F20, G19	Memory Channel Upstream	Data	EDI	RecDiff				
MM_M0_P_PIN_CKD_CLK_P/N	V04, U04	Memory Channel Downstream Forwarded Clock	Data	EDI	DrvDiff				
MM_M0_P_PIN_CKD_DAT_[00:16]_P	T09, R08, U08, T07, W07, V06, R06, V01, T05, T03, P01, R04, R02, P03, N02, N05, M01	Memory Channel Downstream	Data	EDI	DrvDiff				
MM_M0_P_PIN_CKD_DAT_[00:16]_N	R09, P08, T08, R07, V07, U06, P06, U01, U05, U03, R01, T04, T02, R03, P02, P05, N01	Memory Channel Downstream	Data	EDI	DrvDiff				
MM_PIN_P_M0_CKD_CLK_P	B06	Memory Channel Upstream Forwarded Clock	Data	EDI	RecDiff				
MM_PIN_P_M0_CKD_CLK_N	B07	Memory Channel Upstream Forwarded Clock	Data	EDI	RecDiff				
MM_PIN_P_M0_CKD_DAT_[00:23]_P	H10, G10, G11, F08, F10, E07, E09, D06, C06, B04, A05, C07, D08, A08, C10, B09, D11, A11, B12, C13, E12, D14, F13, E14	Memory Channel Upstream	Data	EDI	RecDiff				

1. Do not connect to any voltages or signals. Connect the P/N signals with a 169 Ω, 1% 0402 resistor.
2. Chip internally has a 1 KΩ pull-up.

Table 5-15. DMI Signals (Sheet 3 of 6)

Signal	Pins	Description	Category	Family	Type	Board Pull-up/ Pull-down?	Rail for Pull-up/ Pull-down?	Industry Standard Compliant?	3.3 V Tolerant?
MM_PIN_P_M0_CKD_DAT_[00:23]_N	H11, G09, G12, F09, F11, E08, E10, D07, C05, B05, A06, C08, D09, A09, C11, B10, D12, A10, B11, C12, E13, D13, F14, E15	Memory Channel Upstream	Data	EDI	RecDiff				
MM_PIN_P_CT_M1_FAULT_C_N	AL09	Memory Fault Channel [2]	Data	CMOS	Rec	No			No
MM_PIN_P_CT_M1_FAULT_D_N	AM10		Data	CMOS	Rec	No			No
PV_PIN_P_CT_M1_TERMREF_P/N	BA17, BA18	Memory Termination Reference[1]	DMI	Analog	AnlgIn	No			
MM_M1_P_PIN_CKC_CLK_P/N	BB03, BC03	Memory Channel Downstream Forwarded Clock	Data	EDI	DrvDiff				
MM_M1_P_PIN_CKC_DAT_[00:16]_P	AT07, AV07, AU06, AW06, AV05, AY05, AW04, BA04, BA03, BE01, BD02, BC01, BB02, AT04, AY01, AW02, AV03	Memory Channel Downstream	Data	EDI	DrvDiff				
MM_M1_P_PIN_CKC_DAT_[00:16]_N	AU07, AW07, AV06, AY06, AW05, BA05, AY04, BB04, AY03, BD01, BC02, BB01, BA02, AU04, AW01, AV02, AU03	Memory Channel Downstream	Data	EDI	DrvDiff				
MM_PIN_P_M1_CKC_CLK_P/N	BH22, BH23	Memory Channel Upstream Forwarded Clock	Data	EDI	RecDiff				

1. Do not connect to any voltages or signals. Connect the P/N signals with a 169 Ω, 1% 0402 resistor.
2. Chip internally has a 1 KΩ pull-up.

Table 5-15. DMI Signals (Sheet 4 of 6)

Signal	Pins	Description	Category	Family	Type	Board Pull-up/ Pull-down?	Rail for Pull-up/ Pull-down?	Industry Standard Compliant?	3.3 V Tolerant?
MM_PIN_P_M1_CKC_DAT_[00:23]_P	BF15, BE16, BH14, BG16, BF17, BH17, BG18, BB17, BC18, BH19, BG21, BF20, BG23, BF22, BE19, BH24, BG27, BF26, BE22, BH28, BD19, BD21, BC19, BB18	Memory Channel Upstream	Data	EDI	RecDiff				
MM_PIN_P_M1_CKC_DAT_[00:23]_N	BF16, BE17, BH15, BG17, BF18, BH18, BG19, BB16, BC17, BH20, BG22, BF21, BG24, BF23, BE20, BH25, BG26, BF25, BE21, BH27, BD18, BD20, BC20, BB19	Memory Channel Upstream	Data	EDI	RecDiff				
MM_M1_P_PIN_CKD_CLK_P/N	AL04, AM04	Memory Channel Downstream Forwarded Clock	Data	EDI	DrvDiff				
MM_M1_P_PIN_CKD_DAT_[00:16]_P	AN09, AP08, AM08, AN07, AK07, AL06, AP06, AL01, AN05, AN03, AR01, AP04, AP02, AR03, AT02, AT05, AU01	Memory Channel Downstream	Data	EDI	DrvDiff				

1. Do not connect to any voltages or signals. Connect the P/N signals with a 169 Ω, 1% 0402 resistor.
2. Chip internally has a 1 KΩ pull-up.

Table 5-15. DMI Signals (Sheet 5 of 6)

Signal	Pins	Description	Category	Family	Type	Board Pull-up/ Pull-down?	Rail for Pull-up/ Pull-down?	Industry Standard Compliant?	3.3 V Tolerant?
MM_M1_P_PIN_CKD_DAT_[00:16]_N	AP09, AR08, AN08, AP07, AL07, AM06, AR06, AM01, AM05, AM03, AP01, AN04, AN02, AP03, AR02, AR05, AT01	Memory Channel Downstream	Data	EDI	DrvDiff				
MM_PIN_P_M1_CKD_CLK_P/N	BG06, BG07	Memory Channel Upstream Forwarded Clock	Data	EDI	RecDiff				
MM_PIN_P_M1_CKD_DAT_[00:23]_P	BA10, BB10, BB11, BC08, BC10, BD07, BD09, BE06, BF06, BG04, BH05, BF07, BE08, BH08, BF10, BG09, BE11, BH11, BG12, BF13, BD12, BE14, BC13, BD14	Memory Channel Upstream	Data	EDI	RecDiff				
MM_PIN_P_M1_CKD_DAT_[00:23]_N	BA11, BB09, BB12, BC09, BC11, BD08, BD10, BE07, BF05, BG05, BH06, BF08, BE09, BH09, BF11, BG10, BE12, BH10, BG11, BF12, BD13, BE13, BC14, BD15	Memory Channel Upstream	Data	EDI	RecDiff				

1. Do not connect to any voltages or signals. Connect the P/N signals with a 169 Ω, 1% 0402 resistor.
2. Chip internally has a 1 KΩ pull-up.

Table 5-15. DMI Signals (Sheet 6 of 6)

Signal	Pins	Description	Category	Family	Type	Board Pull-up/ Pull-down?	Rail for Pull-up/ Pull-down?	Industry Standard Compliant?	3.3 V Tolerant?
SH_PIN_P_M1_CKB_DAT_01_P SH_PIN_P_M1_CKB_DAT_03_P SH_PIN_P_M1_CKB_DAT_[06:08]_P SH_PIN_P_M1_CKB_DAT_[10:23]_P	AY15, AW12, BB06, BD04, BF03, AY13, BD05, AY09, BB07, AY12, BA07, BE04, BG14, BC05, BF02, BE03, BH03, BG02, BG01	Memory Channel Upstream	Data	EDI	RecDiff				
MM_CT_P_PIN_MB_NEST_REFCLK2_P MM_CT_P_PIN_MB_NEST_REFCLK2_N MM_CT_P_PIN_MB_NEST_REFCLK3_P MM_CT_P_PIN_MB_NEST_REFCLK3_N MM_CT_P_PIN_MB_NEST_REFCLK6_P MM_CT_P_PIN_MB_NEST_REFCLK6_N MM_CT_P_PIN_MB_NEST_REFCLK7_P MM_CT_P_PIN_MB_NEST_REFCLK7_N	M09 L09 K10 L10 AV09 AU09 AW10 AV10	POWER8 Memory Buffer Nest Clock	CLK	CMOS	Drv				
MM_CT_P_PIN_MB_MEM_REFCLK2_P MM_CT_P_PIN_MB_MEM_REFCLK2_N MM_CT_P_PIN_MB_MEM_REFCLK3_P MM_CT_P_PIN_MB_MEM_REFCLK3_N MM_CT_P_PIN_MB_MEM_REFCLK6_P MM_CT_P_PIN_MB_MEM_REFCLK6_N MM_CT_P_PIN_MB_MEM_REFCLK7_P MM_CT_P_PIN_MB_MEM_REFCLK7_N	L11 M11 L12 K12 AV11 AU11 AT12 AU12	POWER8 Memory Buffer Memory Clock	CLK	CMOS	Drv				
MM_PIN_P_CT_M0_FAULT_C_N MM_PIN_P_CT_M0_FAULT_D_N	V09, P11	Memory Fault Channel	Data	CMOS	Rec				

1. Do not connect to any voltages or signals. Connect the P/N signals with a 169 Ω, 1% 0402 resistor.
2. Chip internally has a 1 KΩ pull-up.

5.2.12 A Bus Signals

Table 5-16 lists the A bus signals.

Table 5-16. A Bus Signals (Sheet 1 of 4)

Signal	Pins	Description	Category	Family	Type	Board Pull-up/ Pull-down?	Rail for Pull-up/ Pull-down?	Industry Standard Compliant?	3.3 V Tolerant?
NA_PIN_P_A0_CK0_CLK_P/N	AK46, AJ46	Clock Input	Data	EDI	RecDiff				
NA_PIN_P_A0_CK0_DAT_[00:22]_P	AJ43, AF43, AL43, AH44, AG45, AJ45, AF47, AH46, AL44, AJ47, AG48, AK48, AL47, AM45, AM48, AN44, AP47, AR48, AN46, AT47, AR46, AU48, AP45	16-Bit Pack Data Input [00:22]	Data	EDI	Rec				
NA_PIN_P_A0_CK0_DAT_[00:22]_N	AK43, AG43, AM43, AG44, AF45, AH45, AE47, AG46, AK44, AH47, AF48, AJ48, AK47, AL45, AL48, AM44, AN47, AP48, AM46, AR47, AP46, AT48, AN45	16-Bit Pack Data Input [00:22]	Data	EDI	Rec				
NA_A0_P_PIN_CK0_CLK_P/N	H48, G48	Clock Output	Data	EDI	DrvDiff				
NA_A0_P_PIN_CK0_DAT_[00:22]_P	D44, C44, B45, A47, E45, B48, G44, D47, E46, E48, F47, G46, H45, J47, H43, K48, L47, K46, N48, M46, J44, N45, K45	16-Bit Pack Data Output [00:22]	Data	EDI	Drv				

1. Do not connect to any voltages or signals. Connect the P/N signals with a 169 Ω, 1% 0402 resistor.

Table 5-16. A Bus Signals (Sheet 2 of 4)

Signal	Pins	Description	Category	Family	Type	Board Pull-up/ Pull-down?	Rail for Pull-up/ Pull-down?	Industry Standard Compliant?	3.3 V Tolerant?
NA_A0_P_PIN_CK0_DAT_[00:22]_N	D43, C45, B46, A46, F45, C48, F44, C47, D46, D48, E47, F46, G45, H47, G43, J48, K47, J46, M48, L46, H44, M45, L45	16-Bit Pack Data Output [00:22]	Data	EDI	Drv				
NA_PIN_P_A1_CK0_CLK_P/N	AT42, AR42	Clock Input	Data	EDI	RecDiff				
NA_PIN_P_A1_CK0_DAT_[00:22]_P	AG40, AH41, AJ40, AK41, AL39, AM40, AN39, AN41, AP40, AP42, AR41, AR43, AU43, AT44, AV44, AU45, AW45, AV46, AY46, AW47, BA47, AY48, BB48	16-Bit Pack Data Input [00:22]	Data	EDI	Rec				
NA_PIN_P_A1_CK0_DAT_[00:22]_N	AF40, AG41, AH40, AJ41, AK39, AL40, AM39, AM41, AN40, AN42, AP41, AP43, AT43, AR44, AU44, AT45, AV45, AU46, AW46, AV47, AY47, AW48, BA48	16-Bit Pack Data Input [00:22]	Data	EDI	Rec				
NA_A1_P_PIN_CK0_CLK_P/N	R43, P43	Clock Output	Data	EDI	DrvDiff				

1. Do not connect to any voltages or signals. Connect the P/N signals with a 169 Ω, 1% 0402 resistor.

Table 5-16. A Bus Signals (Sheet 3 of 4)

Signal	Pins	Description	Category	Family	Type	Board Pull-up/ Pull-down?	Rail for Pull-up/ Pull-down?	Industry Standard Compliant?	3.3 V Tolerant?
NA_A1_P_PIN_CK0_DAT_[00:22]_P	K43, J42, L42, K41, M44, L40, M41, N43, M39, P42, N40, P44, R41, T40, U39, T42, W39, V40, U41, Y41, V43, AA42, W42	16-Bit Pack Data Output [00:22]	Data	EDI	Drv				
NA_A1_P_PIN_CK0_DAT_[00:22]_N	J43, H42, K42, J41, L44, K40, L41, M43, L39, N42, M40, N44, P41, R40, T39, R42, V39, U40, T41, W41, U43, Y42, V42	16-Bit Pack Data Output [00:22]	Data	EDI	Drv				
NA_PIN_P_A2_CK0_CLK_P/N	BC44, BB44	Clock Input	Data	EDI	RecDiff				
NA_PIN_P_A2_CK0_DAT_[00:22]_P	AT39, AV39, AU40, AW40, AV41, AY41, AW42, BA42, AY43, BB43, BA44, BB45, BC46, BD45, BD47, BE48, BF47, BG48, BE46, BH46, BG45, BF44, BE43	16-Bit Pack Data Input [00:22]	Data	EDI	Rec				
NA_PIN_P_A2_CK0_DAT_[00:22]_N	AR39, AU39, AT40, AV40, AU41, AW41, AV42, AY42, AW43, BA43, AY44, BA45, BB46, BC45, BC47, BD48, BE47, BF48, BD46, BH47, BG46, BF45, BE44	16-Bit Pack Data Input [00:22]	Data	EDI	Rec				
NA_A2_P_PIN_CK0_CLK_P/N	Y48, W48	Clock Output	Data	EDI	DrvDiff				

1. Do not connect to any voltages or signals. Connect the P/N signals with a 169 Ω, 1% 0402 resistor.

Table 5-16. A Bus Signals (Sheet 4 of 4)

Signal	Pins	Description	Category	Family	Type	Board Pull-up/ Pull-down?	Rail for Pull-up/ Pull-down?	Industry Standard Compliant?	3.3 V Tolerant?
NA_A2_P_PIN_CK0_DAT_[00:22]_P	U44, T45, R46, P47, U46, R48, T47, V45, V48, W44, W47, Y46, AA47, Y43, AC48, AB46, AA45, AC45, AB44, AD44, AC43, AD42, AB41	16-Bit Pack Data Output [00:22]	Data	EDI	Drv				
NA_A2_P_PIN_CK0_DAT_[00:22]_N	T44, R45, P46, N47, T46, P48, R47, U45, U48, V44, V47, W46, Y47, W43, AB48 AA46, Y45, AB45, AA44, AC44, AB43, AC42, AA41	16-Bit Pack Data Output [00:22]	Data	EDI	Drv				
PV_PIN_P_CT_A_TERMREF_P/N	U38, V48	A Bus Terminal Reference (P/N)[1]	ABus	OD	AnlgIn	No			

1. Do not connect to any voltages or signals. Connect the P/N signals with a 169 Ω, 1% 0402 resistor.

5.2.13 PCIe Bus Signals

Table 5-17 lists the PCIe bus signals.

Table 5-17. PCIe Bus Signals (Sheet 1 of 3)

Signal	Pins	Description	Category	Family	Type	Board Pull-up/ Pull-down?	Rail for Pull-up/ Pull-down?	Industry Standard Compliant?	3.3 V Tolerant?
PV_PIN_P_CT_OSC0_E_REFCLK_P/N	AD40, AD39	PCIe Bus Input Reference Clock[1]	PLL/CLK	PCIE	RecDiff	No	N/A	Yes PCIe HCSL	No
PE_PIN_P_E0_CK0_DAT_[00:07]_P	H36, G37, H38, F38, G39, E39, F39, D38	Data Input (16× non-bifurcatable bus)	Data	PCIE	RecDiff				
PE_PIN_P_E0_CK0_DAT_[00:07]_N	H35, G36, H37, F37, G38, E38, F40, D37,	Data Input (16× non-bifurcatable bus)	Data	PCIE	RecDiff				
PE_PIN_P_E0_CK1_DAT_[00:07]_P	E41, D40, C41, C38, A42, B41, A41, B40	Data Input (16× non-bifurcatable bus)	Data	PCIE	RecDiff				
PE_PIN_P_E0_CK1_DAT_[00:07]_N	E40, D39, C40, C39, A43, B42, A40, B39	Data Input (16× non-bifurcatable bus)	Data	PCIE	RecDiff				
PE_E0_P_PIN_CK0_DAT_[00:07]_P	G30, F32, G32, E33, F34, D34, E34, D32	Data Output (16× non-bifurcatable bus)	Data	PCIE	DrvDiff				
PE_E0_P_PIN_CK0_DAT_[00:07]_N	G31, F31, G33, E32, F33, D33, E35, D31	Data Output (16× non-bifurcatable bus)	Data	PCIE	DrvDiff				
PE_E0_P_PIN_CK1_DAT_[00:07]_P	C35, C33, A36, B35, A34, B34, A32, B31	Data Output (16× non-bifurcatable bus)	Data	PCIE	DrvDiff				
PE_E0_P_PIN_CK1_DAT_[00:07]_N	C34, C32, A37, B36, A35, B33, A31, B30	Data Output (16× non-bifurcatable bus)	Data	PCIE	DrvDiff				
PE_CT_P_PIN_E0_PERST0_B	H33	PCIe Reset 0[2]	Control	OD	Drv		3.3 V AUX	Yes	Yes

1. See the IBM reference design for implementation details.
2. IBM uses a 4.7 KΩ pull-up. Follow PCIe slot/device endpoint specifications. If the bus is not used, this pin can be a no connect. See *Section 3.3.4 PCIe Bus* on page 20 for additional information.
3. Do not connect to any voltages or signals. Connect the P/N signals with a 169 Ω, 1% 0402 resistor.
4. The PRSNT signal has an internal 1 KΩ pull-up to 1.1 V. An additional onboard pull-up of the specified value range is only required if the signal is part of a level-translation circuit. See *Section 3.3.4 PCIe Bus* on page 20 for additional information.

Table 5-17. PCIe Bus Signals (Sheet 2 of 3)

Signal	Pins	Description	Category	Family	Type	Board Pull-up/ Pull-down?	Rail for Pull-up/ Pull-down?	Industry Standard Compliant?	3.3 V Tolerant?
PE_CT_P_PIN_E0_PERST1_B	J34	PCIe Reset 1[2]	Control	OD	Drv		3.3 V AUX	Yes	Yes
PE_PIN_P_CT_E0_PRSNT0_B	J33	Present 0[4]	Control	OD	Rec	Pull-up ≤ 3 KΩ ±5%		No	No
PE_PIN_P_CT_E0_PRSNT1_B	J32	Present 1[4]	Control	OD	Rec	Pull-up ≤ 3 KΩ ±5%		No	No
PE_CT_P_PIN_E0_SLOT_CLK0_P/N	AD37, AC37	Clock 0 P/N	PLL	PCIE	DrvDiff	Pull-down 50 Ω ±5%	GND	Yes	Yes[a]
PV_PIN_P_CT_E0_TERMREF_P/N	M37, N37	PHY Support[3]	PCIe	Analog	AnlgIn	No			
PV_PIN_P_CT_E1_TERMREF_P/N	AT38, AR38	PHY Support[3]	PCIe	Analog	AnlgIn	No			
PE_PIN_P_E1_CK0_DAT_[00:07]_P	BA36, BB37, BA38, BC38, BB39, BD39, BC40, BE37	Data Input (16×/8× bifurcatable bus)	Data	PCIE	RecDiff				
PE_PIN_P_E1_CK0_DAT_[00:07]_N	BA35, BB36, BA37, BC37, BB38, BD38, BC39, BE38	Data Input (16×/8× bifurcatable bus)	Data	PCIE	RecDiff				
PE_PIN_P_E1_CK1_DAT_[00:07]_P	BD41, BE40, BF41, BF38, BH42, BG41, BH41, BG40	Data Input (16×/8× bifurcatable bus)	Data	PCIE	RecDiff				
PE_PIN_P_E1_CK1_DAT_[00:07]_N	BD40, BE39, BF40, BF39, BH43, BG42, BH40, BG39	Data Input (16×/8× bifurcatable bus)	Data	PCIE	RecDiff				
PE_E1_P_PIN_CK0_DAT_[00:07]_P	BC31, BB31, BB33, BD33, BC34, BE34, BD35, BE32	Data Output (16×/8× bifurcatable bus)	Data	PCIE	DrvDiff				

1. See the IBM reference design for implementation details.
2. IBM uses a 4.7 KΩ pull-up. Follow PCIe slot/device endpoint specifications. If the bus is not used, this pin can be a no connect. See *Section 3.3.4 PCIe Bus* on page 20 for additional information.
3. Do not connect to any voltages or signals. Connect the P/N signals with a 169 Ω, 1% 0402 resistor.
4. The PRSNT signal has an internal 1 KΩ pull-up to 1.1 V. An additional onboard pull-up of the specified value range is only required if the signal is part of a level-translation circuit. See *Section 3.3.4 PCIe Bus* on page 20 for additional information.

Table 5-17. PCIe Bus Signals (Sheet 3 of 3)

Signal	Pins	Description	Category	Family	Type	Board Pull-up/ Pull-down?	Rail for Pull-up/ Pull-down?	Industry Standard Compliant?	3.3 V Tolerant?
PE_E1_P_PIN_CK0_DAT_[00:07]_N	BC32, BB30, BB32, BD32, BC33, BE33, BD34, BE31	Data Output (16×/8× bifurcatable bus)	Data	PCIE	DrvDiff				
PE_E1_P_PIN_CK1_DAT_[00:07]_P	BF35, BF32, BH37, BG36,BH34, BG33, BH31, BG30	Data Output (16×/8× bifurcatable bus)	Data	PCIE	DrvDiff				
PE_E1_P_PIN_CK1_DAT_[00:07]_N	BF34, BF33, BH36, BG35, BH35, BG34, BH32, BG31	Data Output (16×/8× bifurcatable bus)	Data	PCIE	DrvDiff				
PE_CT_P_PIN_E1_PERST0_B	AV37	PCIe Reset 0[2]	Control	OD	Drv		3.3 V AUX	Yes	Yes
PE_CT_P_PIN_E1_PERST1_B	AU37	PCIe Reset 1[2]	Control	OD	Drv		3.3 V AUX	Yes	Yes
PE_PIN_P_CT_E1_PRSNT0_B	AY35	Present 0[4]	Control	OD	Rec	Pull-up ≤ 3 KΩ ±5%		No	No
PE_PIN_P_CT_E1_PRSNT1_B	BA33	Present 1[4]	Control	OD	Rec	Pull-up ≤ 3 KΩ ±5%		No	No
PE_CT_P_PIN_E1_SLOT_CLK0_P/N	AG38, AF38	Clock 0	CLK	PCIE	DrvDiff	Pull-down 50 Ω ±5%	GND	Yes	No
PE_CT_P_PIN_E1_SLOT_CLK1_P/N	AH37, AG37	Clock 1	CLK	PCIE	DrvDiff	Pull-down 50 Ω ±5%	GND	Yes	No

1. See the IBM reference design for implementation details.
2. IBM uses a 4.7 KΩ pull-up. Follow PCIe slot/device endpoint specifications. If the bus is not used, this pin can be a no connect. See *Section 3.3.4 PCIe Bus* on page 20 for additional information.
3. Do not connect to any voltages or signals. Connect the P/N signals with a 169 Ω, 1% 0402 resistor.
4. The PRSNT signal has an internal 1 KΩ pull-up to 1.1 V. An additional onboard pull-up of the specified value range is only required if the signal is part of a level-translation circuit. See *Section 3.3.4 PCIe Bus* on page 20 for additional information.

5.2.14 PSI Signals

Table 5-18 lists the PSI signals. The PSI interface is not used in OpenPOWER systems; however, some of the nets require termination as shown in *Table 5-18*.

Table 5-18. PSI Signals

Signal	Pins	Description	Category	Family	Type	Board Pull-up/ Pull-down?	Rail for Pull-up/ Pull-down?	Industry Standard Compliant?	3.3 V Tolerant?
PV_CT_P_PIN_PSI_CLK_P/N	AK12, AL12	No connect. Float Output Clock.	PSI	EI4	DrvDiff	No	N/A	–	No
PV_CT_P_PIN_PSI_DATA	AL11	Output Data. No Connect.	PSI	EI4	Drv	No	N/A	–	No
PV_PIN_P_CT_PSI_DATA	AN11	Input Data. No Connect.	PSI	EI4	Rec	No	N/A	–	No
PV_PIN_P_CT_PSI_CLK_P	AP12	Unused. Terminate Input Clock.	PSI	EI4	RecDiff	Pull-down 49 Ω	GND	–	No
PV_PIN_P_CT_PSI_CLK_N	AN12	Unused. Terminate Input Clock.	PSI	EI4	RecDiff	Pull-up 49 Ω	1.1 V	–	No

5.2.15 Miscellaneous Signals

Table 5-19 lists the JTAG signals.

Note: JTAG is no longer widely use by IBM Power Systems™ except for debug.

Table 5-19. JTAG Signals

Signal	Pins	Description	Category	Family	Type	Board Pull-up/ Pull-down?	Rail for Pull-up/ Pull-down?	Industry Standard Compliant?	3.3 V Tolerant?
TS_PIN_P_CT_CARD_TEST	BD27	Unused. Tie Off.	Pervasive	CMOS	Rec	Pull-down ≤ 3 KΩ ±5%	GND	No	No
TS_PIN_P_CT_JTAG_TMS	G07	Unused. Tie Off.	Pervasive	CMOS	Drv	Pull-up ≤ 3 KΩ ±5%	1.1 V	No	No
TS_PIN_P_CT_JTAG_TDI	F06	Unused. Tie Off.	Pervasive	CMOS	Drv	Pull-up ≤ 3 KΩ ±5%	1.1 V	No	No
TS_CT_P_PIN_JTAG_TDO	E05	Unused. Tie Off.	Pervasive	CMOS	Rec	Pull-up ≤ 3 KΩ ±5%	1.1 V	No	No
TS_PIN_P_CT_EXT_TRIGGER_TCK	P12	Throttle Signal.[1,2]	Pervasive	OD	BiDi	Pull-up ≥ 1 KΩ required	3.3 V	N/A	Yes, up to 3.65 V

1. The TS_PIN_P_CT_EXT_TRIGGER_TCK is an active low signal that can be asserted in the case of an emergency power drop situation. When asserted, it tells the OCC to go to the power state defined for the "N mode" attribute (OPEN_POWER_N_BULK_POWER_LIMIT_WATTS) in the XML file generated by the ServerWiz tool.
2. The reference design implements a possible use case for controlling the TS_PIN_P_CT_EXT_TRIGGER_TCK throttle pin. If one of the power supplies is powered off in a redundant power-supply system, the OCC is instructed to go to power-save mode, which can actuate in less than 10 ms via this throttle pin. This is useful if the total actual system power exceeds the capability of a single power supply (oversubscription). Another common use case is to tie TS_PIN_P_CT_EXT_TRIGGER_TCK to a BMC GPIO for software control.

6. Electrical Characteristics

This section provides AC and DC electrical specifications and thermal characteristics for the POWER8 processor.

6.1 Frequency Domains

Table 6-1 lists the POWER8 and POWER8 memory buffer chip frequency domains and scan frequency domains.

Table 6-1. POWER8/POWER8 memory buffer Frequency Domains (Sheet 1 of 2)

Region	IP	Nominal Frequency	Maximum Frequency	Minimum Frequency	Supply Type	Functional Phase	ET Cycle (ps)	Scan Phase	Scan Cycles	Macro Pin
Core	C1, L2	Varied	5.5	1.2 GHz (200 MHz)	Adaptive and Dynamic	M, M×2	208	S	416	nclk
Chiplet	L3, NCU	Varied	2.75	0.6 GHz (200 MHz)	Adaptive and Dynamic	M1×2	416	S1	416	cache_nclk
PB	nest	2.4 GHz	2.7 GHz	1.9 GHz	Fixed (V_{IO})	NASYNC (×2), N[0:9]ASYNC (×2)	364	SN SN[0:9]	728	nest_nclk
MCIO	DMI	4.8 GHz	5.4 GHz	3.8 GHz	Fixed (V_{IO})	MCIO (×2/×4)	182/364/ 728	N/A	N/A	mcio_nclk
A	A0:2	1.6 GHz	1.8 GHz	1.2 GHz	Fixed (V_{IO})	AASYNC (×2)	550/1100	SA	550	a_nclk
AIO	DiffA	3.2 GHz	3.6 GHz	2.4 GHz	Fixed (V_{IO})	AIO/AIO×2/ AIO×4	275/550/ 1100	N/A	N/A	aio_nclk
PCIe	PCIe	1 GHz	1.1 GHz	0.9 GHz	Fixed (V_{IO})	PCIASYNC (×2/×4)	790/1580/ 3160	SPCI	790	pcie_nclk
PCIIO	PCI	8/5/2.5 GHz	8.8/5.5/2.5 GHz	7.2/4.5/ 2.25 GHz	Fixed (V_{PCI})	PCIIO (×2/×4/×8/×16/ ×32/×64/ ×128)	100	N/A	N/A	No grid clock; various tree clocks
PCIREF	PCI	0.1 GHz	0.1 GHz	0.1 GHz	Fixed (V_{PCI})	PCIREF	7900	N/A	N/A	No grid clock (trees)
PCIFB	PCI	0.1 GHz	0.1 GHz	0.1 GHz	Fixed (V_{PCI})	PCIFB	6400	N/A	N/A	No grid clock (trees)

1. Depends on PHY being at 1.2 V.

Table 6-1. POWER8/POWER8 memory buffer Frequency Domains (Sheet 2 of 2)

Region	IP	Nominal Frequency	Maximum Frequency	Minimum Frequency	Supply Type	Functional Phase	ET Cycle (ps)	Scan Phase	Scan Cycles	Macro Pin
FSI	FSI	166 MHz	166 MHz	1 KHz	Fixed (V_{SB})	FS0CLK, FS1CLK, FSFCLK	5200	SFS	5200	fsi_ck
DDR Memory	MBU	2.4 GHz	2.6 GHz	1.33 GHz	Fixed (V_{DD})	MEM, MEM×2, MEM×4	326	SMEM	652	mem_nclk
SDR Memory	Combo PHY	1200	1200	667	Fixed (V_{DD}, DDR)	DPHY0/1 (×2/×4), SYS, SYSC, SYSQ, SYSQC, RD, DQSMUX, WR	760[1]	SDPHY0 SDPHY1	760	dphy_nclk, sys_nclk, sysc_nclk, sysq_nclk, sysqc_nclk, rd_nclk, dqsmux_nclk, wr_nclk

1. Depends on PHY being at 1.2 V.

6.2 DC Electrical Characteristics

See the _IBM POWER8 Systems Power Design and Validation Guide_ for voltage and current specificiations.

6.2.1 Frequencies and TDP

Table 6-2 lists projected frequencies and TDPs for the POWER8 processor.

Table 6-2. Frequencies and TDP
Note: Values in this table are pending hardware validation and are subject to change.

Part Number	Active Cores	Nominal Frequency (GHz)	Turbo Frequency (GHz)	Nominal TDP (W)	Turbo Power (W)	T_J Maximum (°C)	ADP T_J (°C)	Notes
00NH512	12	TBD	TBD	190	247	85	70	
00UL863	12	2.561	3.226	190	247	85	70	
00UL864	10	2.926	3.492	190	247	85	70	
00UL866	8	3.325	3.857	190	247	85	70	
00UL865	10	2.095	2.827	140	179	85	70	1
				145	184			2
00UL867	8	2.328	3.026	130	169	85	70	1
				135	174			2

1. Power specification associated with 1.05 V V_{IO}. See the _POWER8 Systems Power Design and Validation Guide_ for more information on voltage supply specifications.
2. Power specification associated with 1.10 V V_{IO}. See the _POWER8 Systems Power Design and Validation Guide_ for more information on voltage supply specifications.

6.2.2 Miscellaneous Signals

See the _I²C Bus Specification (version 2.1)_ for DC electrical details of the I²C bus.

Table 6-3. I²C DC Voltage

DC Voltage	Description
I²C Voltage	3.3 V V_{DD}
V_{IH}	$V_{DD} \times 0.7 = 2.3$ V
V_{IL}	$V_{DD} \times 0.3 = 0.99$ V

See the _PCI Local Bus Specification (Revision 3.0)_ for DC electrical details for the LPC bus.

See the _POWER8 Power Systems Signal Integrity Miscellaneous Nets Topology Design Guidelines_ for additional information about the FSI signals.

6.3 AC Electrical Characteristics

This section provides the preliminary AC electrical characteristics for the POWER8 processor. After fabrication, parts are sorted by maximum processor core frequency and tested for conformance to the AC specifications for that frequency.

6.3.1 Clock AC Specifications

System reference clocks are 133.33 MHz and use host clock signal level (HCSL) differential levels, which are the same as the PCIe standard levels. Termination of 50 Ω to GND on each phase is required and is built into the Silicon Labs clock generators that the POWER8 processor uses. There is also the same 50 Ω to GND termination built into the differential receivers on the processor chip, but they are not enabled when the Silicon Labs clock generators are used. They must be enabled if some other vendor clock generator was used that did not have the integrated termination.

Spread spectrum is only allowed on the system reference clocks. It is limited to a spread percentage of 0.5% in the downward direction, which is the specification allowed by the DRAMs.

PCIe reference clocks are 100.00 MHz and use HCSL differential levels, which are the same as the PCIe standard levels. Termination of 50 Ω to GND on each phase is required and is built into the Silicon Labs clock generators that the POWER8 processor uses. There is also the same 50 Ω to GND termination built into the differential receivers on the processor chip, but they are not enabled when the Silicon Labs clock generators are used. They must be enabled if some other vendor clock generator is used that does not have the integrated termination.

PCIe and system reference clocks are HCSL differential levels, which is the PCIe standard. Spread spectrum is not supported by POWER systems on PCIe.

The LPC clock to the processor is 33.33 MHz single-ended CMOS with an MPUL of 1.1 V. The IBM system has a resistor divider network on the board to support this. The reference clock skew specification for LPC is 2.0 ns.

The TOD reference clocks to the processor are 16.0 MHz (20 PPM frequency stability), single-ended CMOS with an MPUL of 1.1 V. There is a resistor divider network on the board to support this.

Figure 6-1 shows the differential HCSL reference clock waveforms.

Figure 6-1. Differential (HCSL) Reference Clock Waveform (System and PCIe)
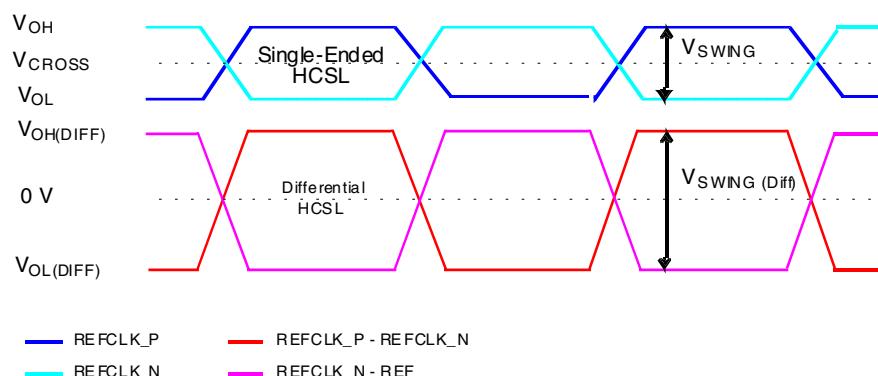
Table 6-4. Differential Reference Clock DC and AC Specification

Symbol	Parameter	Minimum	Typical	Maximum	Units	Notes
V_{OL}	Output low voltage	-0.10	0.0	0.1	V	1
V_{OH}	Output high voltage	0.50	0.70	0.90	V	1
V_{SWING}	Voltage swing	0.50	0.70	1.0	V	1
V_{CROSS}	Absolute crossing point (common mode voltage)	250	350	500	mV	1, 2, 3
V_{CROSS} Delta	Maximum variation in common mode voltage	–	–	100	mV	1, 2, 4
V_{MAX}	Absolute maximum voltage	–	–	1.15	V	1, 5
V_{MIN}	Absolute minimum voltage	-0.20	–	–	V	1, 6
V_{OL} (Diff)	Output low voltage	-0.5	-0.7	-0.9	V	7
V_{OH} (Diff)	Output high voltage	0.50	0.70	0.90	V	7
V_{SWING} (Diff)	Voltage swing (differential)	1.0	1.4	1.8	V	7
T_R, T_F (Diff)	Rising and falling edge rates (differential)	1.0	2.0	4.0	V/ns	7, 8
V_{RB}	Ringback voltage margin	-100	–	100	mV	7, 9
T_{STABLE}	Time before V_{RB} is allowed	500	–	–	ps	7, 9
Duty Cycle	Duty cycle	45	–	55	%	7
T Period Average	Average clock period accuracy	50	–	2550	PPM	7, 10, 11, 12

1. Measurement taken from a single-ended waveform (see *Table 6-1* on page 62).
2. Measured at the crossing point where the instantaneous voltage value of the rising edge of REFCLK_P equals the falling edge of REFCLK_N (see *Figure 6-2* on page 64).
3. Refers to the total variation from the lowest crossing point to the highest crossing point, regardless of which edges are crossing. Refers to all crossing points for this measurement (see *Figure 6-2* on page 64).
4. Defined as the total variation of all crossing voltages of rising REFCLK_P and falling REFCLK_N. This is the maximum allowed variance in V_{CROSS} for any particular system (see *Figure 6-3* on page 65).
5. Defined as the maximum instantaneous voltage including overshoot (see *Figure 6-2* on page 64).
6. Defined as the minimum instantaneous voltage including overshoot (see *Figure 6-2* on page 64).
7. Measurement taken from a differential waveform (see *Figure 6-1* on page 62).
8. Measured from -150 mV to +150 mV on the differential waveform (derived from REFCLK_P - REFCLK_N). The signal must be monotonic through the measurement region for rise and fall time. The 300 mV measurement window is centered on the differential zero crossing (see *Figure 6-5* on page 65).
9. T_{STABLE} is the time that the differential clock must maintain a minimum ±150 mV differential voltage after the rising/falling edges before it is allowed to drop back into the V_{RB} ±100 mV differential range (see *Figure 6-6* on page 66).
10. Defined as the average period. This includes crystal PPM and spread spectrum.
11. Defined as the frequency accuracy specification of the crystal that is used to generate the reference clock (typically less than 100 PPM).
12. PPM refers to parts per million and is a DC absolute period accuracy specification. One PPM is 1/1,000,000th of the clock frequency. The period is to be measured with a frequency counter with the measurement window set to 100 ms or greater. For systems that use spread-spectrum clocking, there is an additional 2,500 PPM average shift in the maximum period resulting from a 0.5% down spread.

Figure 6-2 shows the single-ended measurement points for absolute cross points and swing.

Figure 6-2. Single-Ended Measurement Points for Absolute Cross Points and Swing
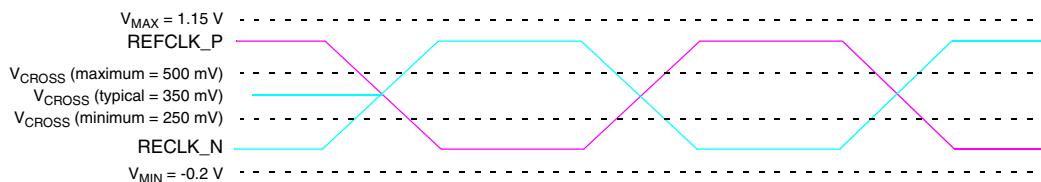
6.3.2 Differential Reference Clock Measurements

Figure 6-3 shows the single-ended measurement points for the delta cross point.

Figure 6-3. Single-Ended Measurement Points for Delta Cross Point
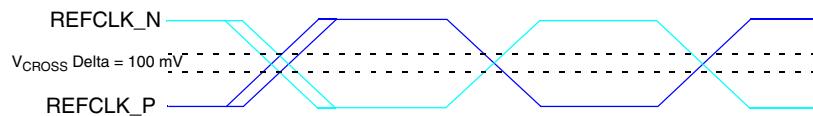
Figure 6-4 shows the differential measurement points for the duty cycle and period.

Figure 6-4. Differential Measurement Points for Duty Cycle and Period
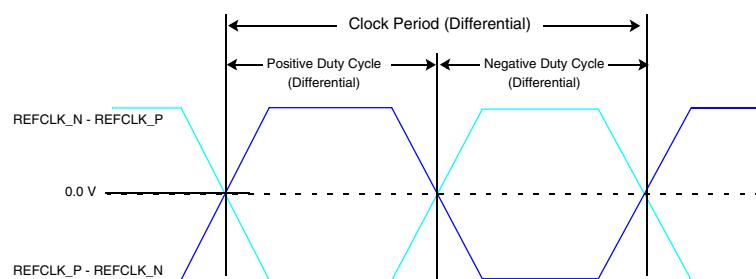
Figure 6-5 shows the differential measurement points for the rise and fall times.

Figure 6-5. Differential Measurement Points for Rise and Fall Times
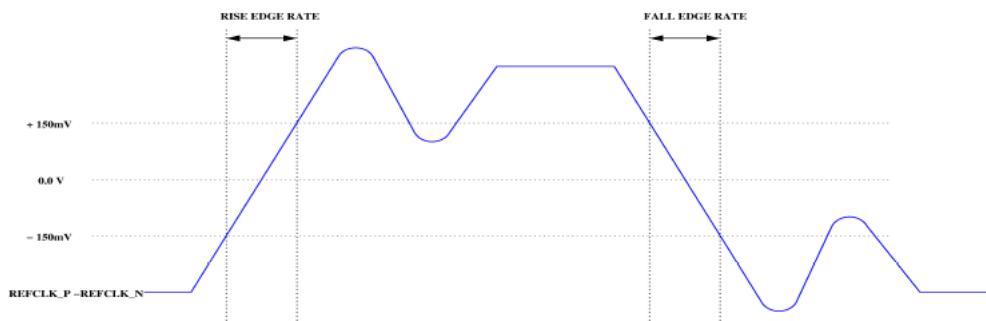
Figure 6-6 shows the differential measurement points for ringback.

Figure 6-6. Differential Measurement Points for Ringback
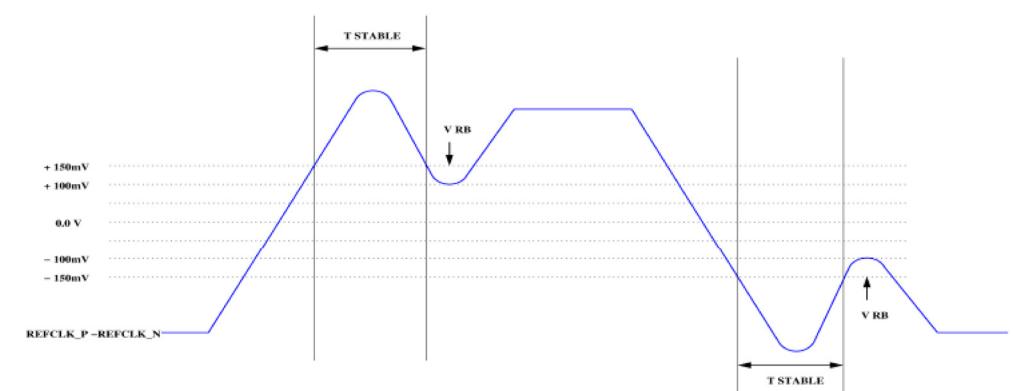
Table 6-5 lists general DC and AC specifications.

Table 6-5. DC and AC Specifications

Parameter	Symbol	Test Condition	Minimum	Typical	Maximum	Units	Notes
Output Voltage	V_{OL}	Output low voltage	–	0	0.2	V	1
	V_{OH}	Output high voltage	0.8	1.0	1.15	V	1
	V_{SWING}	Peak-peak, single-ended swing	0.8	1.0	1,15	V	1, 2
Rise and Fall Times	T_R, T_F	20% - 80%	–	1.5	3.0	ns	1, 3
Duty Cycle	DC	Measured at V_{SWING}/2	45	–	55	%	1, 2, 4
Clock Period	T_{AVG}	Clock period accuracy	-50	–	+50	PPM	1, 2, 4, 5

1. Measurements taken from a single-ended waveform (see *Figure 6-7* on page 67).
2. Voltage swing is equal to V_{OH} - V_{OL} (see *Figure 6-7* on page 67).
3. Rise and fall time measurements taken between 20% and 80% of V_{OH} and V_{OL} (see *Figure 6-7* on page 67).
4. Measurements taken at a voltage equal to V_{SWING}/2 (see *Figure 6-8* on page 67).
5. PPM refers to parts per million and is a DC absolute period accuracy specification. It includes only the accuracy of the crystal that is used to generate the clock because spread spectrum is not enabled. The period is to be measured with a frequency counter with the measurement window set to 100 ms or greater,

Figure 6-7 shows the single-ended processor reference clocks and highlights the voltage and transition time measurement points.

Figure 6-7. Single-Ended Processor Reference Clocks (Voltage and Transition Time Measurement Points)

Single-Ended Reference Clock Waveforms (LPC and TOD Clocks)
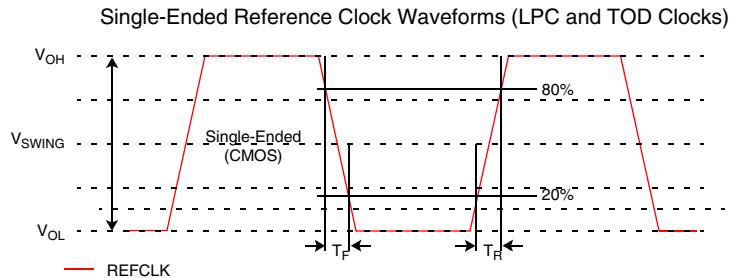
Figure 6-8 shows the single-ended processor reference clocks and highlights the period and duty cycle measurement points.

Figure 6-8. Single-Ended Processor Reference Clocks (Period and Duty-Cycle Measurement Points)
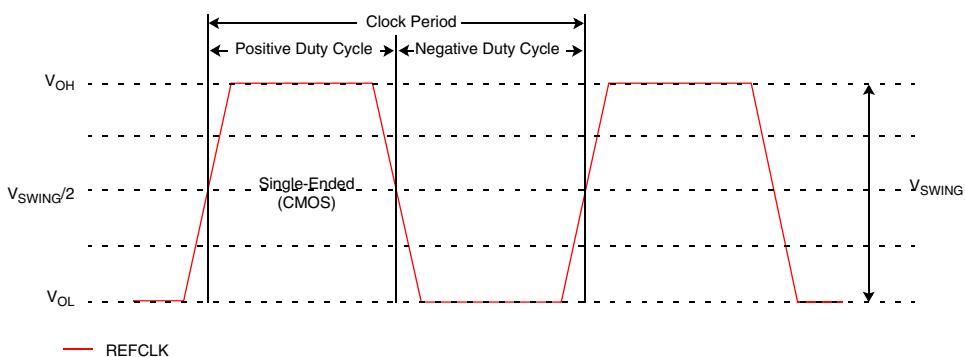
6.3.3 FSI AC Specifications

Table 6-6 lists the AC specifications for the FSI bus.

Table 6-6. FSI Electrical Specification

Description	Minimum	Typical	Maximum	Units	Notes
C4 V_{MAX}			1.65	V	Maximum voltage at the chip pad.
Receiver V_{IL}			$0.3 \times 1.2\ V_{SB}$	mV	For receiver input hysteresis.
Receiver V_{IH}	$0.7 \times 1.2\ V_{SB}$			mV	For receiver input hysteresis.
1 KΩ Pull-up Resistance	1 KΩ	1.25 KΩ	1.5 KΩ	Ω	Pull-up resistance without leakage. If external pull-ups are used, they must be returned to V_{DOUT} and have a combined impedance not smaller than 1 KΩ.
1 KΩ Pull-down Resistance	1 KΩ	1.25 KΩ	1.5 KΩ	Ω	Pull-down resistance without leakage. If external pull downs are used, they have a combined impedance not smaller than 1 KΩ in parallel with 10 KΩ.
10 KΩ Pull-down Resistance	10 KΩ	12.5 KΩ	15 KΩ	Ω	Pull-up resistance without leakage.
Driver V_{OL}	$-0.1 \times 1.2\ V_{SB}$		$0.2 \times 1.2\ V_{SB}$	mV	Output pad driver levels.
Driver V_{OH}	$0.8 \times 1.2\ V_{SB}$		$1.1 \times 1.2\ V_{SB}$	mV	Output pad driver levels.
Duty Cycle distortion at 533 MHz with a 2 pF load	44.8	0	55.2	%	
Rise/Fall Time (10% - 90% of V_{DOUT} with a 2 pF load)	100	300	500	ps	

Table 6-7 lists the default settings for the internal FSI pull-up and pull-down resistors.

Table 6-7. Default FSI Settings (Sheet 1 of 2)

Function	SCM Pin	Pull-Up Internal Value	Pull-Down Internal Value
FSI0 Clock	BE29	–	10 KΩ
FSI0 Data	BE28	1 KΩ	–
FSI1 Clock	BA40	–	10 KΩ
FSI Master 0 Clock	BC42	–	–
FSI Master 0 Data	BB41	–	10 KΩ
FSI Master 1 Clock	AW38	–	–
FSI Master 1 Data	AY39	–	10 KΩ
FSI Master 2 Clock	BA25	–	–
FSI Master 2 Data	BA24	–	10 KΩ
FSI Master 3 Clock	AY23	–	–
FSI Master 3 Data	AY24	–	10 KΩ
FSI Master 6 Clock	BB22	–	–
FSI Master 6 Data	BB23	–	10 KΩ
FSI Master 7 Clock	BA22	–	–

Table 6-7. Default FSI Settings (Sheet 2 of 2)

Function	SCM Pin	Pull-Up Internal Value	Pull-Down Internal Value
FSI Master 7 Data	BA21	–	10 KΩ
FSI Master CP 1 Clock	BB25	–	–
FSI Master CP 1 Data	BB26	–	10 KΩ
FSI Master CP 2 Clock	BC24	–	–
FSI Master CP 2 Data	BC23	–	10 KΩ
FSI Master CP 3 Clock	BD24	–	–
FSI Master CP 3 Data	BD25	–	10 KΩ

6.3.4 SPI AC Specifications

Table 6-8 list the AC specifications for the SPI bus.

Table 6-8. SPI AC Specification

Description	Minimum	Typical	Maximum	Units	Notes
C4 V_{MAX}			1.65	V	Maximum voltage at the chip pad.
Receiver V_{IL}			$0.3 \times V_{I/O}$	mV	For receiver input hysteresis.
Receiver V_{IH}	$0.7 \times V_{I/O}$			mV	For receiver input hysteresis.
1 KΩ Pull-up Resistance	1 KΩ	1.25 KΩ	1.5 KΩ	Ω	Pull-up resistance without leakage. If external pull-ups are used, they must be returned to V_{DOUT} and have a combined impedance not smaller than 1 KΩ.
1 KΩ Pull-down Resistance	1 KΩ	1.25 KΩ	1.5 KΩ	Ω	Pull-down resistance without leakage. If external pull downs are used, they have a combined impedance not smaller than 1 KΩ in parallel with 10 KΩ.
10 KΩ Pull-down Resistance	10 KΩ	12.5 KΩ	15 KΩ	Ω	Pull-up resistance without leakage.
Driver V_{OL}	$-0.1 \times V_{I/O}$		$0.2 \times V_{I/O}$	mV	Output pad driver levels.
Driver V_{OH}	$0.8 \times V_{I/O}$		$1.1 \times V_{I/O}$	mV	Output pad driver levels.
Duty Cycle distortion at 533 MHz with a 2 pF load	44.8	0	55.2	%	
Rise/Fall Time (10% - 90% of V_{DOUT} with a 2 pF load)	100	300	500	ps	

Table 6-9 lists the default settings for the internal SPI pull-up and pull-down resistors.

Table 6-9. Default SPI Settings

Function	SCM Pin	Pull-Up Internal Value	Pull-Down Internal Value
SPIVID0_MOSI	H29	–	–
SPIVID0_MISO	J30	–	–
SPIVID0_SCLK	H28	–	10 KΩ
SPIVID0_CS	J28	1 KΩ	–
SPIPSS_MOSI	Y37	–	–
SPIPSS_MISO	V37	–	–
SPIPSS_SCLK	AA39	–	10 KΩ
SPIPSS_CS0	AA38	1 KΩ	–
SPIPSS_CS1	AA37	1 KΩ	–

7. Mechanical Specifications

This section describes the POWER8 SCM features and pin list.

7.1 Single-Chip Module

Table 7-1 describes the SCM.

Table 7-1. SCM Features

Feature	Description
Body Size	50 x 50 mm
Package Type	FC PLGA
Interconnect Technology	22 nm silicon-on-insulator (SOI)
	1.0 mm orthogonal pin pitch
	6-2-6 LGA
Buses	Four DMI interfaces at 9.6 Gb/s
	Three 2-byte A buses at 6.4 Gb/s
	Two x16 PCIe Generation 3 at 8 Gb/s
Power	130 W, 135 W, 140W, 145 W, or 190 W
Package Pin Assignments	2296 total
SEEPROM Structure	Single SEEPROM

7.2 Electrostatic Discharge Considerations

The POWER8 processor is electrostatic discharge (ESD) sensitive. An appropriate ESD handling procedure must be implemented and maintained by facilities handling this component. Handle according to the ANSI/ESD S20.20 or IEC 61340-5-1 standard. Packaging of this product in an ESD safe container must be maintained according to the ANSI/ESD S541 or IEC 61340-5-3 standard.

The POWER8 processor has completed an ESD stress qualification in accordance with the JEDEC specification JESD47I. The levels shown in *Table 7-2* have been met.

Table 7-2. ESD Stress Qualification

ESD Model	Passing Level	Reference
Human Body Model	1250 V	JS-001[1]
Charged Device Model (CDM) NonPCIe pins	250 V	JESD22-C101[2]
CDM PCIe pins	100 V	JESD22-C101[2]

1. JS-001-2014 is the Joint JEDEC/ESDA Standard for Electrostatic Discharge Sensitivity Test - Human Body Model (HBM) Component Level.
2. JESD22-C101F is the Field-Induced Charged-Device Model Test Method for Electrostatic Discharge Withstand Thresholds of Microelectronic Components.

7.3 Mechanical Drawings

See IBM OpenPOWER Connect for the current mechanical drawings and recommended module layout.

7.4 Pinout

Table 7-3 SCM Pin List on page 73 shows the signal pins for the POWER8 processor by position.

Table 7-3. SCM Pin List

Position	Net Name	Position	Net Name	Position	Net Name
A04	GND	A42	PE_PIN_P_E0_CK1_DAT_04_P	B34	PE_E0_P_PIN_CK1_DAT_05_P
A05	MM_PIN_P_M0_CKD_DAT_10_P	A43	PE_PIN_P_E0_CK1_DAT_04_N	B35	PE_E0_P_PIN_CK1_DAT_03_P
A06	MM_PIN_P_M0_CKD_DAT_10_N	A44	GND	B36	PE_E0_P_PIN_CK1_DAT_03_N
A07	GND	A45	GND	B37	GND
A08	MM_PIN_P_M0_CKD_DAT_13_P	A46	NA_A0_P_PIN_CK0_DAT_03_N	B38	GND
A09	MM_PIN_P_M0_CKD_DAT_13_N	A47	NA_A0_P_PIN_CK0_DAT_03_P	B39	PE_PIN_P_E0_CK1_DAT_07_N
A10	MM_PIN_P_M0_CKD_DAT_17_N	A48	GND	B40	PE_PIN_P_E0_CK1_DAT_07_P
A11	MM_PIN_P_M0_CKD_DAT_17_P	B03	GND	B41	PE_PIN_P_E0_CK1_DAT_05_P
A12	GND	B04	MM_PIN_P_M0_CKD_DAT_09_P	B42	PE_PIN_P_E0_CK1_DAT_05_N
A13	GND	B05	MM_PIN_P_M0_CKD_DAT_09_N	B43	GND
A14	MM_PIN_P_M0_CKC_DAT_02_P	B06	MM_PIN_P_M0_CKD_CLK_P	B44	GND
A15	MM_PIN_P_M0_CKC_DAT_02_N	B07	MM_PIN_P_M0_CKD_CLK_N	B45	NA_A0_P_PIN_CK0_DAT_02_P
A16	GND	B08	GND	B46	NA_A0_P_PIN_CK0_DAT_02_N
A17	MM_PIN_P_M0_CKC_DAT_05_P	B09	MM_PIN_P_M0_CKD_DAT_15_P	B47	GND
A18	MM_PIN_P_M0_CKC_DAT_05_N	B10	MM_PIN_P_M0_CKD_DAT_15_N	B48	NA_A0_P_PIN_CK0_DAT_05_P
A19	MM_PIN_P_M0_CKC_DAT_09_P	B11	MM_PIN_P_M0_CKD_DAT_18_N	C02	GND
A20	MM_PIN_P_M0_CKC_DAT_09_N	B12	MM_PIN_P_M0_CKD_DAT_18_P	C03	GND
A21	GND	B13	GND	C04	GND
A22	MM_PIN_P_M0_CKC_CLK_P	B14	GND	C05	MM_PIN_P_M0_CKD_DAT_08_N
A23	MM_PIN_P_M0_CKC_CLK_N	B15	GND	C06	MM_PIN_P_M0_CKD_DAT_08_P
A24	MM_PIN_P_M0_CKC_DAT_15_P	B16	MM_PIN_P_M0_CKC_DAT_03_P	C07	MM_PIN_P_M0_CKD_DAT_11_P
A25	MM_PIN_P_M0_CKC_DAT_15_N	B17	MM_PIN_P_M0_CKC_DAT_03_N	C08	MM_PIN_P_M0_CKD_DAT_11_N
A26	GND	B18	MM_PIN_P_M0_CKC_DAT_06_P	C09	GND
A27	MM_PIN_P_M0_CKC_DAT_19_N	B19	MM_PIN_P_M0_CKC_DAT_06_N	C10	MM_PIN_P_M0_CKD_DAT_14_P
A28	MM_PIN_P_M0_CKC_DAT_19_P	B20	GND	C11	MM_PIN_P_M0_CKD_DAT_14_N
A29	GND	B21	MM_PIN_P_M0_CKC_DAT_10_P	C12	MM_PIN_P_M0_CKD_DAT_19_N
A30	GND	B22	MM_PIN_P_M0_CKC_DAT_10_N	C13	MM_PIN_P_M0_CKD_DAT_19_P
A31	PE_E0_P_PIN_CK1_DAT_06_N	B23	MM_PIN_P_M0_CKC_DAT_12_P	C14	GND
A32	PE_E0_P_PIN_CK1_DAT_06_P	B24	MM_PIN_P_M0_CKC_DAT_12_N	C15	MM_PIN_P_M0_CKC_DAT_00_P
A33	GND	B25	GND	C16	MM_PIN_P_M0_CKC_DAT_00_N
A34	PE_E0_P_PIN_CK1_DAT_04_P	B26	MM_PIN_P_M0_CKC_DAT_16_N	C17	MM_PIN_P_M0_CKC_DAT_04_P
A35	PE_E0_P_PIN_CK1_DAT_04_N	B27	MM_PIN_P_M0_CKC_DAT_16_P	C18	MM_PIN_P_M0_CKC_DAT_04_N
A36	PE_E0_P_PIN_CK1_DAT_02_P	B28	GND	C19	GND
A37	PE_E0_P_PIN_CK1_DAT_02_N	B29	GND	C20	MM_PIN_P_M0_CKC_DAT_11_P
A38	GND	B30	PE_E0_P_PIN_CK1_DAT_07_N	C21	MM_PIN_P_M0_CKC_DAT_11_N
A39	GND	B31	PE_E0_P_PIN_CK1_DAT_07_P	C22	MM_PIN_P_M0_CKC_DAT_13_P
A40	PE_PIN_P_E0_CK1_DAT_06_N	B32	GND	C23	MM_PIN_P_M0_CKC_DAT_13_N
A41	PE_PIN_P_E0_CK1_DAT_06_P	B33	PE_E0_P_PIN_CK1_DAT_05_N	C24	GND

Position	Net Name
C25	MM_PIN_P_M0_CKC_DAT_17_N
C26	MM_PIN_P_M0_CKC_DAT_17_P
C27	GND
C28	GND
C29	GND
C30	GND
C31	GND
C32	PE_E0_P_PIN_CK1_DAT_01_N
C33	PE_E0_P_PIN_CK1_DAT_01_P
C34	PE_E0_P_PIN_CK1_DAT_00_N
C35	PE_E0_P_PIN_CK1_DAT_00_P
C36	GND
C37	GND
C38	PE_PIN_P_E0_CK1_DAT_03_P
C39	PE_PIN_P_E0_CK1_DAT_03_N
C40	PE_PIN_P_E0_CK1_DAT_02_N
C41	PE_PIN_P_E0_CK1_DAT_02_P
C42	GND
C43	GND
C44	NA_A0_P_PIN_CK0_DAT_01_P
C45	NA_A0_P_PIN_CK0_DAT_01_N
C46	GND
C47	NA_A0_P_PIN_CK0_DAT_07_N
C48	NA_A0_P_PIN_CK0_DAT_05_N
D01	MM_M0_P_PIN_CKC_DAT_09_P
D02	GND
D03	GND
D04	GND
D05	GND
D06	MM_PIN_P_M0_CKD_DAT_07_P
D07	MM_PIN_P_M0_CKD_DAT_07_N
D08	MM_PIN_P_M0_CKD_DAT_12_P
D09	MM_PIN_P_M0_CKD_DAT_12_N
D10	GND
D11	MM_PIN_P_M0_CKD_DAT_16_P
D12	MM_PIN_P_M0_CKD_DAT_16_N
D13	MM_PIN_P_M0_CKD_DAT_21_N
D14	MM_PIN_P_M0_CKD_DAT_21_P

Position	Net Name
D15	GND
D16	MM_PIN_P_M0_CKC_DAT_01_P
D17	MM_PIN_P_M0_CKC_DAT_01_N
D18	GND
D19	MM_PIN_P_M0_CKC_DAT_14_P
D20	MM_PIN_P_M0_CKC_DAT_14_N
D21	MM_PIN_P_M0_CKC_DAT_18_N
D22	MM_PIN_P_M0_CKC_DAT_18_P
D23	GND
D24	GND
D25	GND
D26	GND
D27	GND
D28	GND
D29	GND
D30	GND
D31	PE_E0_P_PIN_CK0_DAT_07_N
D32	PE_E0_P_PIN_CK0_DAT_07_P
D33	PE_E0_P_PIN_CK0_DAT_05_N
D34	PE_E0_P_PIN_CK0_DAT_05_P
D35	GND
D36	GND
D37	PE_PIN_P_E0_CK0_DAT_07_N
D38	PE_PIN_P_E0_CK0_DAT_07_P
D39	PE_PIN_P_E0_CK1_DAT_01_N
D40	PE_PIN_P_E0_CK1_DAT_01_P
D41	GND
D42	GND
D43	NA_A0_P_PIN_CK0_DAT_00_N
D44	NA_A0_P_PIN_CK0_DAT_00_P
D45	GND
D46	NA_A0_P_PIN_CK0_DAT_08_N
D47	NA_A0_P_PIN_CK0_DAT_07_P
D48	NA_A0_P_PIN_CK0_DAT_09_N
E01	MM_M0_P_PIN_CKC_DAT_09_N
E02	MM_M0_P_PIN_CKC_DAT_10_P
E03	GND
E04	GND

Position	Net Name
E05	TS_CT_P_PIN_JTAG_TDO
E06	GND
E07	MM_PIN_P_M0_CKD_DAT_05_P
E08	MM_PIN_P_M0_CKD_DAT_05_N
E09	MM_PIN_P_M0_CKD_DAT_06_P
E10	MM_PIN_P_M0_CKD_DAT_06_N
E11	GND
E12	MM_PIN_P_M0_CKD_DAT_20_P
E13	MM_PIN_P_M0_CKD_DAT_20_N
E14	MM_PIN_P_M0_CKD_DAT_23_P
E15	MM_PIN_P_M0_CKD_DAT_23_N
E16	GND
E17	GND
E18	MM_PIN_P_M0_CKC_DAT_20_N
E19	MM_PIN_P_M0_CKC_DAT_20_P
E20	MM_PIN_P_M0_CKC_DAT_21_N
E21	MM_PIN_P_M0_CKC_DAT_21_P
E22	GND
E23	GND
E24	GND
E25	GND
E26	GND
E27	GND
E28	GND
E29	GND
E30	GND
E31	GND
E32	PE_E0_P_PIN_CK0_DAT_03_N
E33	PE_E0_P_PIN_CK0_DAT_03_P
E34	PE_E0_P_PIN_CK0_DAT_06_P
E35	PE_E0_P_PIN_CK0_DAT_06_N
E36	GND
E37	GND
E38	PE_PIN_P_E0_CK0_DAT_05_N
E39	PE_PIN_P_E0_CK0_DAT_05_P
E40	PE_PIN_P_E0_CK1_DAT_00_N
E41	PE_PIN_P_E0_CK1_DAT_00_P
E42	GND

Position	Net Name	Position	Net Name	Position	Net Name
E43	GND	F33	PE_E0_P_PIN_CK0_DAT_04_N	G23	GND
E44	GND	F34	PE_E0_P_PIN_CK0_DAT_04_P	G24	GND
E45	NA_A0_P_PIN_CK0_DAT_04_P	F35	GND	G25	GND
E46	NA_A0_P_PIN_CK0_DAT_08_P	F36	GND	G26	GND
E47	NA_A0_P_PIN_CK0_DAT_10_N	F37	PE_PIN_P_E0_CK0_DAT_03_N	G27	TS_CT_P_PIN_AMX0_VSENSE
E48	NA_A0_P_PIN_CK0_DAT_09_P	F38	PE_PIN_P_E0_CK0_DAT_03_P	G28	GND
F01	MM_M0_P_PIN_CKC_DAT_11_P	F39	PE_PIN_P_E0_CK0_DAT_06_P	G29	GND
F02	MM_M0_P_PIN_CKC_DAT_10_N	F40	PE_PIN_P_E0_CK0_DAT_06_N	G30	PE_E0_P_PIN_CK0_DAT_00_P
F03	MM_M0_P_PIN_CKC_CLK_N	F41	GND	G31	PE_E0_P_PIN_CK0_DAT_00_N
F04	GND	F42	GND	G32	PE_E0_P_PIN_CK0_DAT_02_P
F05	GND	F43	GND	G33	PE_E0_P_PIN_CK0_DAT_02_N
F06	TS_PIN_P_CT_JTAG_TDI	F44	NA_A0_P_PIN_CK0_DAT_06_N	G34	GND
F07	GND	F45	NA_A0_P_PIN_CK0_DAT_04_N	G35	GND
F08	MM_PIN_P_M0_CKD_DAT_03_P	F46	NA_A0_P_PIN_CK0_DAT_11_N	G36	PE_PIN_P_E0_CK0_DAT_01_N
F09	MM_PIN_P_M0_CKD_DAT_03_N	F47	NA_A0_P_PIN_CK0_DAT_10_P	G37	PE_PIN_P_E0_CK0_DAT_01_P
F10	MM_PIN_P_M0_CKD_DAT_04_P	F48	GND	G38	PE_PIN_P_E0_CK0_DAT_04_N
F11	MM_PIN_P_M0_CKD_DAT_04_N	G01	MM_M0_P_PIN_CKC_DAT_11_N	G39	PE_PIN_P_E0_CK0_DAT_04_P
F12	GND	G02	MM_M0_P_PIN_CKC_DAT_12_P	G40	GND
F13	MM_PIN_P_M0_CKD_DAT_22_P	G03	MM_M0_P_PIN_CKC_CLK_P	G41	GND
F14	MM_PIN_P_M0_CKD_DAT_22_N	G04	MM_M0_P_PIN_CKC_DAT_07_N	G42	GND
F15	GND	G05	GND	G43	NA_A0_P_PIN_CK0_DAT_14_N
F16	GND	G06	GND	G44	NA_A0_P_PIN_CK0_DAT_06_P
F17	MM_PIN_P_M0_CKC_DAT_08_N	G07	TS_PIN_P_CT_JTAG_TMS	G45	NA_A0_P_PIN_CK0_DAT_12_N
F18	MM_PIN_P_M0_CKC_DAT_08_P	G08	GND	G46	NA_A0_P_PIN_CK0_DAT_11_P
F19	MM_PIN_P_M0_CKC_DAT_22_P	G09	MM_PIN_P_M0_CKD_DAT_01_N	G47	GND
F20	MM_PIN_P_M0_CKC_DAT_22_N	G10	MM_PIN_P_M0_CKD_DAT_01_P	G48	NA_A0_P_PIN_CK0_CLK_N
F21	GND	G11	MM_PIN_P_M0_CKD_DAT_02_P	H01	GND
F22	GND	G12	MM_PIN_P_M0_CKD_DAT_02_N	H02	MM_M0_P_PIN_CKC_DAT_12_N
F23	GND	G13	GND	H03	MM_M0_P_PIN_CKC_DAT_08_P
F24	GND	G14	GND	H04	MM_M0_P_PIN_CKC_DAT_07_P
F25	GND	G15	GND	H05	MM_M0_P_PIN_CKC_DAT_05_N
F26	GND	G16	MM_PIN_P_M0_CKC_DAT_07_N	H06	GND
F27	TS_CT_P_PIN_AMX0_GSENSE	G17	MM_PIN_P_M0_CKC_DAT_07_P	H07	GND
F28	GND	G18	MM_PIN_P_M0_CKC_DAT_23_P	H08	TS_CT_P_PIN_PROBE1_N
F29	GND	G19	MM_PIN_P_M0_CKC_DAT_23_N	H09	GND
F30	GND	G20	GND	H10	MM_PIN_P_M0_CKD_DAT_00_P
F31	PE_E0_P_PIN_CK0_DAT_01_N	G21	GND	H11	MM_PIN_P_M0_CKD_DAT_00_N
F32	PE_E0_P_PIN_CK0_DAT_01_P	G22	GND	H12	GND

Position	Net Name	Position	Net Name	Position	Net Name
H13	GND	J03	MM_M0_P_PIN_CKC_DAT_08_N	J41	NA_A1_P_PIN_CK0_DAT_03_N
H14	GND	J04	MM_M0_P_PIN_CKC_DAT_06_N	J42	NA_A1_P_PIN_CK0_DAT_01_P
H15	GND	J05	MM_M0_P_PIN_CKC_DAT_05_P	J43	NA_A1_P_PIN_CK0_DAT_00_N
H16	GND	J06	MM_M0_P_PIN_CKC_DAT_03_N	J44	NA_A0_P_PIN_CK0_DAT_20_P
H17	GND	J07	GND	J45	GND
H18	TS_CT_P_PIN_M0_T_PLLHFC_MKERF_N	J08	TS_CT_P_PIN_PROBE1_P	J46	NA_A0_P_PIN_CK0_DAT_17_N
H19	GND	J09	GND	J47	NA_A0_P_PIN_CK0_DAT_13_P
H20	GND	J10	GND	J48	NA_A0_P_PIN_CK0_DAT_15_N
H21	GND	J11	GND	K01	MM_M0_P_PIN_CKC_DAT_14_N
H22	GND	J12	GND	K02	MM_M0_P_PIN_CKC_DAT_15_P
H23	GND	J13	GND	K03	GND
H24	GND	J14	GND	K04	MM_M0_P_PIN_CKC_DAT_06_P
H25	TS_CT_P_PIN_M0_C_MKERF_P	J15	GND	K05	MM_M0_P_PIN_CKC_DAT_04_N
H26	GND	J16	GND	K06	MM_M0_P_PIN_CKC_DAT_03_P
H27	GND	J17	TS_CT_P_PIN_M0_PLL_ANATST	K07	MM_M0_P_PIN_CKC_DAT_01_N
H28	PV_CT_P_PIN_SPIVID0_SCLK	J18	TS_CT_P_PIN_M0_T_PLLHFC_MKERF_P	K08	GND
H29	PV_CT_P_PIN_SPIVID0_MOSI	J19	GND	K09	GND
H30	GND	J20	PV_PIN_P_CT_M0_TERMREF_P	K10	MM_CT_P_PIN_MB_NEST_REFCLK3_N
H31	GND	J21	PV_PIN_P_CT_M0_TERMREF_N	K11	GND
H32	GND	J22	GND	K12	MM_CT_P_PIN_MB_MEM_REFCLK3_N
H33	PE_CT_P_PIN_E0_PERST0_B	J23	GND	K13	VIO_1P10
H34	GND	J24	GND	K14	GND
H35	PE_PIN_P_E0_CK0_DAT_00_N	J25	TS_CT_P_PIN_M0_C_MKERF_N	K15	VIO_1P10
H36	PE_PIN_P_E0_CK0_DAT_00_P	J26	GND	K16	GND
H37	PE_PIN_P_E0_CK0_DAT_02_N	J27	GND	K17	VIO_1P10
H38	PE_PIN_P_E0_CK0_DAT_02_P	J28	PV_CT_P_PIN_SPIVID0_CS	K18	GND
H39	GND	J29	GND	K19	VIO_1P10
H40	GND	J30	PV_PIN_P_CT_SPIVID0_MISO	K20	GND
H41	GND	J31	GND	K21	VIO_1P10
H42	NA_A1_P_PIN_CK0_DAT_01_N	J32	PE_PIN_P_CT_E0_PRSNT1_B	K22	GND
H43	NA_A0_P_PIN_CK0_DAT_14_P	J33	PE_PIN_P_CT_E0_PRSNT0_B	K23	VIO_1P10
H44	NA_A0_P_PIN_CK0_DAT_20_N	J34	PE_CT_P_PIN_E0_PERST1_B	K24	GND
H45	NA_A0_P_PIN_CK0_DAT_12_P	J35	GND	K25	VIO_1P10
H46	GND	J36	GND	K26	GND
H47	NA_A0_P_PIN_CK0_DAT_13_N	J37	TS_CT_P_PIN_VIO_VSENSE	K27	VIO_1P10
H48	NA_A0_P_PIN_CK0_CLK_P	J38	GND	K28	GND
J01	MM_M0_P_PIN_CKC_DAT_14_P	J39	GND	K29	VIO_1P10
J02	GND	J40	GND		

Position	Net Name
K30	GND
K31	VIO_1P10
K32	GND
K33	VIO_1P10
K34	GND
K35	VIO_1P10
K36	GND
K37	TS_CT_P_PIN_VIO_VPCI_GSENSE
K38	GND
K39	GND
K40	NA_A1_P_PIN_CK0_DAT_05_N
K41	NA_A1_P_PIN_CK0_DAT_03_P
K42	NA_A1_P_PIN_CK0_DAT_02_N
K43	NA_A1_P_PIN_CK0_DAT_00_P
K44	GND
K45	NA_A0_P_PIN_CK0_DAT_22_P
K46	NA_A0_P_PIN_CK0_DAT_17_P
K47	NA_A0_P_PIN_CK0_DAT_16_N
K48	NA_A0_P_PIN_CK0_DAT_15_P
L01	GND
L02	MM_M0_P_PIN_CKC_DAT_15_N
L03	MM_M0_P_PIN_CKC_DAT_16_P
L04	GND
L05	MM_M0_P_PIN_CKC_DAT_04_P
L06	MM_M0_P_PIN_CKC_DAT_02_N
L07	MM_M0_P_PIN_CKC_DAT_01_P
L08	GND
L09	MM_CT_P_PIN_MB_NEST_REFCLK2_P
L10	MM_CT_P_PIN_MB_NEST_REFCLK3_P
L11	MM_CT_P_PIN_MB_MEM_REFCLK2_P
L12	MM_CT_P_PIN_MB_MEM_REFCLK3_P
L13	GND
L14	VIO_1P10
L15	GND
L16	VIO_1P10
L17	GND

Position	Net Name
L18	VIO_1P10
L19	GND
L20	VIO_1P10
L21	GND
L22	VIO_1P10
L23	GND
L24	VIO_1P10
L25	GND
L26	VIO_1P10
L27	GND
L28	VIO_1P10
L29	GND
L30	VIO_1P10
L31	GND
L32	VIO_1P10
L33	GND
L34	VIO_1P10
L35	VPCI_1P20
L36	VIO_1P10
L37	TS_CT_P_PIN_VPCI0_VSENSE
L38	GND
L39	NA_A1_P_PIN_CK0_DAT_08_N
L40	NA_A1_P_PIN_CK0_DAT_05_P
L41	NA_A1_P_PIN_CK0_DAT_06_N
L42	NA_A1_P_PIN_CK0_DAT_02_P
L43	GND
L44	NA_A1_P_PIN_CK0_DAT_04_N
L45	NA_A0_P_PIN_CK0_DAT_22_N
L46	NA_A0_P_PIN_CK0_DAT_19_N
L47	NA_A0_P_PIN_CK0_DAT_16_P
L48	GND
M01	MM_M0_P_PIN_CKD_DAT_16_P
M02	GND
M03	MM_M0_P_PIN_CKC_DAT_16_N
M04	MM_M0_P_PIN_CKC_DAT_13_N
M05	GND
M06	MM_M0_P_PIN_CKC_DAT_02_P
M07	MM_M0_P_PIN_CKC_DAT_00_N

Position	Net Name
M08	GND
M09	MM_CT_P_PIN_MB_NEST_REFCLK2_N
M10	GND
M11	MM_CT_P_PIN_MB_MEM_REFCLK2_N
M12	GND
M13	VIO_1P10
M14	GND
M15	VDD_0P89
M16	GND
M17	VDD_0P89
M18	GND
M19	VDD_0P89
M20	TS_CT_P_PIN_VCSCORE0_VSENSE
M21	VDD_0P89
M22	GND
M23	VDD_0P89
M24	TS_CT_P_PIN_GDECO0_GSENSE
M25	VIO_1P10
M26	GND
M27	VDD_0P89
M28	GND
M29	VDD_0P89
M30	GND
M31	VDD_0P89
M32	GND
M33	VDD_0P89
M34	GND
M35	VIO_1P10
M36	VPCI_1P20
M37	PV_PIN_P_CT_E0_TERMREF_P
M38	GND
M39	NA_A1_P_PIN_CK0_DAT_08_P
M40	NA_A1_P_PIN_CK0_DAT_10_N
M41	NA_A1_P_PIN_CK0_DAT_06_P
M42	GND
M43	NA_A1_P_PIN_CK0_DAT_07_N

Position	Net Name
M44	NA_A1_P_PIN_CK0_DAT_04_P
M45	NA_A0_P_PIN_CK0_DAT_21_N
M46	NA_A0_P_PIN_CK0_DAT_19_P
M47	GND
M48	NA_A0_P_PIN_CK0_DAT_18_N
N01	MM_M0_P_PIN_CKD_DAT_16_N
N02	MM_M0_P_PIN_CKD_DAT_14_P
N03	GND
N04	MM_M0_P_PIN_CKC_DAT_13_P
N05	MM_M0_P_PIN_CKD_DAT_15_P
N06	GND
N07	MM_M0_P_PIN_CKC_DAT_00_P
N08	GND
N09	GND
N10	PV_CT_M_PIN_SEEPROM1_CLK
N11	GND
N12	GND
N13	GND
N14	VDD_0P89
N15	GND
N16	VDD_0P89
N17	GND
N18	TS_CT_P_PIN_DTS2_MONI
N19	VCS_0P97
N20	TS_CT_P_PIN_GDSCORE0_GSENSE
N21	GND
N22	VCS_0P97
N23	TS_CT_P_PIN_VDDECO0_VSENSE
N24	TS_CT_P_PIN_VCSECO0_VSENSE
N25	GND
N26	VDD_0P89
N27	VCS_0P97
N28	VDD_0P89
N29	GND
N30	VCS_0P97
N31	GND
N32	VDD_0P89

Position	Net Name
N33	GND
N34	VDD_0P89
N35	VPCI_1P20
N36	GND
N37	PV_PIN_P_CT_E0_TERMREF_N
N38	GND
N39	GND
N40	NA_A1_P_PIN_CK0_DAT_10_P
N41	GND
N42	NA_A1_P_PIN_CK0_DAT_09_N
N43	NA_A1_P_PIN_CK0_DAT_07_P
N44	NA_A1_P_PIN_CK0_DAT_11_N
N45	NA_A0_P_PIN_CK0_DAT_21_P
N46	GND
N47	NA_A2_P_PIN_CK0_DAT_03_N
N48	NA_A0_P_PIN_CK0_DAT_18_P
P01	MM_M0_P_PIN_CKD_DAT_10_P
P02	MM_M0_P_PIN_CKD_DAT_14_N
P03	MM_M0_P_PIN_CKD_DAT_13_P
P04	GND
P05	MM_M0_P_PIN_CKD_DAT_15_N
P06	MM_M0_P_PIN_CKD_DAT_06_N
P07	GND
P08	MM_M0_P_PIN_CKD_DAT_01_N
P09	GND
P10	PV_CT_M_PIN_SEEPROM1_DATA
P11	MM_PIN_P_CT_M0_FAULT_D_N
P12	TS_PIN_P_CT_EXT_TRIGGER_TCK
P13	VIO_1P10
P14	GND
P15	VDD_0P89
P16	GND
P17	VDD_0P89
P18	GND
P19	VDD_0P89
P20	GND
P21	VDD_0P89

Position	Net Name
P22	GND
P23	VDD_0P89
P24	VIO_1P10
P25	VDD_0P89
P26	GND
P27	VDD_0P89
P28	GND
P29	VDD_0P89
P30	GND
P31	VDD_0P89
P32	GND
P33	VDD_0P89
P34	GND
P35	VIO_1P10
P36	VPCI_1P20
P37	TS_CT_P_PIN_PE0_PLL_ANATST
P38	TS_CT_P_PIN_A_PLLHFC_MKERF_N
P39	GND
P40	GND
P41	NA_A1_P_PIN_CK0_DAT_12_N
P42	NA_A1_P_PIN_CK0_DAT_09_P
P43	NA_A1_P_PIN_CK0_CLK_N
P44	NA_A1_P_PIN_CK0_DAT_11_P
P45	GND
P46	NA_A2_P_PIN_CK0_DAT_02_N
P47	NA_A2_P_PIN_CK0_DAT_03_P
P48	NA_A2_P_PIN_CK0_DAT_05_N
R01	MM_M0_P_PIN_CKD_DAT_10_N
R02	MM_M0_P_PIN_CKD_DAT_12_P
R03	MM_M0_P_PIN_CKD_DAT_13_N
R04	MM_M0_P_PIN_CKD_DAT_11_P
R05	GND
R06	MM_M0_P_PIN_CKD_DAT_06_P
R07	MM_M0_P_PIN_CKD_DAT_03_N
R08	MM_M0_P_PIN_CKD_DAT_01_P
R09	MM_M0_P_PIN_CKD_DAT_00_N
R10	GND
R11	GND

Position	Net Name
R12	GND
R13	GND
R14	TS_CT_P_PIN_VDDCORE0_VSENSE
R15	GND
R16	VDD_0P89
R17	GND
R18	VDD_0P89
R19	VCS_0P97
R20	VDD_0P89
R21	GND
R22	VCS_0P97
R23	GND
R24	VDD_0P89
R25	GND
R26	VDD_0P89
R27	VCS_0P97
R28	VDD_0P89
R29	GND
R30	VCS_0P97
R31	GND
R32	VDD_0P89
R33	GND
R34	VDD_0P89
R35	VPCI_1P20
R36	GND
R37	GND
R38	TS_CT_P_PIN_A_PLLHFC_MKERF_P
R39	GND
R40	NA_A1_P_PIN_CK0_DAT_13_N
R41	NA_A1_P_PIN_CK0_DAT_12_P
R42	NA_A1_P_PIN_CK0_DAT_15_N
R43	NA_A1_P_PIN_CK0_CLK_P
R44	GND
R45	NA_A2_P_PIN_CK0_DAT_01_N
R46	NA_A2_P_PIN_CK0_DAT_02_P
R47	NA_A2_P_PIN_CK0_DAT_06_N
R48	NA_A2_P_PIN_CK0_DAT_05_P

Position	Net Name
T01	GND
T02	MM_M0_P_PIN_CKD_DAT_12_N
T03	MM_M0_P_PIN_CKD_DAT_09_P
T04	MM_M0_P_PIN_CKD_DAT_11_N
T05	MM_M0_P_PIN_CKD_DAT_08_P
T06	GND
T07	MM_M0_P_PIN_CKD_DAT_03_P
T08	MM_M0_P_PIN_CKD_DAT_02_N
T09	MM_M0_P_PIN_CKD_DAT_00_P
T10	GND
T11	PV_PIN_P_CT_OSC0_C1_REFCLK_P
T12	PV_PIN_P_CT_OSC0_C1_REFCLK_N
T13	VIO_1P10
T14	TS_CT_P_PIN_GDDCORE0_GSENSE
T15	VDD_0P89
T16	GND
T17	VDD_0P89
T18	GND
T19	VDD_0P89
T20	GND
T21	VDD_0P89
T22	GND
T23	VDD_0P89
T24	TS_CT_P_PIN_EX0_GSENSE
T25	VIO_1P10
T26	GND
T27	VDD_0P89
T28	GND
T29	VDD_0P89
T30	GND
T31	VDD_0P89
T32	GND
T33	VDD_0P89
T34	GND
T35	VIO_1P10
T36	VPCI_1P20
T37	TS_CT_P_PIN_A_PLL_ANATST

Position	Net Name
T38	GND
T39	NA_A1_P_PIN_CK0_DAT_14_N
T40	NA_A1_P_PIN_CK0_DAT_13_P
T41	NA_A1_P_PIN_CK0_DAT_18_N
T42	NA_A1_P_PIN_CK0_DAT_15_P
T43	GND
T44	NA_A2_P_PIN_CK0_DAT_00_N
T45	NA_A2_P_PIN_CK0_DAT_01_P
T46	NA_A2_P_PIN_CK0_DAT_04_N
T47	NA_A2_P_PIN_CK0_DAT_06_P
T48	GND
U01	MM_M0_P_PIN_CKD_DAT_07_N
U02	GND
U03	MM_M0_P_PIN_CKD_DAT_09_N
U04	MM_M0_P_PIN_CKD_CLK_N
U05	MM_M0_P_PIN_CKD_DAT_08_N
U06	MM_M0_P_PIN_CKD_DAT_05_N
U07	GND
U08	MM_M0_P_PIN_CKD_DAT_02_P
U09	GND
U10	GND
U11	GND
U12	GND
U13	GND
U14	VDD_0P89
U15	GND
U16	VDD_0P89
U17	GND
U18	VDD_0P89
U19	GND
U20	VDD_0P89
U21	GND
U22	VDD_0P89
U23	TS_CT_P_PIN_VCSEX0_VSENSE
U24	TS_CT_P_PIN_VDDEX0_VSENSE
U25	GND
U26	VDD_0P89
U27	GND

Position	Net Name	Position	Net Name	Position	Net Name
U28	VDD_0P89	V18	GND	W08	GND
U29	GND	V19	VCS_0P97	W09	GND
U30	VDD_0P89	V20	GND	W10	GND
U31	GND	V21	VDD_0P89	W11	NC_VDD
U32	VDD_0P89	V22	VCS_0P97	W12	NC_VDD
U33	GND	V23	VDD_0P89	W13	GND
U34	VDD_0P89	V24	VIO_1P10	W14	VDD_0P89
U35	GND	V25	VDD_0P89	W15	GND
U36	VIO_1P10	V26	GND	W16	VDD_0P89
U37	GND	V27	VCS_0P97	W17	GND
U38	PV_PIN_P_CT_A_TERMREF_P	V28	GND	W18	VDD_0P89
U39	NA_A1_P_PIN_CK0_DAT_14_P	V29	VDD_0P89	W19	GND
U40	NA_A1_P_PIN_CK0_DAT_17_N	V30	VCS_0P97	W20	VDD_0P89
U41	NA_A1_P_PIN_CK0_DAT_18_P	V31	VDD_0P89	W21	GND
U42	GND	V32	GND	W22	VDD_0P89
U43	NA_A1_P_PIN_CK0_DAT_20_N	V33	VDD_0P89	W23	GND
U44	NA_A2_P_PIN_CK0_DAT_00_P	V34	GND	W24	VDD_0P89
U45	NA_A2_P_PIN_CK0_DAT_07_N	V35	GND	W25	GND
U46	NA_A2_P_PIN_CK0_DAT_04_P	V36	VIO_1P10	W26	VDD_0P89
U47	GND	V37	PV_PIN_P_CT_SPIADC_MISO	W27	GND
U48	NA_A2_P_PIN_CK0_DAT_08_N	V38	PV_PIN_P_CT_A_TERMREF_N	W28	VDD_0P89
V01	MM_M0_P_PIN_CKD_DAT_07_P	V39	NA_A1_P_PIN_CK0_DAT_16_N	W29	GND
V02	GND	V40	NA_A1_P_PIN_CK0_DAT_17_P	W30	VDD_0P89
V03	GND	V41	GND	W31	GND
V04	MM_M0_P_PIN_CKD_CLK_P	V42	NA_A1_P_PIN_CK0_DAT_22_N	W32	VDD_0P89
V05	GND	V43	NA_A1_P_PIN_CK0_DAT_20_P	W33	GND
V06	MM_M0_P_PIN_CKD_DAT_05_P	V44	NA_A2_P_PIN_CK0_DAT_09_N	W34	VDD_0P89
V07	MM_M0_P_PIN_CKD_DAT_04_N	V45	NA_A2_P_PIN_CK0_DAT_07_P	W35	VIO_1P10
V08	GND	V46	GND	W36	GND
V09	MM_PIN_P_CT_M0_FAULT_C_N	V47	NA_A2_P_PIN_CK0_DAT_10_N	W37	GND
V10	PV_PIN_P_CT_OSC0_TODREFCLK	V48	NA_A2_P_PIN_CK0_DAT_08_P	W38	GND
V11	GND	W01	GND	W39	NA_A1_P_PIN_CK0_DAT_16_P
V12	NC_VDD	W02	GND	W40	GND
V13	VIO_1P10	W03	GND	W41	NA_A1_P_PIN_CK0_DAT_19_N
V14	GND	W04	GND	W42	NA_A1_P_PIN_CK0_DAT_22_P
V15	VDD_0P89	W05	GND	W43	NA_A2_P_PIN_CK0_DAT_13_N
V16	GND	W06	GND	W44	NA_A2_P_PIN_CK0_DAT_09_P
V17	VDD_0P89	W07	MM_M0_P_PIN_CKD_DAT_04_P	W45	GND

Position	Net Name	Position	Net Name	Position	Net Name
W46	NA_A2_P_PIN_CK0_DAT_11_N	Y36	VIO_1P10	AA26	VDD_0P89
W47	NA_A2_P_PIN_CK0_DAT_10_P	Y37	PV_CT_P_PIN_SPIADC_MOSI	AA27	GND
W48	NA_A2_P_PIN_CK0_CLK_N	Y38	GND	AA28	VDD_0P89
Y01	NC_VDD	Y39	GND	AA29	GND
Y02	NC_VDD	Y40	GND	AA30	VDD_0P89
Y03	NC_VDD	Y41	NA_A1_P_PIN_CK0_DAT_19_P	AA31	GND
Y04	NC_VDD	Y42	NA_A1_P_PIN_CK0_DAT_21_N	AA32	VDD_0P89
Y05	NC_VDD	Y43	NA_A2_P_PIN_CK0_DAT_13_P	AA33	GND
Y06	NC_VDD	Y44	GND	AA34	VDD_0P89
Y07	GND	Y45	NA_A2_P_PIN_CK0_DAT_16_N	AA35	VIO_1P10
Y08	GND	Y46	NA_A2_P_PIN_CK0_DAT_11_P	AA36	GND
Y09	NC_VDD	Y47	NA_A2_P_PIN_CK0_DAT_12_N	AA37	PV_CT_P_PIN_SPIADC_CS1
Y10	NC_VDD	Y48	NA_A2_P_PIN_CK0_CLK_P	AA38	PV_CT_P_PIN_SPIADC_CS0
Y11	NC_VDD	AA01	NC_VDD	AA39	PV_CT_P_PIN_SPIADC_SCLK
Y12	NC_VDD	AA02	NC_VDD	AA40	GND
Y13	VIO_1P10	AA03	NC_VDD	AA41	NA_A2_P_PIN_CK0_DAT_22_N
Y14	GND	AA04	NC_VDD	AA42	NA_A1_P_PIN_CK0_DAT_21_P
Y15	VDD_0P89	AA05	NC_VDD	AA43	GND
Y16	GND	AA06	NC_VDD	AA44	NA_A2_P_PIN_CK0_DAT_18_N
Y17	VDD_0P89	AA07	NC_VDD	AA45	NA_A2_P_PIN_CK0_DAT_16_P
Y18	GND	AA08	NC_VDD	AA46	NA_A2_P_PIN_CK0_DAT_15_N
Y19	VCS_0P97	AA09	NC_VDD	AA47	NA_A2_P_PIN_CK0_DAT_12_P
Y20	GND	AA10	NC_VDD	AA48	GND
Y21	VDD_0P89	AA11	NC_VDD	AB01	NC_VDD
Y22	VCS_0P97	AA12	NC_VDD	AB02	NC_VDD
Y23	VDD_0P89	AA13	GND	AB03	NC_VDD
Y24	GND	AA14	VDD_0P89	AB04	NC_VDD
Y25	VIO_1P10	AA15	GND	AB05	NC_VDD
Y26	GND	AA16	VDD_0P89	AB06	NC_VDD
Y27	VCS_0P97	AA17	GND	AB07	NC_VDD
Y28	GND	AA18	VDD_0P89	AB08	NC_VDD
Y29	VDD_0P89	AA19	GND	AB09	NC_VDD
Y30	VCS_0P97	AA20	VDD_0P89	AB10	NC_VDD
Y31	VDD_0P89	AA21	GND	AB11	GND
Y32	GND	AA22	VDD_0P89	AB12	GND
Y33	VDD_0P89	AA23	GND	AB13	NC_VDD
Y34	GND	AA24	VDD_0P89	AB14	GND
Y35	GND	AA25	GND	AB15	VDD_0P89

Position	Net Name
AB16	GND
AB17	VDD_0P89
AB18	GND
AB19	VCS_0P97
AB20	GND
AB21	VDD_0P89
AB22	VCS_0P97
AB23	VDD_0P89
AB24	VIO_1P10
AB25	TS_CT_P_PIN_PFAMX_VSENSE
AB26	GND
AB27	VCS_0P97
AB28	GND
AB29	VDD_0P89
AB30	VCS_0P97
AB31	VDD_0P89
AB32	GND
AB33	VDD_0P89
AB34	GND
AB35	GND
AB36	VIO_1P10
AB37	GND
AB38	GND
AB39	GND
AB40	GND
AB41	NA_A2_P_PIN_CK0_DAT_22_P
AB42	GND
AB43	NA_A2_P_PIN_CK0_DAT_20_N
AB44	NA_A2_P_PIN_CK0_DAT_18_P
AB45	NA_A2_P_PIN_CK0_DAT_17_N
AB46	NA_A2_P_PIN_CK0_DAT_15_P
AB47	GND
AB48	NA_A2_P_PIN_CK0_DAT_14_N
AC01	NC_VDD
AC02	NC_VDD
AC03	NC_VDD
AC04	NC_VDD
AC05	NC_VDD

Position	Net Name
AC06	NC_VDD
AC07	NC_VDD
AC08	PV_MSOP_M_CT_VREF_N
AC09	PV_MSOP_M_CT_VREF_P
AC10	GND
AC11	DVDD_1P50
AC12	DVDD_1P50
AC13	GND
AC14	VDD_0P89
AC15	GND
AC16	VDD_0P89
AC17	GND
AC18	VDD_0P89
AC19	GND
AC20	VDD_0P89
AC21	GND
AC22	VDD_0P89
AC23	GND
AC24	TS_CT_P_PIN_VCAL
AC25	TS_CT_P_PIN_PFAMX_GSENSE
AC26	VDD_0P89
AC27	GND
AC28	VDD_0P89
AC29	GND
AC30	VDD_0P89
AC31	GND
AC32	VDD_0P89
AC33	GND
AC34	VDD_0P89
AC35	VIO_1P10
AC36	GND
AC37	PE_CT_P_PIN_E0_SLOT_CLK0_N
AC38	GND
AC39	GND
AC40	GND
AC41	GND
AC42	NA_A2_P_PIN_CK0_DAT_21_N
AC43	NA_A2_P_PIN_CK0_DAT_20_P

Position	Net Name
AC44	NA_A2_P_PIN_CK0_DAT_19_N
AC45	NA_A2_P_PIN_CK0_DAT_17_P
AC46	GND
AC47	GND
AC48	NA_A2_P_PIN_CK0_DAT_14_P
AD01	NC_VDD
AD02	NC_VDD
AD03	NC_VDD
AD04	NC_VDD
AD05	GND
AD06	GND
AD07	GND
AD08	GND
AD09	GND
AD10	GND
AD11	AVDD_1P50
AD12	AVDD_1P50
AD13	VIO_1P10
AD14	VIO_1P10
AD15	VDD_0P89
AD16	GND
AD17	VDD_0P89
AD18	VIO_1P10
AD19	VDD_0P89
AD20	GND
AD21	VDD_0P89
AD22	VIO_1P10
AD23	VDD_0P89
AD24	GND
AD25	VIO_1P10
AD26	GND
AD27	VDD_0P89
AD28	GND
AD29	VIO_1P10
AD30	GND
AD31	VDD_0P89
AD32	GND
AD33	VIO_1P10

Position	Net Name
AD34	GND
AD35	GND
AD36	VIO_1P10
AD37	PE_CT_P_PIN_E0_SLOT_CLK0_P
AD38	GND
AD39	PV_PIN_P_CT_OSC0_E_REFCLK_N
AD40	PV_PIN_P_CT_OSC0_E_REFCLK_P
AD41	GND
AD42	NA_A2_P_PIN_CK0_DAT_21_P
AD43	GND
AD44	NA_A2_P_PIN_CK0_DAT_19_P
AD45	GND
AD46	GND
AD47	GND
AD48	GND
AE01	GND
AE02	GND
AE03	GND
AE04	GND
AE05	NC_VDD
AE06	NC_VDD
AE07	NC_VDD
AE08	NC_VDD
AE09	NC_VDD
AE10	GND
AE11	GND
AE12	GND
AE13	GND
AE14	VDD_0P89
AE15	GND
AE16	VIO_1P10
AE17	GND
AE18	VDD_0P89
AE19	GND
AE20	VIO_1P10
AE21	GND
AE22	VDD_SENSE_P

Position	Net Name
AE23	VDD_SENSE_N
AE24	VIO_1P10
AE25	GND
AE26	VDD_0P89
AE27	VIO_1P10
AE28	VDD_0P89
AE29	GND
AE30	VDD_0P89
AE31	VIO_1P10
AE32	VDD_0P89
AE33	GND
AE34	VDD_0P89
AE35	VIO_1P10
AE36	GND
AE37	GND
AE38	GND
AE39	GND
AE40	GND
AE41	GND
AE42	GND
AE43	GND
AE44	GND
AE45	GND
AE46	GND
AE47	NA_PIN_P_A0_CK0_DAT_06_N
AE48	GND
AF01	NC_VDD
AF02	NC_VDD
AF03	NC_VDD
AF04	NC_VDD
AF05	NC_VDD
AF06	NC_VDD
AF07	NC_VDD
AF08	NC_VDD
AF09	NC_VDD
AF10	NC_VDD
AF11	NC_VDD
AF12	NC_VDD

Position	Net Name
AF13	NC_VDD
AF14	GND
AF15	VDD_0P89
AF16	GND
AF17	VDD_0P89
AF18	GND
AF19	VDD_0P89
AF20	GND
AF21	VDD_0P89
AF22	GND
AF23	VDD_0P89
AF24	GND
AF25	VDD_0P89
AF26	GND
AF27	VDD_0P89
AF28	GND
AF29	VDD_0P89
AF30	GND
AF31	VDD_0P89
AF32	GND
AF33	VDD_0P89
AF34	GND
AF35	GND
AF36	VIO_1P10
AF37	GND
AF38	PE_CT_P_PIN_E1_SLOT_CLK0_N
AF39	GND
AF40	NA_PIN_P_A1_CK0_DAT_00_N
AF41	GND
AF42	GND
AF43	NA_PIN_P_A0_CK0_DAT_01_P
AF44	GND
AF45	NA_PIN_P_A0_CK0_DAT_04_N
AF46	GND
AF47	NA_PIN_P_A0_CK0_DAT_06_P
AF48	NA_PIN_P_A0_CK0_DAT_10_N
AG01	NC_VDD
AG02	NC_VDD

Position	Net Name
AG03	NC_VDD
AG04	NC_VDD
AG05	NC_VDD
AG06	NC_VDD
AG07	NC_VDD
AG08	NC_VDD
AG09	NC_VDD
AG10	NC_VDD
AG11	NC_VDD
AG12	NC_VDD
AG13	GND
AG14	VDD_0P89
AG15	GND
AG16	VDD_0P89
AG17	GND
AG18	VDD_0P89
AG19	VCS_0P97
AG20	VDD_0P89
AG21	GND
AG22	VCS_SENSE_P
AG23	VCS_SENSE_N
AG24	VDD_0P89
AG25	VIO_1P10
AG26	VDD_0P89
AG27	VCS_0P97
AG28	VDD_0P89
AG29	GND
AG30	VCS_0P97
AG31	GND
AG32	VDD_0P89
AG33	GND
AG34	VDD_0P89
AG35	VIO_1P10
AG36	GND
AG37	PE_CT_P_PIN_E1_SLOT_CLK1_N
AG38	PE_CT_P_PIN_E1_SLOT_CLK0_P
AG39	GND
AG40	NA_PIN_P_A1_CK0_DAT_00_P

Position	Net Name
AG41	NA_PIN_P_A1_CK0_DAT_01_N
AG42	GND
AG43	NA_PIN_P_A0_CK0_DAT_01_N
AG44	NA_PIN_P_A0_CK0_DAT_03_N
AG45	NA_PIN_P_A0_CK0_DAT_04_P
AG46	NA_PIN_P_A0_CK0_DAT_07_N
AG47	GND
AG48	NA_PIN_P_A0_CK0_DAT_10_P
AH01	NC_VDD
AH02	NC_VDD
AH03	NC_VDD
AH04	NC_VDD
AH05	NC_VDD
AH06	NC_VDD
AH07	NC_VDD
AH08	NC_VDD
AH09	NC_VDD
AH10	NC_VDD
AH11	NC_VDD
AH12	NC_VDD
AH13	VIO_1P10
AH14	GND
AH15	VDD_0P89
AH16	GND
AH17	VDD_0P89
AH18	GND
AH19	VDD_0P89
AH20	GND
AH21	VDD_0P89
AH22	GND
AH23	VDD_0P89
AH24	GND
AH25	VDD_0P89
AH26	GND
AH27	VDD_0P89
AH28	GND
AH29	VDD_0P89
AH30	GND

Position	Net Name
AH31	VDD_0P89
AH32	GND
AH33	VDD_0P89
AH34	GND
AH35	GND
AH36	VIO_1P10
AH37	PE_CT_P_PIN_E1_SLOT_CLK1_P
AH38	GND
AH39	GND
AH40	NA_PIN_P_A1_CK0_DAT_02_N
AH41	NA_PIN_P_A1_CK0_DAT_01_P
AH42	GND
AH43	GND
AH44	NA_PIN_P_A0_CK0_DAT_03_P
AH45	NA_PIN_P_A0_CK0_DAT_05_N
AH46	NA_PIN_P_A0_CK0_DAT_07_P
AH47	NA_PIN_P_A0_CK0_DAT_09_N
AH48	GND
AJ01	NC_VDD
AJ02	NC_VDD
AJ03	NC_VDD
AJ04	NC_VDD
AJ05	NC_VDD
AJ06	NC_VDD
AJ07	GND
AJ08	VSB_3P30
AJ09	VSB_3P30
AJ10	GND
AJ11	GND
AJ12	GND
AJ13	GND
AJ14	VDD_0P89
AJ15	GND
AJ16	VDD_0P89
AJ17	GND
AJ18	VDD_0P89
AJ19	VCS_0P97
AJ20	VDD_0P89

Position	Net Name
AJ21	GND
AJ22	VCS_0P97
AJ23	GND
AJ24	VIO_1P10
AJ25	GND
AJ26	VDD_0P89
AJ27	VCS_0P97
AJ28	VDD_0P89
AJ29	GND
AJ30	VCS_0P97
AJ31	GND
AJ32	VDD_0P89
AJ33	GND
AJ34	VDD_0P89
AJ35	VIO_1P10
AJ36	GND
AJ37	GND
AJ38	TS_CT_P_PIN_A1_MKERF_N
AJ39	GND
AJ40	NA_PIN_P_A1_CK0_DAT_02_P
AJ41	NA_PIN_P_A1_CK0_DAT_03_N
AJ42	GND
AJ43	NA_PIN_P_A0_CK0_DAT_00_P
AJ44	GND
AJ45	NA_PIN_P_A0_CK0_DAT_05_P
AJ46	NA_PIN_P_A0_CK0_CLK_N
AJ47	NA_PIN_P_A0_CK0_DAT_09_P
AJ48	NA_PIN_P_A0_CK0_DAT_11_N
AK01	GND
AK02	GND
AK03	GND
AK04	GND
AK05	GND
AK06	GND
AK07	MM_M1_P_PIN_CKD_DAT_04_P
AK08	GND
AK09	TS_CT_P_PIN_PXFM_PLL_HFC_N

Position	Net Name
AK10	TS_CT_P_PIN_PXFM_PLL_HFC_P
AK11	GND
AK12	PV_CT_P_PIN_PSI_CLK_P
AK13	VIO_1P10
AK14	GND
AK15	VDD_0P89
AK16	GND
AK17	VDD_0P89
AK18	GND
AK19	VDD_0P89
AK20	GND
AK21	VDD_0P89
AK22	GND
AK23	VDD_0P89
AK24	GND
AK25	VDD_0P89
AK26	GND
AK27	VDD_0P89
AK28	GND
AK29	VDD_0P89
AK30	GND
AK31	VDD_0P89
AK32	GND
AK33	VDD_0P89
AK34	GND
AK35	GND
AK36	VIO_1P10
AK37	GND
AK38	TS_CT_P_PIN_A1_MKERF_P
AK39	NA_PIN_P_A1_CK0_DAT_04_N
AK40	GND
AK41	NA_PIN_P_A1_CK0_DAT_03_P
AK42	GND
AK43	NA_PIN_P_A0_CK0_DAT_00_N
AK44	NA_PIN_P_A0_CK0_DAT_08_N
AK45	GND
AK46	NA_PIN_P_A0_CK0_CLK_P
AK47	NA_PIN_P_A0_CK0_DAT_12_N

Position	Net Name
AK48	NA_PIN_P_A0_CK0_DAT_11_P
AL01	MM_M1_P_PIN_CKD_DAT_07_P
AL02	GND
AL03	GND
AL04	MM_M1_P_PIN_CKD_CLK_P
AL05	GND
AL06	MM_M1_P_PIN_CKD_DAT_05_P
AL07	MM_M1_P_PIN_CKD_DAT_04_N
AL08	GND
AL09	MM_PIN_P_CT_M1_FAULT_C_N
AL10	GND
AL11	PV_CT_P_PIN_PSI_DATA
AL12	PV_CT_P_PIN_PSI_CLK_N
AL13	GND
AL14	VDD_0P89
AL15	GND
AL16	VDD_0P89
AL17	TS_CT_P_PIN_TDIODE_C5
AL18	TS_CT_P_PIN_TDIODE_A5
AL19	VCS_0P97
AL20	VDD_0P89
AL21	GND
AL22	VCS_0P97
AL23	GND
AL24	VDD_0P89
AL25	VIO_1P10
AL26	VDD_0P89
AL27	VCS_0P97
AL28	VDD_0P89
AL29	GND
AL30	VCS_0P97
AL31	TS_CT_P_PIN_TDIODE_A13
AL32	TS_CT_P_PIN_TDIODE_C13
AL33	GND
AL34	VDD_0P89
AL35	VIO_1P10
AL36	GND
AL37	PV_CT_B_PIN_PCI_I2C_SDA_B

Position	Net Name	Position	Net Name	Position	Net Name
AL38	GND	AM28	GND	AN18	VDD_0P89
AL39	NA_PIN_P_A1_CK0_DAT_04_P	AM29	VDD_0P89	AN19	GND
AL40	NA_PIN_P_A1_CK0_DAT_05_N	AM30	GND	AN20	VDD_0P89
AL41	GND	AM31	VDD_0P89	AN21	GND
AL42	GND	AM32	GND	AN22	VDD_0P89
AL43	NA_PIN_P_A0_CK0_DAT_02_P	AM33	VDD_0P89	AN23	GND
AL44	NA_PIN_P_A0_CK0_DAT_08_P	AM34	GND	AN24	VIO_1P10
AL45	NA_PIN_P_A0_CK0_DAT_13_N	AM35	GND	AN25	TS_CT_P_PIN_AMX1_VSENSE
AL46	GND	AM36	VIO_1P10	AN26	VDD_0P89
AL47	NA_PIN_P_A0_CK0_DAT_12_P	AM37	PV_CT_B_PIN_PCI_I2C_SCL_B	AN27	GND
AL48	NA_PIN_P_A0_CK0_DAT_14_N	AM38	GND	AN28	VDD_0P89
AM01	MM_M1_P_PIN_CKD_DAT_07_N	AM39	NA_PIN_P_A1_CK0_DAT_06_N	AN29	GND
AM02	GND	AM40	NA_PIN_P_A1_CK0_DAT_05_P	AN30	VDD_0P89
AM03	MM_M1_P_PIN_CKD_DAT_09_N	AM41	NA_PIN_P_A1_CK0_DAT_07_N	AN31	GND
AM04	MM_M1_P_PIN_CKD_CLK_N	AM42	GND	AN32	VDD_0P89
AM05	MM_M1_P_PIN_CKD_DAT_08_N	AM43	NA_PIN_P_A0_CK0_DAT_02_N	AN33	GND
AM06	MM_M1_P_PIN_CKD_DAT_05_N	AM44	NA_PIN_P_A0_CK0_DAT_15_N	AN34	VDD_0P89
AM07	GND	AM45	NA_PIN_P_A0_CK0_DAT_13_P	AN35	VIO_1P10
AM08	MM_M1_P_PIN_CKD_DAT_02_P	AM46	NA_PIN_P_A0_CK0_DAT_18_N	AN36	VPCI_1P20
AM09	GND	AM47	GND	AN37	GND
AM10	MM_PIN_P_CT_M1_FAULT_D_N	AM48	NA_PIN_P_A0_CK0_DAT_14_P	AN38	GND
AM11	GND	AN01	GND	AN39	NA_PIN_P_A1_CK0_DAT_06_P
AM12	GND	AN02	MM_M1_P_PIN_CKD_DAT_12_N	AN40	NA_PIN_P_A1_CK0_DAT_08_N
AM13	VIO_1P10	AN03	MM_M1_P_PIN_CKD_DAT_09_P	AN41	NA_PIN_P_A1_CK0_DAT_07_P
AM14	GND	AN04	MM_M1_P_PIN_CKD_DAT_11_N	AN42	NA_PIN_P_A1_CK0_DAT_09_N
AM15	VDD_0P89	AN05	MM_M1_P_PIN_CKD_DAT_08_P	AN43	GND
AM16	GND	AN06	GND	AN44	NA_PIN_P_A0_CK0_DAT_15_P
AM17	VDD_0P89	AN07	MM_M1_P_PIN_CKD_DAT_03_P	AN45	NA_PIN_P_A0_CK0_DAT_22_N
AM18	GND	AN08	MM_M1_P_PIN_CKD_DAT_02_N	AN46	NA_PIN_P_A0_CK0_DAT_18_P
AM19	VDD_0P89	AN09	MM_M1_P_PIN_CKD_DAT_00_P	AN47	NA_PIN_P_A0_CK0_DAT_16_N
AM20	GND	AN10	GND	AN48	GND
AM21	VDD_0P89	AN11	PV_PIN_P_CT_PSI_DATA	AP01	MM_M1_P_PIN_CKD_DAT_10_N
AM22	GND	AN12	PV_PIN_P_CT_PSI_CLK_N	AP02	MM_M1_P_PIN_CKD_DAT_12_P
AM23	VDD_0P89	AN13	GND	AP03	MM_M1_P_PIN_CKD_DAT_13_N
AM24	GND	AN14	VDD_0P89	AP04	MM_M1_P_PIN_CKD_DAT_11_P
AM25	TS_CT_P_PIN_AMX1_GSENSE	AN15	GND	AP05	GND
AM26	GND	AN16	VDD_0P89	AP06	MM_M1_P_PIN_CKD_DAT_06_P
AM27	VDD_0P89	AN17	GND	AP07	MM_M1_P_PIN_CKD_DAT_03_N

Position	Net Name
AP08	MM_M1_P_PIN_CKD_DAT_01_P
AP09	MM_M1_P_PIN_CKD_DAT_00_N
AP10	TS_CT_P_PIN_PXFM_PLL_ANATST
AP11	GND
AP12	PV_PIN_P_CT_PSI_CLK_P
AP13	VIO_1P10
AP14	GND
AP15	VDD_0P89
AP16	GND
AP17	VDD_0P89
AP18	GND
AP19	VCS_0P97
AP20	GND
AP21	VDD_0P89
AP22	VCS_0P97
AP23	VDD_0P89
AP24	GND
AP25	TS_PIN_P_CT_EFUSE_FSOURCE
AP26	GND
AP27	VCS_0P97
AP28	GND
AP29	VDD_0P89
AP30	VCS_0P97
AP31	VDD_0P89
AP32	GND
AP33	VDD_0P89
AP34	GND
AP35	VPCI_1P20
AP36	GND
AP37	GND
AP38	GND
AP39	GND
AP40	NA_PIN_P_A1_CK0_DAT_08_P
AP41	NA_PIN_P_A1_CK0_DAT_10_N
AP42	NA_PIN_P_A1_CK0_DAT_09_P
AP43	NA_PIN_P_A1_CK0_DAT_11_N
AP44	GND

Position	Net Name
AP45	NA_PIN_P_A0_CK0_DAT_22_P
AP46	NA_PIN_P_A0_CK0_DAT_20_N
AP47	NA_PIN_P_A0_CK0_DAT_16_P
AP48	NA_PIN_P_A0_CK0_DAT_17_N
AR01	MM_M1_P_PIN_CKD_DAT_10_P
AR02	MM_M1_P_PIN_CKD_DAT_14_N
AR03	MM_M1_P_PIN_CKD_DAT_13_P
AR04	GND
AR05	MM_M1_P_PIN_CKD_DAT_15_N
AR06	MM_M1_P_PIN_CKD_DAT_06_N
AR07	GND
AR08	MM_M1_P_PIN_CKD_DAT_01_N
AR09	GND
AR10	PV_PIN_P_CT_TPM_INTERRUPT
AR11	TS_PIN_P_CT_TST_FORCE_PWR_ON
AR12	GND
AR13	GND
AR14	VDD_0P89
AR15	GND
AR16	VDD_0P89
AR17	GND
AR18	VDD_0P89
AR19	GND
AR20	VDD_0P89
AR21	GND
AR22	VDD_0P89
AR23	GND
AR24	VDD_0P89
AR25	VIO_1P10
AR26	VDD_0P89
AR27	GND
AR28	VDD_0P89
AR29	GND
AR30	VDD_0P89
AR31	GND
AR32	VDD_0P89
AR33	GND
AR34	VDD_0P89

Position	Net Name
AR35	VIO_1P10
AR36	VPCI_1P20
AR37	TS_CT_P_PIN_PE1_PLL_ANATST
AR38	PV_PIN_P_CT_E1_TERMREF_N
AR39	NA_PIN_P_A2_CK0_DAT_00_N
AR40	GND
AR41	NA_PIN_P_A1_CK0_DAT_10_P
AR42	NA_PIN_P_A1_CK0_CLK_N
AR43	NA_PIN_P_A1_CK0_DAT_11_P
AR44	NA_PIN_P_A1_CK0_DAT_13_N
AR45	GND
AR46	NA_PIN_P_A0_CK0_DAT_20_P
AR47	NA_PIN_P_A0_CK0_DAT_19_N
AR48	NA_PIN_P_A0_CK0_DAT_17_P
AT01	MM_M1_P_PIN_CKD_DAT_16_N
AT02	MM_M1_P_PIN_CKD_DAT_14_P
AT03	GND
AT04	MM_M1_P_PIN_CKC_DAT_13_P
AT05	MM_M1_P_PIN_CKD_DAT_15_P
AT06	GND
AT07	MM_M1_P_PIN_CKC_DAT_00_P
AT08	GND
AT09	GND
AT10	PV_CT_P_PIN_TPM_RESET
AT11	GND
AT12	MM_CT_P_PIN_MB_MEM_REFCLK7_P
AT13	VIO_1P10
AT14	GND
AT15	VDD_0P89
AT16	GND
AT17	VDD_0P89
AT18	GND
AT19	VCS_0P97
AT20	GND
AT21	VDD_0P89
AT22	VCS_0P97
AT23	VDD_0P89
AT24	GND

Position	Net Name
AT25	VDD_0P89
AT26	GND
AT27	VCS_0P97
AT28	GND
AT29	VDD_0P89
AT30	VCS_0P97
AT31	VDD_0P89
AT32	GND
AT33	VDD_0P89
AT34	GND
AT35	VPCI_1P20
AT36	GND
AT37	GND
AT38	PV_PIN_P_CT_E1_TERMREF_P
AT39	NA_PIN_P_A2_CK0_DAT_00_P
AT40	NA_PIN_P_A2_CK0_DAT_02_N
AT41	GND
AT42	NA_PIN_P_A1_CK0_CLK_P
AT43	NA_PIN_P_A1_CK0_DAT_12_N
AT44	NA_PIN_P_A1_CK0_DAT_13_P
AT45	NA_PIN_P_A1_CK0_DAT_15_N
AT46	GND
AT47	NA_PIN_P_A0_CK0_DAT_19_P
AT48	NA_PIN_P_A0_CK0_DAT_21_N
AU01	MM_M1_P_PIN_CKD_DAT_16_P
AU02	GND
AU03	MM_M1_P_PIN_CKC_DAT_16_N
AU04	MM_M1_P_PIN_CKC_DAT_13_N
AU05	GND
AU06	MM_M1_P_PIN_CKC_DAT_02_P
AU07	MM_M1_P_PIN_CKC_DAT_00_N
AU08	GND
AU09	MM_CT_P_PIN_MB_NEST_ REFCLK6_P
AU10	GND
AU11	MM_CT_P_PIN_MB_MEM_ REFCLK6_N
AU12	MM_CT_P_PIN_MB_MEM_ REFCLK7_N
AU13	GND

Position	Net Name
AU14	VDD_0P89
AU15	GND
AU16	VDD_0P89
AU17	GND
AU18	VDD_0P89
AU19	GND
AU20	VDD_0P89
AU21	GND
AU22	VDD_0P89
AU23	GND
AU24	VIO_1P10
AU25	GND
AU26	VDD_0P89
AU27	GND
AU28	VDD_0P89
AU29	GND
AU30	VDD_0P89
AU31	GND
AU32	VDD_0P89
AU33	GND
AU34	VDD_0P89
AU35	VIO_1P10
AU36	VPCI_1P20
AU37	PE_CT_P_PIN_E1_PERST1_B
AU38	GND
AU39	NA_PIN_P_A2_CK0_DAT_01_N
AU40	NA_PIN_P_A2_CK0_DAT_02_P
AU41	NA_PIN_P_A2_CK0_DAT_04_N
AU42	GND
AU43	NA_PIN_P_A1_CK0_DAT_12_P
AU44	NA_PIN_P_A1_CK0_DAT_14_N
AU45	NA_PIN_P_A1_CK0_DAT_15_P
AU46	NA_PIN_P_A1_CK0_DAT_17_N
AU47	GND
AU48	NA_PIN_P_A0_CK0_DAT_21_P
AV01	GND
AV02	MM_M1_P_PIN_CKC_DAT_15_N
AV03	MM_M1_P_PIN_CKC_DAT_16_P

Position	Net Name
AV04	GND
AV05	MM_M1_P_PIN_CKC_DAT_04_P
AV06	MM_M1_P_PIN_CKC_DAT_02_N
AV07	MM_M1_P_PIN_CKC_DAT_01_P
AV08	GND
AV09	MM_CT_P_PIN_MB_NEST_ REFCLK6_N
AV10	MM_CT_P_PIN_MB_NEST_ REFCLK7_P
AV11	MM_CT_P_PIN_MB_MEM_ REFCLK6_P
AV12	GND
AV13	VIO_1P10
AV14	GND
AV15	VIO_1P10
AV16	GND
AV17	VIO_1P10
AV18	GND
AV19	VIO_1P10
AV20	GND
AV21	VIO_1P10
AV22	GND
AV23	VIO_1P10
AV24	GND
AV25	VIO_1P10
AV26	GND
AV27	VIO_1P10
AV28	GND
AV29	VIO_1P10
AV30	GND
AV31	VSB_1P20
AV32	GND
AV33	VSB_1P20
AV34	GND
AV35	VPCI_1P20
AV36	GND
AV37	PE_CT_P_PIN_E1_PERST0_B
AV38	GND
AV39	NA_PIN_P_A2_CK0_DAT_01_P
AV40	NA_PIN_P_A2_CK0_DAT_03_N

Position	Net Name
AV41	NA_PIN_P_A2_CK0_DAT_04_P
AV42	NA_PIN_P_A2_CK0_DAT_06_N
AV43	GND
AV44	NA_PIN_P_A1_CK0_DAT_14_P
AV45	NA_PIN_P_A1_CK0_DAT_16_N
AV46	NA_PIN_P_A1_CK0_DAT_17_P
AV47	NA_PIN_P_A1_CK0_DAT_19_N
AV48	GND
AW01	MM_M1_P_PIN_CKC_DAT_14_N
AW02	MM_M1_P_PIN_CKC_DAT_15_P
AW03	GND
AW04	MM_M1_P_PIN_CKC_DAT_06_P
AW05	MM_M1_P_PIN_CKC_DAT_04_N
AW06	MM_M1_P_PIN_CKC_DAT_03_P
AW07	MM_M1_P_PIN_CKC_DAT_01_N
AW08	GND
AW09	GND
AW10	MM_CT_P_PIN_MB_NEST_REFCLK7_N
AW11	GND
AW12	SH_PIN_P_M1_CKB_DAT_03_P
AW13	GND
AW14	VIO_1P10
AW15	GND
AW16	VIO_1P10
AW17	GND
AW18	VIO_1P10
AW19	GND
AW20	VIO_1P10
AW21	GND
AW22	VIO_1P10
AW23	GND
AW24	VIO_1P10
AW25	GND
AW26	PV_PIN_P_CT_VIO_PGOOD
AW27	GND
AW28	VIO_1P10
AW29	GND
AW30	VIO_1P10

Position	Net Name
AW31	PV_CT_B_PIN_LPC_DATA_03
AW32	PV_CT_B_PIN_LPC_DATA_01
AW33	PV_CT_P_PIN_LPC_FRAME_B
AW34	PV_PIN_P_CT_LPC_RESET_B
AW35	VIO_1P10
AW36	PV_PIN_P_CT_LPC_CLK
AW37	GND
AW38	SH_CT_P_PIN_MB_FSI1_CLK
AW39	GND
AW40	NA_PIN_P_A2_CK0_DAT_03_P
AW41	NA_PIN_P_A2_CK0_DAT_05_N
AW42	NA_PIN_P_A2_CK0_DAT_06_P
AW43	NA_PIN_P_A2_CK0_DAT_08_N
AW44	GND
AW45	NA_PIN_P_A1_CK0_DAT_16_P
AW46	NA_PIN_P_A1_CK0_DAT_18_N
AW47	NA_PIN_P_A1_CK0_DAT_19_P
AW48	NA_PIN_P_A1_CK0_DAT_21_N
AY01	MM_M1_P_PIN_CKC_DAT_14_P
AY02	GND
AY03	MM_M1_P_PIN_CKC_DAT_08_N
AY04	MM_M1_P_PIN_CKC_DAT_06_N
AY05	MM_M1_P_PIN_CKC_DAT_05_P
AY06	MM_M1_P_PIN_CKC_DAT_03_N
AY07	GND
AY08	PV_CT_M_PIN_SEEPROM0_CLK
AY09	SH_PIN_P_M1_CKB_DAT_12_P
AY10	GND
AY11	GND
AY12	SH_PIN_P_M1_CKB_DAT_14_P
AY13	SH_PIN_P_M1_CKB_DAT_10_P
AY14	GND
AY15	SH_PIN_P_M1_CKB_DAT_01_P
AY16	TS_CT_P_PIN_PROBE2
AY17	TS_CT_P_PIN_PROBE4
AY18	TS_CT_P_PIN_M1_PLL_ANATST
AY19	GND
AY20	TS_CT_P_PIN_PROBE3

Position	Net Name
AY21	PV_CT_P_PIN_SPARE0
AY22	GND
AY23	MM_CT_P_PIN_MB_FSI3_CLK
AY24	MM_CT_B_PIN_MB_FSI3_DATA
AY25	GND
AY26	PV_CT_B_PIN_LP_I2C_SCL_B
AY27	PV_CT_B_PIN_LP_I2C_SDA_B
AY28	GND
AY29	TS_CT_P_PIN_PROBE0_P
AY30	TS_CT_P_PIN_PROBE0_N
AY31	GND
AY32	PV_CT_B_PIN_LPC_DATA_02
AY33	PV_CT_B_PIN_LPC_DATA_00
AY34	GND
AY35	PE_PIN_P_CT_E1_PRSNT0_B
AY36	GND
AY37	GND
AY38	GND
AY39	SH_CT_B_PIN_MB_FSI1_DATA
AY40	GND
AY41	NA_PIN_P_A2_CK0_DAT_05_P
AY42	NA_PIN_P_A2_CK0_DAT_07_N
AY43	NA_PIN_P_A2_CK0_DAT_08_P
AY44	NA_PIN_P_A2_CK0_DAT_10_N
AY45	GND
AY46	NA_PIN_P_A1_CK0_DAT_18_P
AY47	NA_PIN_P_A1_CK0_DAT_20_N
AY48	NA_PIN_P_A1_CK0_DAT_21_P
BA01	GND
BA02	MM_M1_P_PIN_CKC_DAT_12_N
BA03	MM_M1_P_PIN_CKC_DAT_08_P
BA04	MM_M1_P_PIN_CKC_DAT_07_P
BA05	MM_M1_P_PIN_CKC_DAT_05_N
BA06	GND
BA07	SH_PIN_P_M1_CKB_DAT_15_P
BA08	PV_CT_M_PIN_SEEPROM0_DATA
BA09	GND
BA10	MM_PIN_P_M1_CKD_DAT_00_P

Position	Net Name
BA11	MM_PIN_P_M1_CKD_DAT_00_N
BA12	GND
BA13	GND
BA14	TS_CT_P_PIN_M1_T_PLLHFC_MKERF_P
BA15	TS_CT_P_PIN_M1_T_PLLHFC_MKERF_N
BA16	GND
BA17	PV_PIN_P_CT_M1_TERMREF_P
BA18	PV_PIN_P_CT_M1_TERMREF_N
BA19	GND
BA20	GND
BA21	MM_CT_B_PIN_MB_FSI7_DATA
BA22	MM_CT_P_PIN_MB_FSI7_CLK
BA23	GND
BA24	MM_CT_B_PIN_MB_FSI2_DATA
BA25	MM_CT_P_PIN_MB_FSI2_CLK
BA26	GND
BA27	PV_PIN_B_CT_I2CSL_SCL
BA28	PV_PIN_B_CT_I2CSL_SDA
BA29	GND
BA30	GND
BA31	GND
BA32	GND
BA33	PE_PIN_P_CT_E1_PRSNT1_B
BA34	GND
BA35	PE_PIN_P_E1_CK0_DAT_00_N
BA36	PE_PIN_P_E1_CK0_DAT_00_P
BA37	PE_PIN_P_E1_CK0_DAT_02_N
BA38	PE_PIN_P_E1_CK0_DAT_02_P
BA39	GND
BA40	SH_PIN_P_CT_FSP1_FSI_CLK
BA41	GND
BA42	NA_PIN_P_A2_CK0_DAT_07_P
BA43	NA_PIN_P_A2_CK0_DAT_09_N
BA44	NA_PIN_P_A2_CK0_DAT_10_P
BA45	NA_PIN_P_A2_CK0_DAT_11_N
BA46	GND
BA47	NA_PIN_P_A1_CK0_DAT_20_P

Position	Net Name
BA48	NA_PIN_P_A1_CK0_DAT_22_N
BB01	MM_M1_P_PIN_CKC_DAT_11_N
BB02	MM_M1_P_PIN_CKC_DAT_12_P
BB03	MM_M1_P_PIN_CKC_CLK_P
BB04	MM_M1_P_PIN_CKC_DAT_07_N
BB05	GND
BB06	SH_PIN_P_M1_CKB_DAT_06_P
BB07	SH_PIN_P_M1_CKB_DAT_13_P
BB08	GND
BB09	MM_PIN_P_M1_CKD_DAT_01_N
BB10	MM_PIN_P_M1_CKD_DAT_01_P
BB11	MM_PIN_P_M1_CKD_DAT_02_P
BB12	MM_PIN_P_M1_CKD_DAT_02_N
BB13	GND
BB14	GND
BB15	GND
BB16	MM_PIN_P_M1_CKC_DAT_07_N
BB17	MM_PIN_P_M1_CKC_DAT_07_P
BB18	MM_PIN_P_M1_CKC_DAT_23_P
BB19	MM_PIN_P_M1_CKC_DAT_23_N
BB20	GND
BB21	GND
BB22	MM_CT_P_PIN_MB_FSI6_CLK
BB23	MM_CT_B_PIN_MB_FSI6_DATA
BB24	GND
BB25	PV_CT_P_PIN_FSI1_CLK
BB26	PV_CT_B_PIN_FSI1_DATA
BB27	GND
BB28	PV_CT_P_PIN_ATTENTION_B
BB29	GND
BB30	PE_E1_P_PIN_CK0_DAT_01_N
BB31	PE_E1_P_PIN_CK0_DAT_01_P
BB32	PE_E1_P_PIN_CK0_DAT_02_N
BB33	PE_E1_P_PIN_CK0_DAT_02_P
BB34	GND
BB35	GND
BB36	PE_PIN_P_E1_CK0_DAT_01_N
BB37	PE_PIN_P_E1_CK0_DAT_01_P

Position	Net Name
BB38	PE_PIN_P_E1_CK0_DAT_04_N
BB39	PE_PIN_P_E1_CK0_DAT_04_P
BB40	GND
BB41	SH_CT_B_PIN_MB_FSI0_DATA
BB42	GND
BB43	NA_PIN_P_A2_CK0_DAT_09_P
BB44	NA_PIN_P_A2_CK0_CLK_N
BB45	NA_PIN_P_A2_CK0_DAT_11_P
BB46	NA_PIN_P_A2_CK0_DAT_12_N
BB47	GND
BB48	NA_PIN_P_A1_CK0_DAT_22_P
BC01	MM_M1_P_PIN_CKC_DAT_11_P
BC02	MM_M1_P_PIN_CKC_DAT_10_N
BC03	MM_M1_P_PIN_CKC_CLK_N
BC04	GND
BC05	SH_PIN_P_M1_CKB_DAT_18_P
BC06	SH_SPARE_BG01
BC07	GND
BC08	MM_PIN_P_M1_CKD_DAT_03_P
BC09	MM_PIN_P_M1_CKD_DAT_03_N
BC10	MM_PIN_P_M1_CKD_DAT_04_P
BC11	MM_PIN_P_M1_CKD_DAT_04_N
BC12	GND
BC13	MM_PIN_P_M1_CKD_DAT_22_P
BC14	MM_PIN_P_M1_CKD_DAT_22_N
BC15	GND
BC16	GND
BC17	MM_PIN_P_M1_CKC_DAT_08_N
BC18	MM_PIN_P_M1_CKC_DAT_08_P
BC19	MM_PIN_P_M1_CKC_DAT_22_P
BC20	MM_PIN_P_M1_CKC_DAT_22_N
BC21	GND
BC22	GND
BC23	PV_CT_B_PIN_FSI2_DATA
BC24	PV_CT_P_PIN_FSI2_CLK
BC25	GND
BC26	TS_PIN_P_CT_TEST_LSSD_TE
BC27	GND

Position	Net Name	Position	Net Name	Position	Net Name
BC28	TS_PIN_P_CT_STBY_RESET_B	BD18	MM_PIN_P_M1_CKC_DAT_20_N	BE08	MM_PIN_P_M1_CKD_DAT_12_P
BC29	PV_PIN_P_CT_FSI_IN_ENA1	BD19	MM_PIN_P_M1_CKC_DAT_20_P	BE09	MM_PIN_P_M1_CKD_DAT_12_N
BC30	GND	BD20	MM_PIN_P_M1_CKC_DAT_21_N	BE10	GND
BC31	PE_E1_P_PIN_CK0_DAT_00_P	BD21	MM_PIN_P_M1_CKC_DAT_21_P	BE11	MM_PIN_P_M1_CKD_DAT_16_P
BC32	PE_E1_P_PIN_CK0_DAT_00_N	BD22	GND	BE12	MM_PIN_P_M1_CKD_DAT_16_N
BC33	PE_E1_P_PIN_CK0_DAT_04_N	BD23	GND	BE13	MM_PIN_P_M1_CKD_DAT_21_N
BC34	PE_E1_P_PIN_CK0_DAT_04_P	BD24	PV_CT_P_PIN_FSI3_CLK	BE14	MM_PIN_P_M1_CKD_DAT_21_P
BC35	GND	BD25	PV_CT_B_PIN_FSI3_DATA	BE15	GND
BC36	GND	BD26	GND	BE16	MM_PIN_P_M1_CKC_DAT_01_P
BC37	PE_PIN_P_E1_CK0_DAT_03_N	BD27	TS_PIN_P_CT_CARD_TEST	BE17	MM_PIN_P_M1_CKC_DAT_01_N
BC38	PE_PIN_P_E1_CK0_DAT_03_P	BD28	GND	BE18	GND
BC39	PE_PIN_P_E1_CK0_DAT_06_N	BD29	GND	BE19	MM_PIN_P_M1_CKC_DAT_14_P
BC40	PE_PIN_P_E1_CK0_DAT_06_P	BD30	PV_PIN_P_CT_CHIP_ID1	BE20	MM_PIN_P_M1_CKC_DAT_14_N
BC41	GND	BD31	GND	BE21	MM_PIN_P_M1_CKC_DAT_18_N
BC42	SH_CT_P_PIN_MB_FSI0_CLK	BD32	PE_E1_P_PIN_CK0_DAT_03_N	BE22	MM_PIN_P_M1_CKC_DAT_18_P
BC43	GND	BD33	PE_E1_P_PIN_CK0_DAT_03_P	BE23	GND
BC44	NA_PIN_P_A2_CK0_CLK_P	BD34	PE_E1_P_PIN_CK0_DAT_06_N	BE24	GND
BC45	NA_PIN_P_A2_CK0_DAT_13_N	BD35	PE_E1_P_PIN_CK0_DAT_06_P	BE25	GND
BC46	NA_PIN_P_A2_CK0_DAT_12_P	BD36	GND	BE26	GND
BC47	NA_PIN_P_A2_CK0_DAT_14_N	BD37	GND	BE27	GND
BC48	GND	BD38	PE_PIN_P_E1_CK0_DAT_05_N	BE28	PV_PIN_B_CT_FSP0_FSI_DATA
BD01	MM_M1_P_PIN_CKC_DAT_09_N	BD39	PE_PIN_P_E1_CK0_DAT_05_P	BE29	PV_PIN_P_CT_FSP0_FSI_CLK
BD02	MM_M1_P_PIN_CKC_DAT_10_P	BD40	PE_PIN_P_E1_CK1_DAT_00_N	BE30	GND
BD03	GND	BD41	PE_PIN_P_E1_CK1_DAT_00_P	BE31	PE_E1_P_PIN_CK0_DAT_07_N
BD04	SH_PIN_P_M1_CKB_DAT_07_P	BD42	GND	BE32	PE_E1_P_PIN_CK0_DAT_07_P
BD05	SH_PIN_P_M1_CKB_DAT_11_P	BD43	GND	BE33	PE_E1_P_PIN_CK0_DAT_05_N
BD06	GND	BD44	GND	BE34	PE_E1_P_PIN_CK0_DAT_05_P
BD07	MM_PIN_P_M1_CKD_DAT_05_P	BD45	NA_PIN_P_A2_CK0_DAT_13_P	BE35	GND
BD08	MM_PIN_P_M1_CKD_DAT_05_N	BD46	NA_PIN_P_A2_CK0_DAT_18_N	BE36	GND
BD09	MM_PIN_P_M1_CKD_DAT_06_P	BD47	NA_PIN_P_A2_CK0_DAT_14_P	BE37	PE_PIN_P_E1_CK0_DAT_07_P
BD10	MM_PIN_P_M1_CKD_DAT_06_N	BD48	NA_PIN_P_A2_CK0_DAT_15_N	BE38	PE_PIN_P_E1_CK0_DAT_07_N
BD11	GND	BE01	MM_M1_P_PIN_CKC_DAT_09_P	BE39	PE_PIN_P_E1_CK1_DAT_01_N
BD12	MM_PIN_P_M1_CKD_DAT_20_P	BE02	GND	BE40	PE_PIN_P_E1_CK1_DAT_01_P
BD13	MM_PIN_P_M1_CKD_DAT_20_N	BE03	SH_PIN_P_M1_CKB_DAT_20_P	BE41	GND
BD14	MM_PIN_P_M1_CKD_DAT_23_P	BE04	SH_PIN_P_M1_CKB_DAT_16_P	BE42	GND
BD15	MM_PIN_P_M1_CKD_DAT_23_N	BE05	GND	BE43	NA_PIN_P_A2_CK0_DAT_22_P
BD16	GND	BE06	MM_PIN_P_M1_CKD_DAT_07_P	BE44	NA_PIN_P_A2_CK0_DAT_22_N
BD17	GND	BE07	MM_PIN_P_M1_CKD_DAT_07_N	BE45	GND

Position	Net Name	Position	Net Name	Position	Net Name
BE46	NA_PIN_P_A2_CK0_DAT_18_P	BF36	GND	BG26	MM_PIN_P_M1_CKC_DAT_16_N
BE47	NA_PIN_P_A2_CK0_DAT_16_N	BF37	GND	BG27	MM_PIN_P_M1_CKC_DAT_16_P
BE48	NA_PIN_P_A2_CK0_DAT_15_P	BF38	PE_PIN_P_E1_CK1_DAT_03_P	BG28	GND
BF01	GND	BF39	PE_PIN_P_E1_CK1_DAT_03_N	BG29	GND
BF02	SH_PIN_P_M1_CKB_DAT_19_P	BF40	PE_PIN_P_E1_CK1_DAT_02_N	BG30	PE_E1_P_PIN_CK1_DAT_07_P
BF03	SH_PIN_P_M1_CKB_DAT_08_P	BF41	PE_PIN_P_E1_CK1_DAT_02_P	BG31	PE_E1_P_PIN_CK1_DAT_07_N
BF04	GND	BF42	GND	BG32	GND
BF05	MM_PIN_P_M1_CKD_DAT_08_N	BF43	GND	BG33	PE_E1_P_PIN_CK1_DAT_05_P
BF06	MM_PIN_P_M1_CKD_DAT_08_P	BF44	NA_PIN_P_A2_CK0_DAT_21_P	BG34	PE_E1_P_PIN_CK1_DAT_05_N
BF07	MM_PIN_P_M1_CKD_DAT_11_P	BF45	NA_PIN_P_A2_CK0_DAT_21_N	BG35	PE_E1_P_PIN_CK1_DAT_03_N
BF08	MM_PIN_P_M1_CKD_DAT_11_N	BF46	GND	BG36	PE_E1_P_PIN_CK1_DAT_03_P
BF09	GND	BF47	NA_PIN_P_A2_CK0_DAT_16_P	BG37	GND
BF10	MM_PIN_P_M1_CKD_DAT_14_P	BF48	NA_PIN_P_A2_CK0_DAT_17_N	BG38	GND
BF11	MM_PIN_P_M1_CKD_DAT_14_N	BG01	SH_PIN_P_M1_CKB_DAT_23_P	BG39	PE_PIN_P_E1_CK1_DAT_07_N
BF12	MM_PIN_P_M1_CKD_DAT_19_N	BG02	SH_PIN_P_M1_CKB_DAT_22_P	BG40	PE_PIN_P_E1_CK1_DAT_07_P
BF13	MM_PIN_P_M1_CKD_DAT_19_P	BG03	GND	BG41	PE_PIN_P_E1_CK1_DAT_05_P
BF14	GND	BG04	MM_PIN_P_M1_CKD_DAT_09_P	BG42	PE_PIN_P_E1_CK1_DAT_05_N
BF15	MM_PIN_P_M1_CKC_DAT_00_P	BG05	MM_PIN_P_M1_CKD_DAT_09_N	BG43	GND
BF16	MM_PIN_P_M1_CKC_DAT_00_N	BG06	MM_PIN_P_M1_CKD_CLK_P	BG44	GND
BF17	MM_PIN_P_M1_CKC_DAT_04_P	BG07	MM_PIN_P_M1_CKD_CLK_N	BG45	NA_PIN_P_A2_CK0_DAT_20_P
BF18	MM_PIN_P_M1_CKC_DAT_04_N	BG08	GND	BG46	NA_PIN_P_A2_CK0_DAT_20_N
BF19	GND	BG09	MM_PIN_P_M1_CKD_DAT_15_P	BG47	GND
BF20	MM_PIN_P_M1_CKC_DAT_11_P	BG10	MM_PIN_P_M1_CKD_DAT_15_N	BG48	NA_PIN_P_A2_CK0_DAT_17_P
BF21	MM_PIN_P_M1_CKC_DAT_11_N	BG11	MM_PIN_P_M1_CKD_DAT_18_N	BH03	SH_PIN_P_M1_CKB_DAT_21_P
BF22	MM_PIN_P_M1_CKC_DAT_13_P	BG12	MM_PIN_P_M1_CKD_DAT_18_P	BH04	GND
BF23	MM_PIN_P_M1_CKC_DAT_13_N	BG13	GND	BH05	MM_PIN_P_M1_CKD_DAT_10_P
BF24	GND	BG14	SH_PIN_P_M1_CKB_DAT_17_P	BH06	MM_PIN_P_M1_CKD_DAT_10_N
BF25	MM_PIN_P_M1_CKC_DAT_17_N	BG15	GND	BH07	GND
BF26	MM_PIN_P_M1_CKC_DAT_17_P	BG16	MM_PIN_P_M1_CKC_DAT_03_P	BH08	MM_PIN_P_M1_CKD_DAT_13_P
BF27	GND	BG17	MM_PIN_P_M1_CKC_DAT_03_N	BH09	MM_PIN_P_M1_CKD_DAT_13_N
BF28	GND	BG18	MM_PIN_P_M1_CKC_DAT_06_P	BH10	MM_PIN_P_M1_CKD_DAT_17_N
BF29	PV_PIN_P_CT_FSI_SMD	BG19	MM_PIN_P_M1_CKC_DAT_06_N	BH11	MM_PIN_P_M1_CKD_DAT_17_P
BF30	PV_PIN_P_CT_CHIP_ID0	BG20	GND	BH12	GND
BF31	GND	BG21	MM_PIN_P_M1_CKC_DAT_10_P	BH13	GND
BF32	PE_E1_P_PIN_CK1_DAT_01_P	BG22	MM_PIN_P_M1_CKC_DAT_10_N	BH14	MM_PIN_P_M1_CKC_DAT_02_P
BF33	PE_E1_P_PIN_CK1_DAT_01_N	BG23	MM_PIN_P_M1_CKC_DAT_12_P	BH15	MM_PIN_P_M1_CKC_DAT_02_N
BF34	PE_E1_P_PIN_CK1_DAT_00_N	BG24	MM_PIN_P_M1_CKC_DAT_12_N	BH16	GND
BF35	PE_E1_P_PIN_CK1_DAT_00_P	BG25	GND	BH17	MM_PIN_P_M1_CKC_DAT_05_P

Position	Net Name
BH18	MM_PIN_P_M1_CKC_DAT_05_N
BH19	MM_PIN_P_M1_CKC_DAT_09_P
BH20	MM_PIN_P_M1_CKC_DAT_09_N
BH21	GND
BH22	MM_PIN_P_M1_CKC_CLK_P
BH23	MM_PIN_P_M1_CKC_CLK_N
BH24	MM_PIN_P_M1_CKC_DAT_15_P
BH25	MM_PIN_P_M1_CKC_DAT_15_N
BH26	GND
BH27	MM_PIN_P_M1_CKC_DAT_19_N
BH28	MM_PIN_P_M1_CKC_DAT_19_P
BH29	GND
BH30	GND
BH31	PE_E1_P_PIN_CK1_DAT_06_P
BH32	PE_E1_P_PIN_CK1_DAT_06_N
BH33	GND
BH34	PE_E1_P_PIN_CK1_DAT_04_P
BH35	PE_E1_P_PIN_CK1_DAT_04_N
BH36	PE_E1_P_PIN_CK1_DAT_02_N
BH37	PE_E1_P_PIN_CK1_DAT_02_P
BH38	GND
BH39	GND
BH40	PE_PIN_P_E1_CK1_DAT_06_N
BH41	PE_PIN_P_E1_CK1_DAT_06_P
BH42	PE_PIN_P_E1_CK1_DAT_04_P
BH43	PE_PIN_P_E1_CK1_DAT_04_N
BH44	GND
BH45	GND
BH46	NA_PIN_P_A2_CK0_DAT_19_P
BH47	NA_PIN_P_A2_CK0_DAT_19_N
BH48	GND

Glossary

AES	Advanced Encryption Standard
ASIC	Application-specific integrated circuit
BIST	Built-in self-test
BMC	Baseboard management controller
BR	Branch register unit
CAI	Coherent accelerator
CMOS	Complementary metal–oxide–semiconductor
CPM	Critical path monitor
CR	Condition register unit
DDR	Double data rate
DFE	Decision feedback equalizer
DFU	Decimal floating-point unit
DIMM	Dual in-line memory module
DMA	Direct memory attach
DMI	Differential memory interface
DRAM	Dynamic random access memory
DTS	Digital thermal sensor
ECO	Extended cache option
ECID	Electronic chip identification
ECRC	End-to-end CRC
EDI	Elastic differential I/O
EEH	Enhance error handling
EEPROM	Electrically erasable programmable read-only memory
EI4	Elastic interface 4
ET	Early time
FC PLGA	Flip-chip plastic land grid array
FIFO	First-in, first-out
FSI	Flexible service interface

FSP	Flexible service processor
FXU	Fixed-point units
GFW	Global firmware
GT/s	Gigatransfers per second
HCSL	Host clock signal level
HSS	High-speed serial
I^{2}C	Inter-integrated circuit
IEEE	Institute of Electrical and Electronics Engineers
IFU	Instruction fetch units
IP	Intellectual property
ISA	Instruction set architecture
iVRM	Internal voltage regulator module
JTAG	Joint Test Action Group
LCB	Logon control block
LED	Light-emitting diode
LGA	Land grid array
LPAR	Logical partition
LPC	Low pin count bus or lowest point of coherency
LPST	Local Pstate table
LSI	Level signalled interrup
LSSD	Level-sensitive scan design
LSU	Load store units
MFSI	Master FSI
MPG	Multi-protocol gateway
MPUL	Most-positive up level
MSI	Message signalled interrupt
OCC	On-chip controller
OEM	Original equipment manufacturer
PAPR	Power Architecture Platform Reference

PCIe	Peripheral Component Interconnect Express
PE	Partitionable endpoints
PEC	PCI Express controller
PLL	Phase-locked loop
PMC	Power management control
PMCR	Power Management Control Register
PMICR	Power Management Idle Control Register
PMSR	Power Management Status Register
PPM	Parts per million
PSI	Processor support interface
PVR	Processor Version Register
RC	Root complex
SBE	Self-boot engine
SCM	Single-chip module
SCOM	Scan communications
SEEPROM	Serial electrically erasable programmable read-only memory
SMP	Symmetric multiprocessing
SHA	Secure Hash Algorithm
SOI	Silicon on insulator
SPI	Serial peripheral interconnect
SPR	Special-Purpose Register
SRAM	Static random access memory
SVIC	Special, vertical interconnect channel
TCE	Translation control entry
TDP	Thermal design point
TLP	Transaction layer packet
TPM	Trusted platform module
UPS	Uninterrupted power system
VID	Voltage ID

VPD	Vital product data
VLE	Variable length encoding
VRM	Voltage regulator module