DJ-191

Service Manual

CONTENTS

SPECIFICATIONS

Frequency Coverage	TX	RX
DJ-191T (U.S. Amateur version)	144.000 ~ 147.995MHz	135.000 ~ 173.995MHz
DJ-191E (European Amateur version)	144.000 ~ 145.995MHz	144.000 ~ 145.995MHz
DJ-191TA1 (Commercial version VHF-L)	135.000 ~ 150.000MHz	135.000 ~ 173.995MHz
DJ-191TA2 (Commercial version VHF-H)	150.000 ~ 173.995MHz	135.000 ~ 173.995MHz
Channel Step:	5, 10, 12.5, 15, 20, 25, 30kHz steps	
Memory Channels:	40 Channels + 1 Call Channel and 10 Memory	
Antenna Impedance:	50Ω unbalanced	
Frequency Stability:	±5 ppm	
Microphone Input Impedance:	2kΩ nominal.	
Signal Type:	F3E (FM)	
Offset Range:	0 ~ 99.995MHz	
Deviation:	±5kHz max.	
TX Output (supply voltage):	1.5W (4.8V) / 3.5W (7.2V) / 5W (9.6 ~ 13.8V)	
RX Sensitivity:	12dB SINAD better than −16dBμ	
RX Selectivity:	−6dB / ±12kHz	
I.F.:	(1st) 21.25MHz / (2nd) 450kHz	
Power Supply Requirements:	4.8 ~ 13.8V DC (4.8V DC standard)	
Current Consumption at 13.8V DC:	Transmitting: Approx. 1.2 Amp. in High Power Setting	
	Receiving: Squelched Approx. 24mA (BS on)	
Operating Temperature:	−10 ~ +60°C, 14 ~ 140°F	
Dimensions: (with EBP-37N without projections)	57(W) × 151(H) × 28(D) mm $2^{1}/_{4}$(W) × 6(H) × $1^{1}/_{16}$(D) inches	
Weight:	Approx. 300g	
DTMF:	16 Button Keypad, encoder/decoder installed	
Subaudible Tones (CTCSS):	Encoder installed (50 tones)	

CIRCUIT DESCRIPTION

1) Receiver System

The receiver system is a double superheterodyne system with a 21.7 MHz first IF and a 450 kHz second IF.

1. Front End

The received signal at any frequency in the 130.00- to 173.995-MHz range is passed through the low-pass filter (L102, L103, L104, C113, C107, C116, and C114) and tuning circuit (L112 and D107), and amplified by the RF amplifier (Q107). The signal from Q107 is then passed through the tuning circuit (L109, L110, L111, and varicaps D104, D105 and D106) and converted into 21.7 MHz by the mixer (Q106). The tuning circuit, which consists of L112, L109, varicaps D107 and D104, L110, L111, varicaps D105 and D106, is controlled by the tracking voltage from the CPU so that it is optimized for the reception frequency. The local signal from the VCO is passed through the buffer (Q108), and supplied to the source of the mixer (Q106). The radio uses the lower side of the superheterodyne system.

2. IF Circuit

The mixer mixes the received signal with the local signal to obtain the sum of and difference between them. The crystal filter (XF101, XF102) selects 21.7 MHz frequency from the results and eliminates the signals of the unwanted frequencies. The first IF amplifier (Q105) then amplifies the signal of the selected frequency.

3. Demodulator Circuit

After the signal is amplified by the first IF amplifier (Q105), it is input to pin 16 of the demodulator IC (IC104). The second local signal of 21.25 MHz (shared with PLL IC reference oscillation), which is oscillated by the internal oscillation circuit in IC102 and crystal (X101), is input through pin 1 of IC104. Then, these two signals are mixed by the internal mixer in IC104 and the result is converted into the second IF signal with a frequency of 450 kHz. The second IF signal is output from pin 3 of IC104 to the ceramic filter (FL101), where the unwanted frequency band of that signal is eliminated, and the resulting signal is sent back to the IC104 through pins 5 and 7.

The second IF signal input via pin 7 is demodulated by the internal limiter amplifier and quadrature detection circuit in IC104, and output as an audio signal through pin 9.

4. Audio Circuit

The audio signal from pin 9 of IC104 is compensated to the audio frequency characteristics in the de-emphasis circuit (R162, R161, C172, C173) and amplified by the AF amplifier (Q109). The signal is then input to pin 2 of the electronic volume (IC103) for volume adjustment, and output from pin 1. The adjusted signal is sent to the audio power amplifier (IC105) through pin 2 to drive the speaker.

5. Squelch Circuit

Part of the audio signal from pin 9 of IC104 is amplified by the noise filter amplifier consisting of R176, R186, R177, C179, C183, C191, and C194, and the internal noise amplifier in IC104. The desired noise of the signal is output through pin 11 of IC104, to be further amplified by the noise amplifier (Q115). The amplified noise signal is rectified by voltage doubler D109 and input to pin 4 of CPU (IC5).

2) Transmitter System

1. Modulator Circuit

The audio signal is converted to an electric signal in either the internal or external microphone, and input to the microphone amplifier (IC6). IC6 consists of two operational amplifiers; one amplifier (pins 1, 2, and 3) is composed of pre-emphasis and IDC circuits and the other (pins 5, 6, and 7) is composed of a splatter filter. The maximum frequency deviation is obtained by VR2 and input to the cathode of the varicap of the VCO, to change the electric capacity in the oscillation circuit. This produces the frequency modulation.

2. Power Amplifier Circuit

The transmitted signal is oscillated by the VCO, amplified by the pre-drive amplifier (Q102) and drive amplifier (Q101), and input to the power module (IC101). The signal is then amplified by the power module (IC101) and led to the antenna switch (D101) and low-pass filter (L102, L103, L104, C113, C107, C116, and C114), where unwanted high harmonic waves are reduced as needed, and the resulting signal is supplied to the antenna.

3. APC Circuit

Part of the transmission power from the low-pass filter is detected by D103, converted to DC, and then amplified by a differential amplifier. The output voltage controls the bias voltage from pin 2 of the power module (IC101) to maintain the transmission power constant.

3) PLL Synthesizer Circuit

1. PLL

The dividing ratio is obtained by sending data from the CPU (IC5) to pin 2 and sending clock puises to pin 3 of the PLL IC (IC102). The oscillated signal from the VCO is amplified by the buffer (Q117) and input to pin 6 of IC102. Each programmable divider in IC102 divides the frequency of the input signal by N according to the frequency data, to generate a comparison frequency of 5 or 6.25 kHz.

2. Reference Frequency Circuit

The reference frequency appropriate for the channel steps is obtained by dividing the 21.25 MHz reference oscillation (X101) by 4250 or 3400, according to the data from the CPU (IC5). When the resulting frequency is 5 kHz, channel steps of 5, 10, 15, 20, 25, 30, and 50 kHz are used. When it is 6.25 kHz, the 12.5 kHz channel step is used.

3. Phase Comparator Circuit

The PLL (IC102) uses the reference frequency, 5 or 6.25 kHz. The phase comparator in the IC102 compares the phase of the frequency from the VCO with that of the comparison frequency, 5 or 6.25 kHz, which is obtained by the internal divider in IC102.

4. PLL Loop Filter Circuit

If a phase difference is found in the phase comparison between the reference frequency and VCO output frequency, the charge pump output (pin 8) of IC102 generates a pulse signal, which is converted to DC voltage by the PLL loop filter and input to the varicap of the VCO unit for oscillation frequency control.

5. VCO Circuit

A Colpitts oscillation circuit driven by Q301 directly oscillates the desired frequency. The frequency control voltage determined in the CPU (IC5) and PLL circuit is input to the varicaps (D301 and D304). This changes the oscillation frequency, which is amplified by the VCO buffer (Q302) and output from the VCO unit.

Note

The oscillation frequency is determined by turning Q301 ON and OFF.

Displayed frequencies	Q301
TX: 130.00 - 139.995 MHz RX: 130.00 - 161.695 MHz	OFF
TX: 140.00 - 173.995 MHz RX: 161.70 - 173.995 MHz	ON

4) CPU and Peripheral Circuits

1. LCD Display Circuit

The CPU turns ON the LCD via segment and common terminals with 1/3 the duty and 1/3 the bias, at the frame frequency is 85Hz.

2. Display Lamp Circuit

When the LAMP key is pressed, "H" is output from pin 45 of CPU (IC5) to the bases of Q1 and Q12. Q1 and Q12 then turn ON and the LEDs (D1, D3, D14, D15, D16, and D17) light.

3. Reset and Backup Circuits

When the power from the DC jack or external battery increases from 0 V to 2.5 or more, "H" level reset signal is output from the reset IC (IC2) to pin 35 of the CPU (IC5), causing the CPU to reset. The reset signal, however, waits at C6 and R1010, and does not enter the CPU until the CPU clock (X1) has stablized. When the external power drops to 3.2 V or below, the output signal from the backup IC (IC3), which has been input to pin 34 of the CPU, changes from "H" to "L" level. The CPU will then be in the backup state.

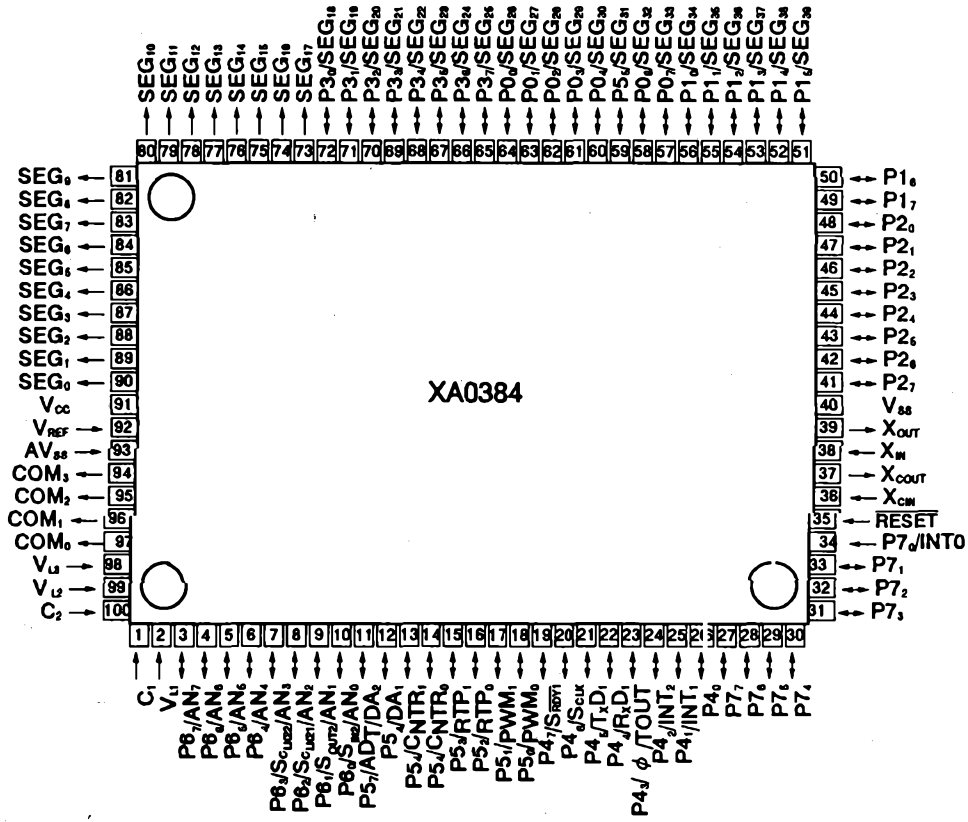
4. S(Signal)Meter Circuit The DC potential of pin 13 of IC104 is input to pin 3 of the CPU (IC5), converted from an analog to a digital signal, and displayed as the S-meter signal on the LCD.

5. DTMF Encoder The CPU (IC5) is equipped with an internal DTMF encoder. The DTMF signal is output from pin 12, through R90 and R91 (for level adjustment), and then through the microphone amplifier (IC6), and is sent to the varicap of the VCO for modulation. At the same time, the monitoring tone passes through the AF circuit and is output from the speaker.

6. DTMF Decoder Part of the audio signal demodulated by IC104 is input to pin 1 of DTMF IC (IC8). The internal signal judging circuit in IC 8 then checks if the signal is valid or invalid. The judged signal is converted into a 4-bit code and sent to pin 29 of IC5.

7. Tone Encoder The CPU (IC5) is equipped with an internal tone encoder. The tone signal (67.0 to 254.1 Hz) is output from pin 11 of the CPU to the varicap of the VCO for modulation.

5) CPU Terminal Functions: M38267M8L (XA0384)



No.	Pin Name	Signal	I/O	Logic	Description
1	C1	C1	-	-	-
2	VL1	VL1	I	A/D	LCD power supply
3	P67/AN7	SMT	I	A/D	S-meter input
4	P66/AN6	SQL	I	A/D	Noise level input for squelch
5	P65/AN5	BAT	I	A/D	Low battery detection input
6	P64/AN4	BP5	I	A/D	Band plan 5
7	P63/CLK22/AN3	BP4	I	-	Band plan 4
8	P62/CLK21/AN2	UL	I	Active high	PLL unlock signal input
9	P61/SOUT2/AN1	BP1,2	I	A/D	Band plans 1 and 2
10	P60/SIN2/AN0	MONI	I	Active low	Monitor key input
11	P57/ADT/DA2	CTOUT	O	D/A	CTCSS tone output
12	P56/AD1	DTOUT	O	D/A	DTMF output
13	P55/CNTR1	TSQD	I	Active low	CTCSS tone detection input/Trunking board detection
14	P54/CNTR0	BEP	O	Pulse	Beep tone output/Band plan 3
15	P53/RTP1	STB2	I/O	Active low/pulse	CTCSS unit detection/Strobe signal to CTCSS unit/Strobe signal to trunking board/Audio line control
16	P52/RTP0	MUTE	I/O	Active high	Microphone mute/Bank change input while trunking
17	P51/PWM1	CLK	O	Pulse	Serial clock output for PLL, CTCSS, and trunking board
18	P50/PWM0	DATA	O	Pulse	Serial data output for PLL, CTCSS, and trunking board
19	P47/SRDY1	ACK	I/O	Pulse	Clock output for DTMF shift out/Band plan 6
20	P46/SCLK1	STB1	O	Pulse	Strobe for PLL IC
21	P45/TXD1	UTX	O	Pulse	UART data transmission output
22	P44/RXD1	URX	I	Pulse	UART data reception input
23	P43/ϕ/TOUT	TBST	O	Pulse	Tone burst (1750Hz) output (European version)
24	P42/INT2	RE2	I	Active low	Rotary encoder input
25	P41/INT1	RE1	I	Active low	
26	P40	PTT	I	Active high	PTT input
27	P77	DSW	O	Active low	DTMF IC ON/OFF
28	P76	STD	I/O	Active high	DTMF signal detection input during reception/Deviation adjustment during transmission
29	P75	DSD	I	Pulse	Decoded DTMF serial data input during reception/Deviation adjustment during transmission
30	P74	T3C	O	Active low	TX power ON/OFF output
31	P73	P3C	O	Active low	PLL power ON/OFF output
32	P72	AFP	O	Active low	AFAMP power ON/OFF output
33	P71	R3C	O	Active low	RX power ON/OFF output
34	P70/INTO	BU	I	Active low	Backup signal detection input
35	RESET	RST	I	Active low	Reset input
36	XCIN	XCIN	-	-	-
37	XCOUNT	XCOUT	-	-	-
38	XIN	XIN	-	-	Main clock input
39	XOUT	XOUT	-	-	Main clock output
40	VSS	GND	-	-	CPU ground
41	P27	PSW	I	Active low	Power switch input
42	P26	SCL	O	Pulse	Serial clock for EEPROM
43	P25	C3C	O	Active high	C3 power ON/OFF output
44	P24	SDA	O	Pulse	Serial data for EEPROM
45	P23	LMP	O	Active high	Lamp ON/OFF
46	P22	T/KEY	I	Active low	Tone burst/LPTT input
47	P21	KO0	I/O	-	Key matrix output/Band plan BP7 input
48	P20	K01	O	-	Key matrix output
49	P17	K02	O	-	
50	P16	K03	O	-	

No.	Pin Name	Signal	I/O	Logic	Description
51	P15/SEG39	F/KEY	I	Active low	Function key input
52	P14/SEG38	K10	I	-	Key matrix input
53	P13/SEG37	K11	I	-	
54	P12/SEG36	K12	I	-	
55	P11/SEG35	K13	I	-	
56	P10/SEG34	K14	I	-	
57	P07/SEG33	SFT	O	-	VCO frequency range change
58	P06/SEG32	SD	O	Active low	Signal detection output
59	P05/SEG31	AFC	O	Active high	AF tone control output
60	P04/SEG30	DA4	O	-	DA converter for electronic volume and output power
61	P03/SEG29	DA3	O	-	
62	P02/SEG28	DA2	O	-	
63	P01/SEG27	DA1	O	-	
64	P00/SEG26	DA0	O	-	
65	P37/SEG25	S25	O	-	LCD segment signal
66	P36/SEG24	S24	O	-	
67	P35/SEG23	S23	O	-	
68	P34/SEG22	S22	O	-	
69	P33/SEG21	S21	O	-	
70	P32/SEG20	S20	O	-	
71	P31/SEG19	S19	O	-	
72	P30/SEG18	S18	O	-	
73	SEG17	S17	O	-	
74	SEG16	S16	O	-	
75	SEG15	S15	O	-	
76	SEG14	S14	O	-	
77	SEG13	S13	O	-	
78	SEG12	S12	O	-	
79	SEG11	S11	O	-	
80	SEG10	S10	O	-	
81	SEG9	S9	O	-	
82	SEG8	S8	O	-	
83	SEG7	S7	O	-	
84	SEG6	S6	O	-	
85	SEG5	S5	O	-	
86	SEG4	S4	O	-	
87	SEG3	S3	O	-	
88	SEG2	S2	O	-	
89	SEG1	S1	O	-	
90	SEG0	S0	O	-	
91	VCC	VDD	–	-	CPU power terminal
92	VREF	VREF	–	-	AD converter power supply
93	AVSS	AVSS	–	-	AD converter ground
94	COM3	COM3	–	-	-
95	COM2	COM2	O	-	LCD COM2 output
96	COM1	COM1	O	-	LCD COM1 output
97	COM0	COM0	O	-	LCD COM0 output
98	VL3	VL3	I	-	LCD power supply
99	VL2	VL2	I	-	LCD power supply
100	C2	I	–	-	-

ADJUSTMENT

1) Required Test Equipment

The following items are required to adjust radio parameters:

1. Regulated power supply	Supply voltage: Current:	5 - 14 VDC 3 A or more
2. Digital multimeter	Voltage range: Current: Input resistance:	FS = Approx. 20 V 10A or more High impedance
3. Oscilloscope	Measurable frequency:	Audio frequency
4. Audio dummy load	Impedance: Dissipation: Jack:	8 Ω 1 W or more 3.5 mm ϕ
5. SSG	Output frequency: Output level: Modulation:	200 MHz or more -20 dB/0.1 μ V - 120dB/1V AM/FM
6. Spectrum Analyzer	Measuring range:	Up to 2 GHz or more
7. Power meter	Measurable frequency: Impedance: Measuring range:	Up to 200 MHz 50 Ω , unbalanced 0.1 W - 10 W
8. Audio volmeter	Measurable frequency: Sensitivity:	Up to 100 kHz 1 mV to 10 V
9. Audio generator	Output frequency: Output impedance:	67 Hz to 10 kHz 600 Ω , unbalanced
10. Distortion meter /SINAD meter	Measurable frequency: Input level: Distortion level:	1 kHz Up to 40 dB 1 % - 100 %
11. Frequency counter	Measurable frequency: Measurable stability:	Up to 200 MHz Approx. +/-0.1 ppm
12. Linear detector	Measurable frequency: Characteristics: CN:	Up to 200 MHz Flat 60 dB or more

Note

- Standard modulation: 1 kHz +/-3.5 kHz/DEV
- Reference sensitivity: 12 dB SINAD
- Specified audio output level: 200 mW at 8 Ω
- Standard audio output level: 50 mW at 8 Ω
- Use an RF cable (3D2W: 1 m) for test equipment.
- Attach a fuse to the RF test equipment.
- All SSG outputs are indicated by EMF.
- Supply voltage for the transceiver: 13.8 VDC

2) Adjustment Mode

The DJ - 191 does not require a serviceperson to manipulate the components on the printed - circuit board, except the trimmer when adjusting reference frequency and deviation. Most of the adjustments for the transceiver are made by using the keys on it while the unit is in the adjustment mode. Because the adjustment mode temporarily uses the channels, frequency must be set on each channel before adjustments can be made. For instructions on how to program the channels, see the "DJ - 191 INSTRUCTION MANUAL" which came with the product. In consideration of the radio environment, the frequency on each channel must be near the value (+/ - 1 MHz) listed in the table below. To enter the adjustment mode, turn the power off, hold down both the UP and DOWN keys, and press the POWER key. "chEc" appears on the LCD for about two seconds, and "C" appears indicating the unit is in the adjustment mode.

Channel frequencies used in the adjustment mode

Channel	Channel function	Frequency
1	Reference frequency adjustment	145 MHz
2	High power adjustment	145 MHz
3	Low power adjustment	145 MHz
4	Minimum frequency sensitivity adjustment	130 MHz
5	Medium frequency sensitivity adjustment	145 MHz
6	Maximum frequency sensitivity adjustment	173 MHz
7	S-meter (1) adjustment	145 MHz
8	S-meter (FULL) adjustment	145 MHz
9	Deviation	145 MHz
10	DTMF (1) test	145 MHz
11	DTMF (D) test	145 MHz
12	Tone 67 Hz test	145 MHz
13	Tone 88.5 Hz test	145 MHz
14	Tone 250.3 Hz test	145 MHz
15	Tone burst test	145 MHz
16	Aging (Not required to use)	145 MHz
20	VCO frequency shift change (Do not change).	-

Caution

- Do not press the (UP) or (DOWN) key while channel 20 is selected in the adjustment mode. Otherwise, the VCO switch frequency will change, causing a malfunction.

Reference Frequency Adjustment

1. In the adjustment mode, select channel 1 by rotating the main tuning dial.
2. Press the (PTT) key to start transmission.
3. Rotate TC101 on the RF circuit board until the value on the frequency counter matches the one displayed on the LCD.

High Power Adjustment

1. In the adjustment mode, select channel 2 by rotating the main tuning dial.
2. Hold down the (F) key and press the (H/L) key to enter the high power mode ("L" at the lower-left of the display disappears).
3. Hold down the (PTT) key to start transmission.
4. While watching the reading of the TX power meter, set the output power to the value closest to 5 W by using the (UP) and (DOWN) keys.
5. When the (PTT) key is released, the output power at that time will be stored as the high power setting.

Low Power Adjustment

1. In the adjustment mode, select channel 3 by rotating the main tuning dial.
2. Hold down the (F) key and press the (H/L) key to enter the low power mode ("L" appears at the lower-left of the display).
3. Hold down the (PTT) key to start transmission.
4. While watching the reading of the TX power meter, set the output power to the value closest to 0.5 W by using the (UP) and (DOWN) keys.
5. When the (PTT) key is released, the output power at that time will be stored as the low power setting.

Minimum Frequency Sensitivity Adjustment

See "Note on Adjusting the Sensitivity" later in this section.

1. In the adjustment mode, select channel 4 by rotating the main tuning dial.
2. Using the (UP) and (DOWN) key, set the minimum frequency sensitivity.

Medium Frequency Sensitivity Adjustment

See "Note on Adjusting the Sensitivity" later in this section.

1. In the adjustment mode, select channel 5 by rotating the main tuning dial.
2. Using the (UP) and (DOWN) key, set the medium frequency sensitivity.

Maximum Frequency Sensitivity Adjustment

See "Note on Adjusting the Sensitivity" later in this section.

1. In the adjustment mode, select channel 6 by rotating the main tuning dial.
2. Using the (UP) and (DOWN) key, set the maximum frequency sensitivity.

S-meter (1) Adjustment

1. In the adjustment mode, select channel 7 by rotating the main tuning dial. The S-meter will show a single star (★).
2. Enter "0" dB μ (EMF) with the transceiver tester.
3. Press the (DOWN) key. The transceiver beeps indicating the new setting has been stored successfully.

S-meter (FULL) Adjustment

1. In the adjustment mode, select channel 8 by rotating the main tuning dial. The S-meter will show all six stars (★ ★ ★ ★ ★ ✪).
2. Enter "+20" dB μ (EMF) with the transceiver tester.
3. Press the (DOWN) key. The transceiver beeps indicating the new setting has been stored successfully.

Deviation

1. In the adjustment mode, select channel 9 by rotating the main tuning dial.
2. Input a 50 mVrms, 1 KMz signal with your transceiver tester through the external microphone jack.
3. With the tester, put the transceiver in the transmission mode.
4. Rotate the VR2 on the printed - circuit board of the transceiver until the deviation is set to 4.5 KHz.

DTMF (1) Test

This function is only for checking the DTMF code, not adjusting it.

1. In the adjustment mode, select channel 10 by rotating the main tuning dial.
2. Press the (PTT) key. DTMF code "1" is automatically sent and you will hear the monitoring tone from the speaker.
3. Check the deviation with the transceiver tester.

DTMF (D) Test

1. In the adjustment mode, select channel 11 by rotating the main tuning dial.
2. Press the (PTT) key. DTMF code "D" is automatically sent and you will hear the monitoring tone from the speaker.
3. Check the deviation with the transceiver tester.

Tone 67 Hz Test

This function is only for checking the tone encoder, not adjusting it.

1. In the adjustment mode, select channel 12 by rotating the main tuning dial.
2. Press the (PTT) key. A 67 Hz tone is automatically sent.
3. Check the deviation with the transceiver tester.

Tone 88.5 Hz Test

1. In the adjustment mode, select channel 13 by rotating the main tuning dial.
2. Press the (PTT) key. An 88.5 Hz tone is automatically sent.
3. Check the deviation with the transceiver tester.

Tone 250.3 Hz Test

1. In the adjustment mode, select channel 14 by rotating the main tuning dial.
2. Press the (PTT) key. A 250.3 Hz tone is automatically sent.
3. Check the deviation with the transceiver tester.

Tone Burst Test

This function is only for checking the tone burst, not adjusting it.

1. In the adjustment mode, select channel 15 by rotating the main tuning dial.
2. Press the (PTT) key. A 1750 Hz tone burst is automatically sent.
3. Check the deviation with the transceiver tester.

Aging

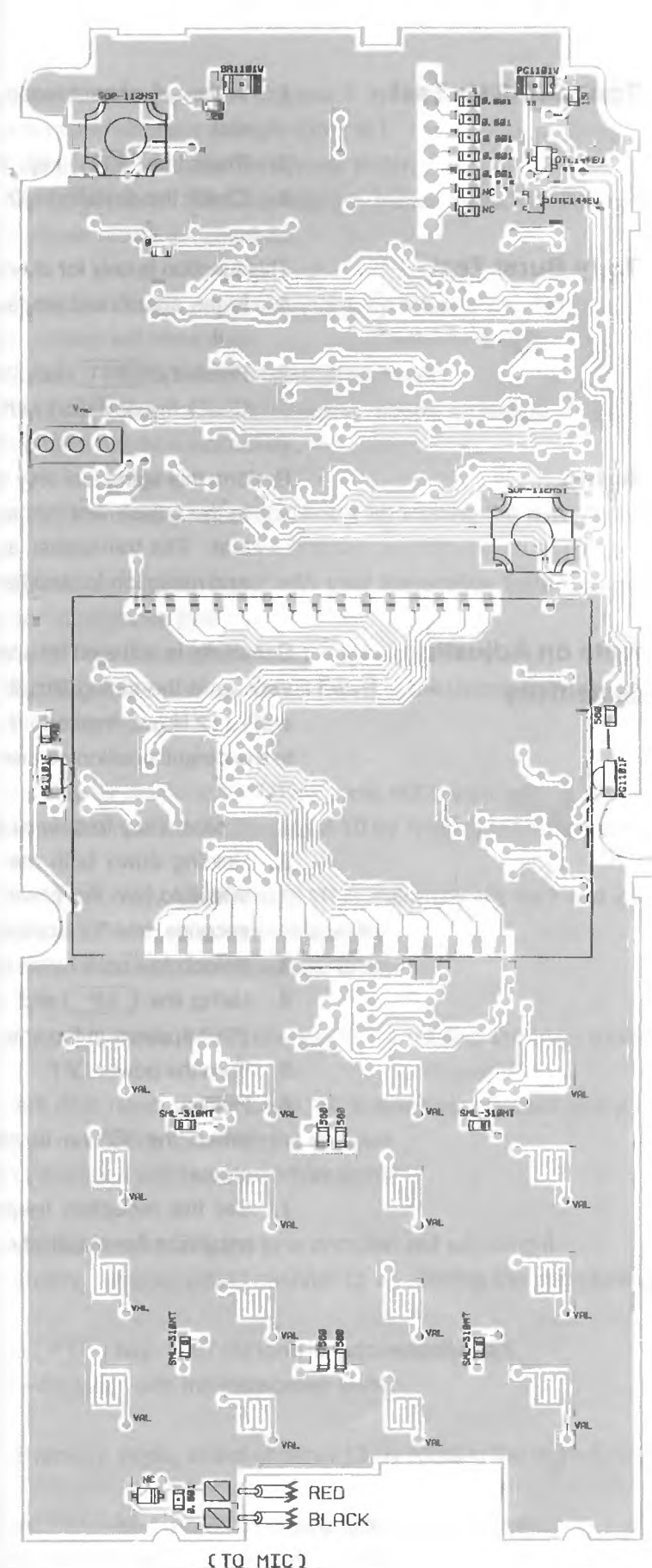
Perform this aging test only when necessary.

1. In the adjustment mode, select channel 16 by rotating the main tuning dial. The transceiver automatically repeats transmission for a minute and reception for another minute.

Note on Adjusting Sensitivity

Sensitivity is adjusted by applying the optimum voltage from the CPU to the varicap of the tuning circuit. The coil manipulation for L109, L110, L111, and L112 is not required. If any of the coils is accidentally rotated, return it to the default position as described below, before adjusting the sensitivity.

1. Program any frequency within 145 MHz +/-1 on memory channel 5.
2. Holding down both the (UP) and (DOWN) key, press the POWER switch to turn the power ON. "chEc" will appears on the LCD for two seconds, and "C" appears.
3. Select channel 5 by rotating the main tuning dial.
4. Using the (UP) and (DOWN) keys, set the adjustment data to "7F" ("7F" appears in the channel number area on the LCD).
5. Turn the power OFF.
6. Holding down both the (UP) and (DOWN) key, turn the power ON. When the "C" no longer appears, the transceiver is in the normal status.
7. Set the reception frequency to 145 MHz +/-1. Rotate the coil to maximize the sensitivity.



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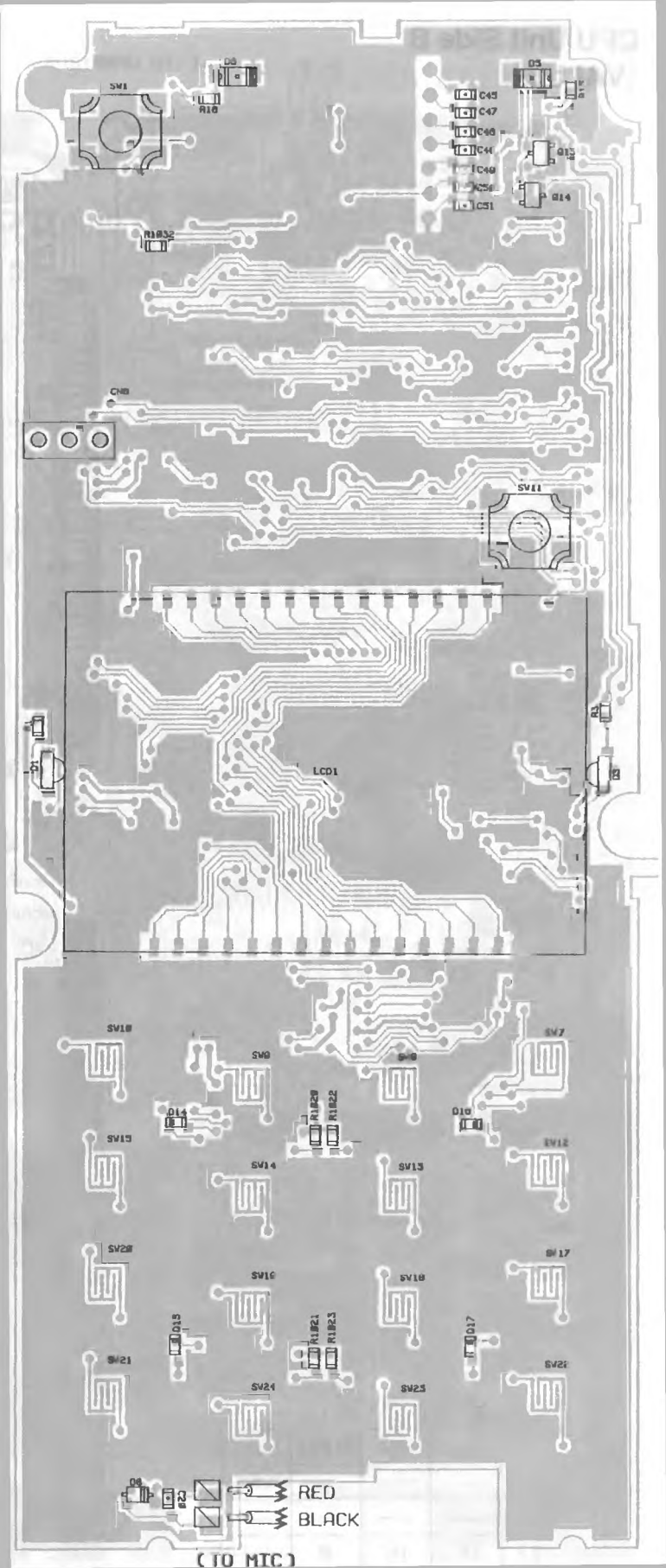
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D5
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C47
C46
C44
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SW9
SW8
SW7
D14
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SW15
SW14
SW13
SW12
SW20
SW16
SW18
SW17
D13
R1021
R1023
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SW24
SW25
SW22
D9
RED
BLACK
(TO MIC)

(TO SPEAKER)

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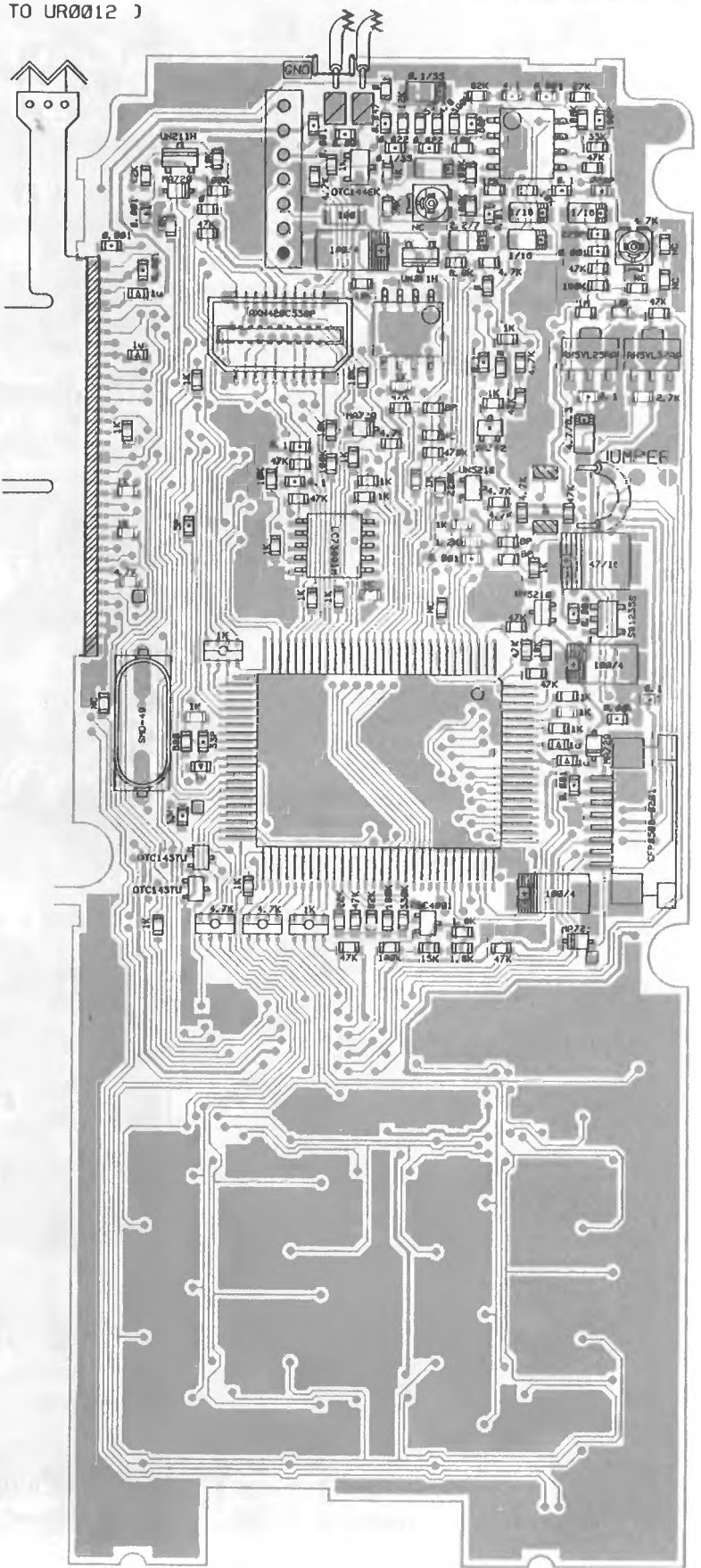
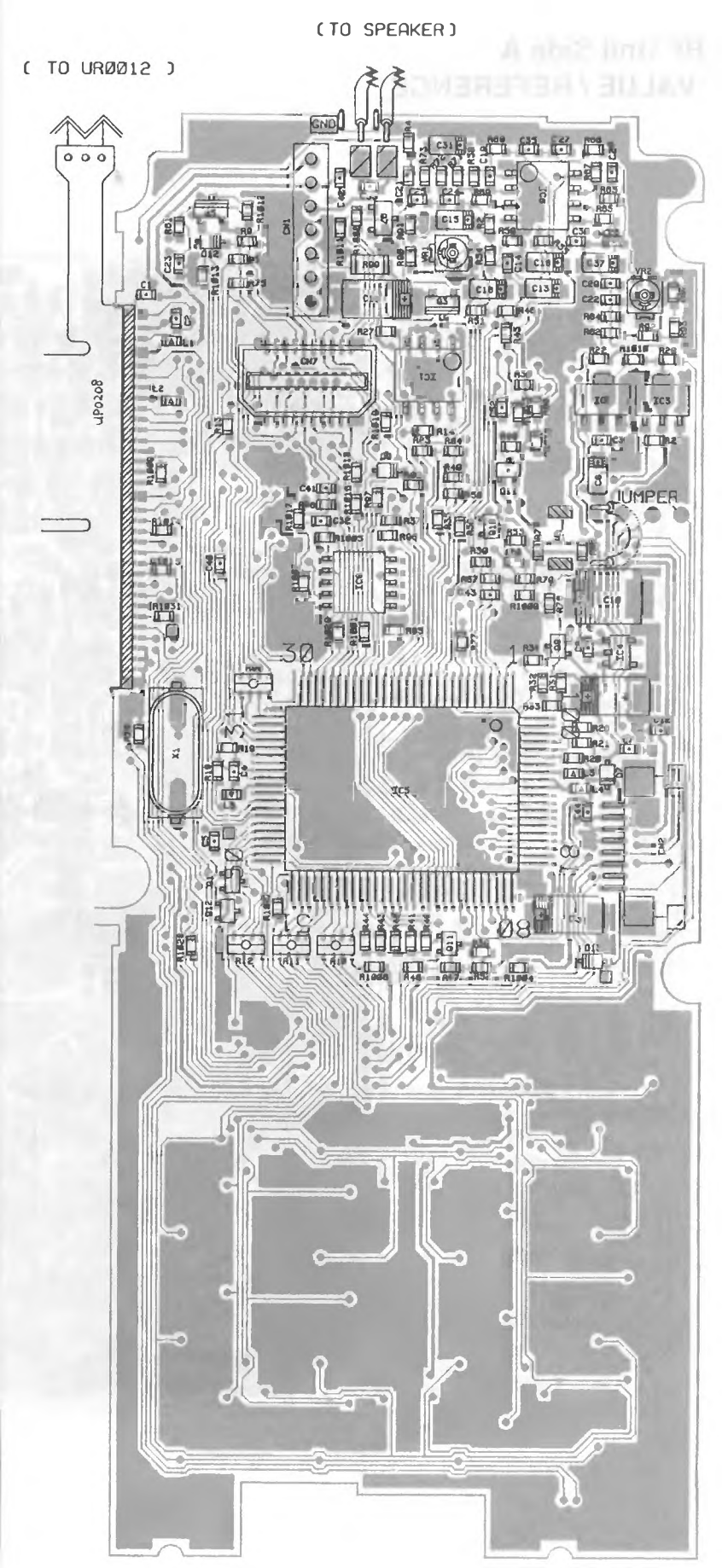
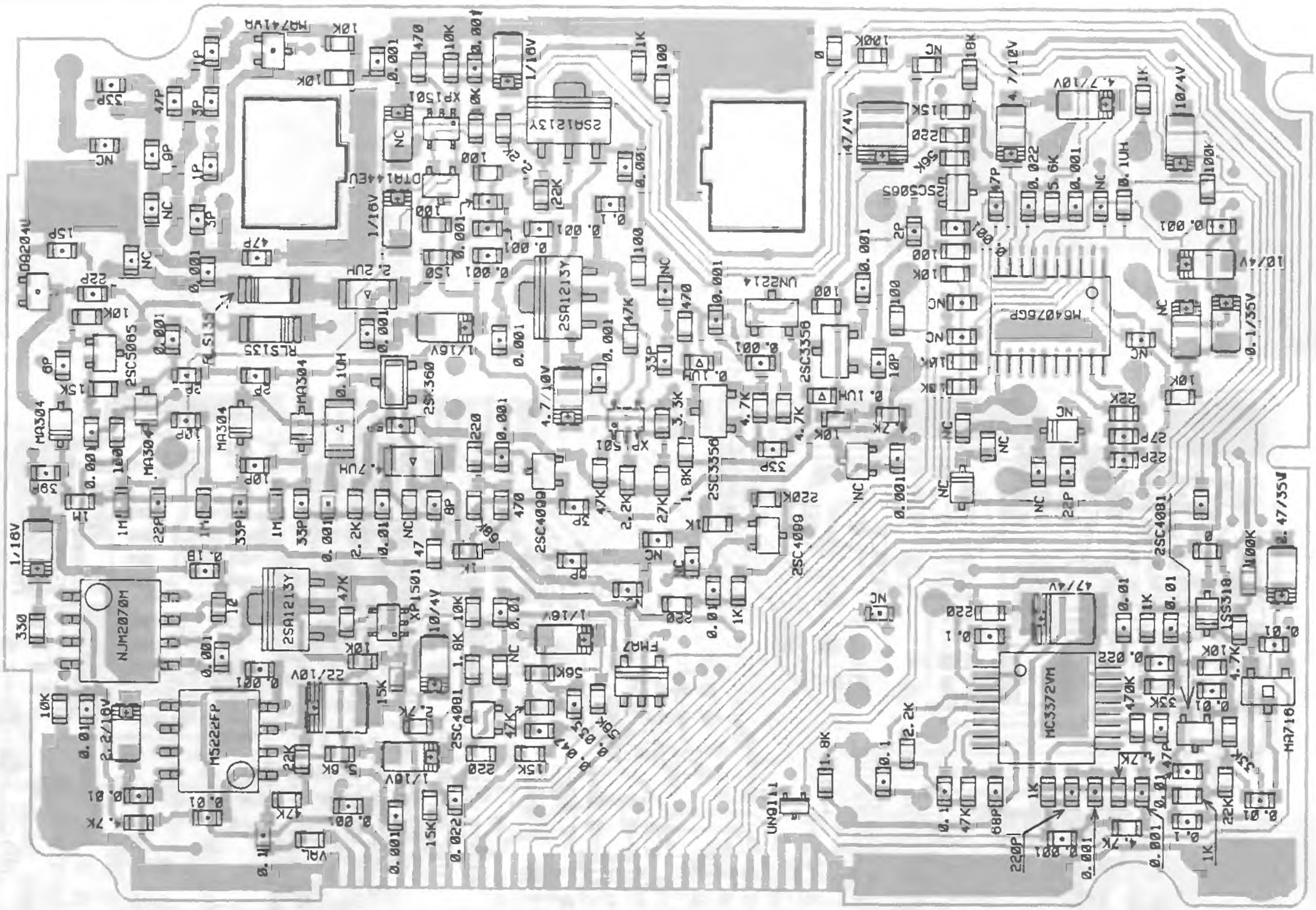


(TO SPEAKER)

(TO UR0012)



ANT
JP01 R-01
L102
0KA65A
L103
0KA65A
L104
0KA65A
L107
0KA75A
L108
0A0071
L109
0A0071
L110
0A0071
L111
0A0071
L112
0A0071
C205
100/16V
+B
TP2
RED
TP1
GND
R168
2.2
C188
100/6V
VR101
NC
IC101
C101
10P
VR102
NC
X101
21.254
CFUM450E
0.1FL
X102
CDBM450C7
XF101
21.7MHZ
XF102
21.7MHZ
C198
100/6V
C199
100/6V


NJM2070M
M5222FP
MC3372VM
M64076GP
2SA1213Y
2SC4001
2SC3356
2SC4009
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2SC5065
XP1501
FMA7
UN9111
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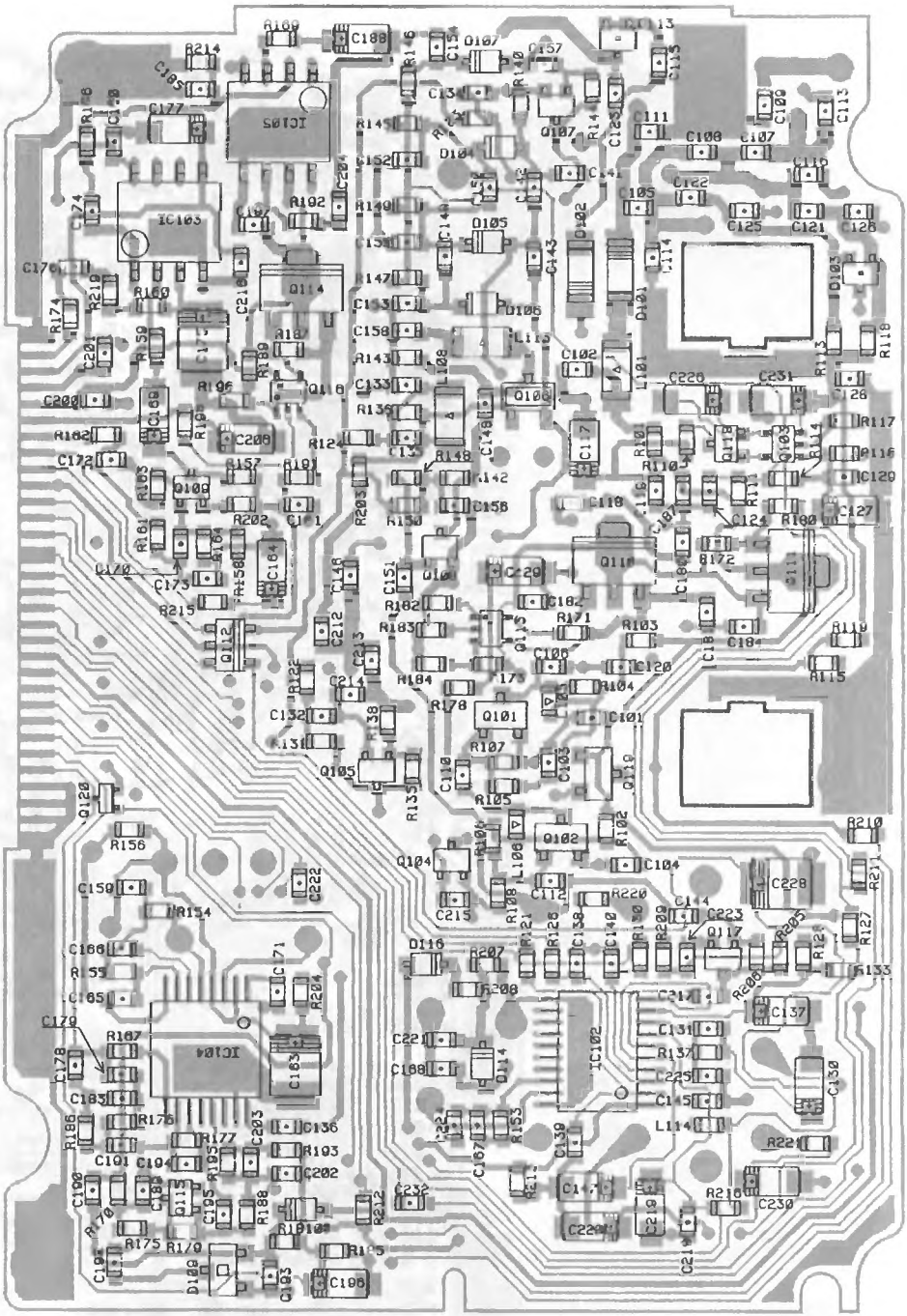
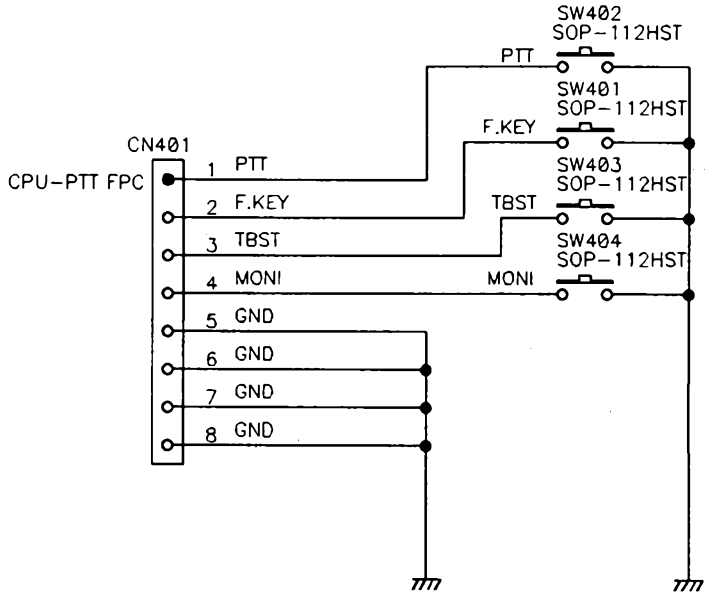
MA716
1SS318
MA304
RLS135
DTA144EU

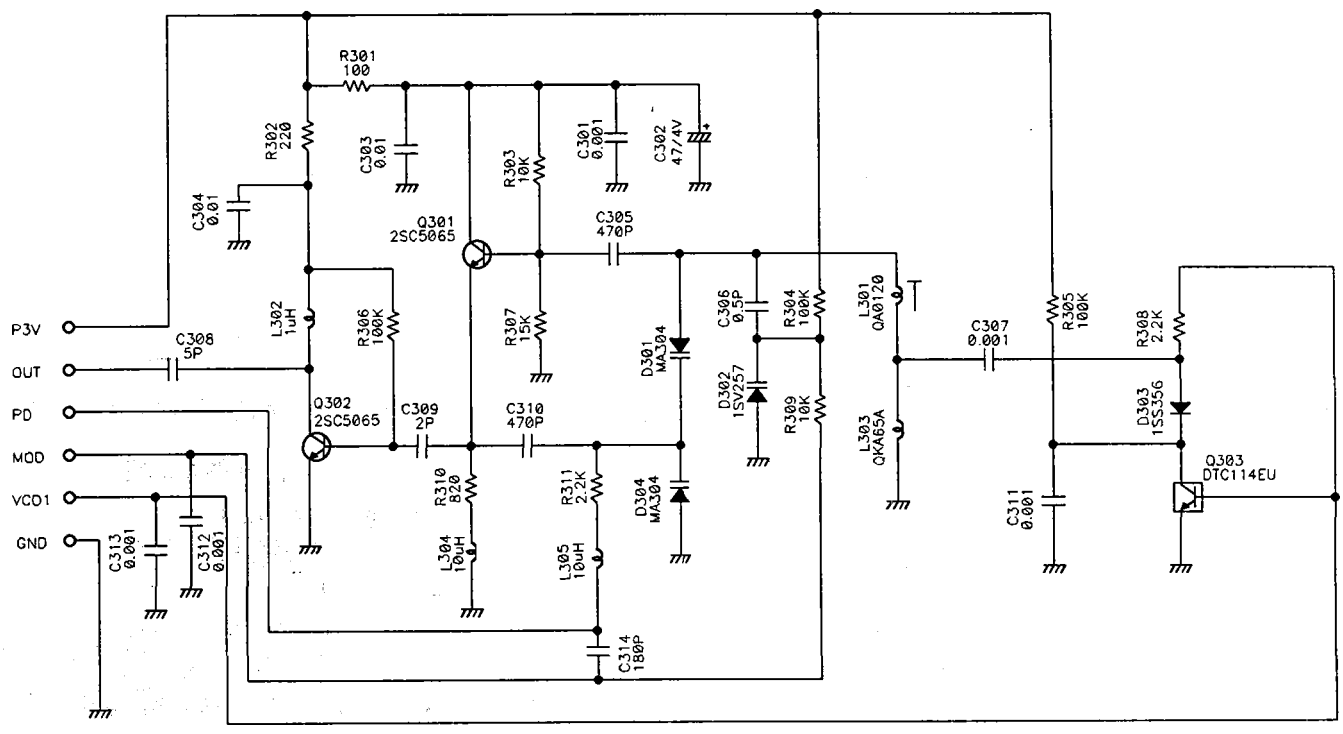


CIRCUIT DIAGRAM

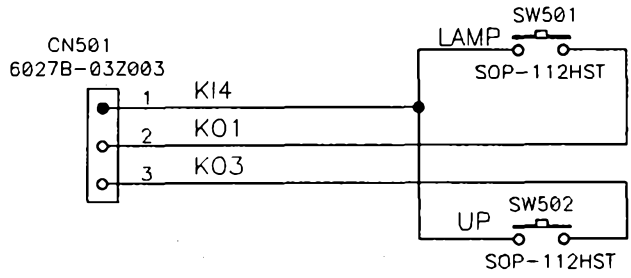
PTT UNIT



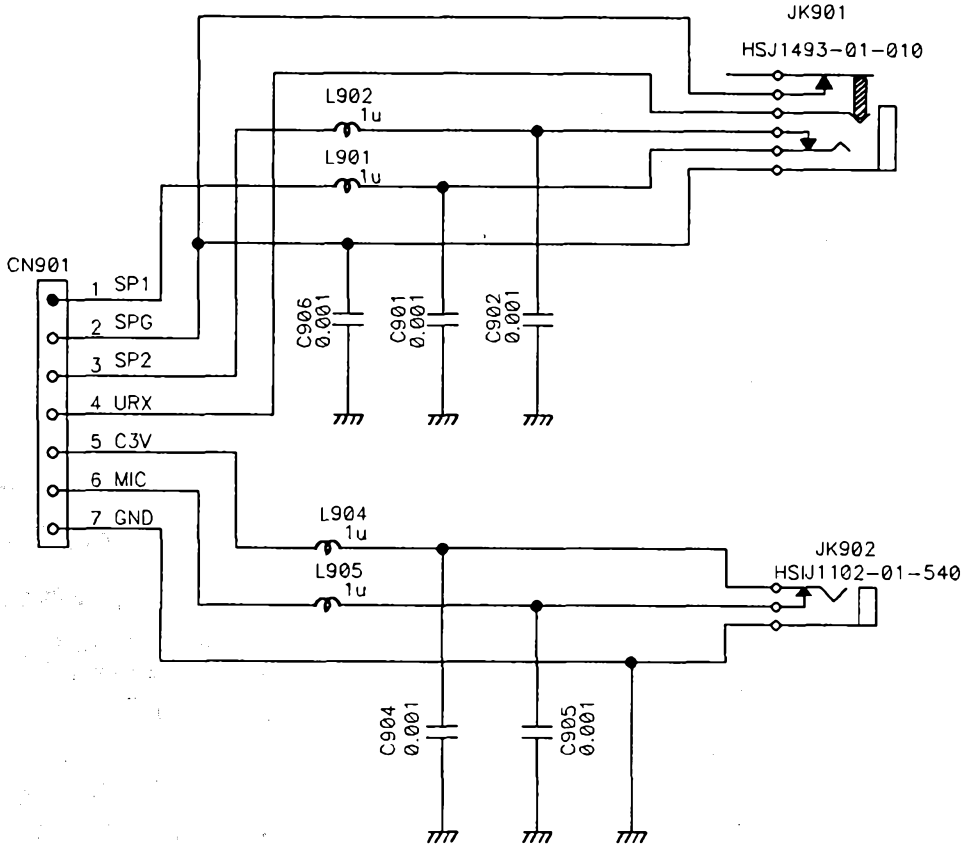
VCO UNIT



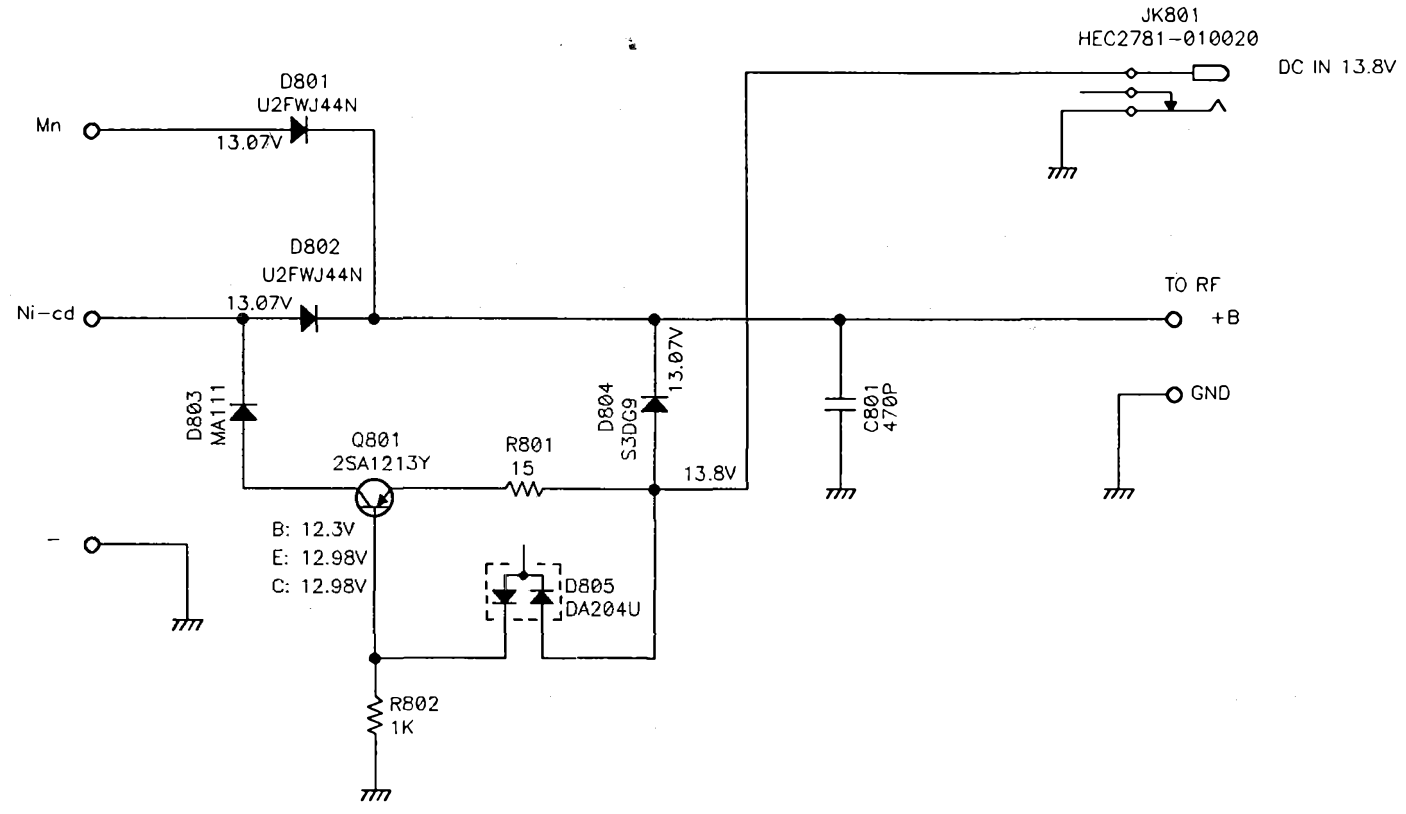
SW UNIT



SP-JACK UNIT



CHARGE UNIT


JK801
HEC2781-010020
DC IN 13.8V
D801
U2FWJ44N
Mn
13.07V
D802
U2FWJ44N
Ni-cd
13.07V
TO RF
+B
GND
D803
MA111
Q801
2SA1213Y
R801
15
D804
S3DG9
13.07V
13.8V
C801
470P
B: 12.3V
E: 12.98V
C: 12.98V
D805
DA204U
R802
1K

CPU UNIT

IC5
M38267M8L

LD1

Q11 2SC4081

Q1 DTC143TU

Q12 DTC143TU

D1,D3 PG1101F

D14–D17 SML-310MT

Q3 UN211H

Q5 UN211H

Q9 UN5210

Q10 UN5210

D7 MA729

D9 MA729

D11 MA742

D12 MA729

IC1 CD5080 24LC16BT

IC2 RH5VL25AA

IC3 RH5VL32AA

IC4 S-81235SG

IC6:A NJM2100M

IC6:B

IC8 LC73881M

X1 4.19MHz SMD-49

SOP-112HST

CN1 JK-CPU_CABLE

CN3 TO RF

CN6

CN7

CFP0508-0201

	R79	R84	R1008	J1
T	—	—	—	JUMPER
TA	—	—	—	—
E	1K	1K	0	—

IC6 (TX)

Pin NO	V
1	85
2	1.88V
3	1.88V
4	0V
5	88V
6	1.88V
7	1.88V
8	3.48V

RF UNIT

RX:145MHz SQ OFF VOL LEVEL 16

TX:145MHz LOW POWER

( )内はTX時

VCO

Q303	B	E	C
RX 130.00-161.7MHz TX 130.00-140.00MHz	3.0V	0V	0V
RX 161.17-174.00MHz TX 140.00-174.00MHz	0V	0V	2.6V

TO CPU BOARD

O CHARGE BOARD